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Battery Management System Design and Implementation of Intelligent Emergency Light Based on the Technology of Loose Capacitance and FSM

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Abstract

This paper presents a design and implement method of battery management system about emergency light based on loose capacitance synchronous sampling measure technology and balanced technology. Through the real-time data acquisition, charge and discharge control, the low voltage detection and protection mechanisms of the system, the system achieves protecting the battery pack of emergency light successfully, collecting data accurately and processing the collected data.

Keywords: *battery management system, loose capacitance, FSM (finite-state machine)*

1. Introduction

Industrial emergency light is often used in coal mining, chemical fuels, iron and steel smelting, civil engineering and other areas of the industrial production and construction, Working environment is poor, influenced by many such as poor ventilation, narrow space, harsh environment, high temperature and flammable, and power supply equipment such as lithium ion battery, nickel zinc battery, nickel metal hydride batteries which may be explosion duing to improper control them, they operate with high voltage and Small volume. However, these features brings the new challenges of the battery management and control , to overcharge, discharge and over current of the single battery will cause irreversible damage to the battery, even cause safety accidents[1]. In china there is no mature research of battery management system for industrial emergency lighting. In this paper, the battery management system provides accurate and reliable maintenance personnel battery status information , various aspects of performance of the battery can implement real-time monitoring, which can also monitor the running data of dynamic measurement and analysis, the battery management system design of the emergency light mainly uses the N to 1 loose capacitance technology, SMBus bus communication protocol, integrated into software design idea of finite state machine[2], the above problems are to be solved ,it is ensured that the emergency light in the industrial environment is safety and stability.

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2. Hardware Design of the System

2.1. The Overall Hardware

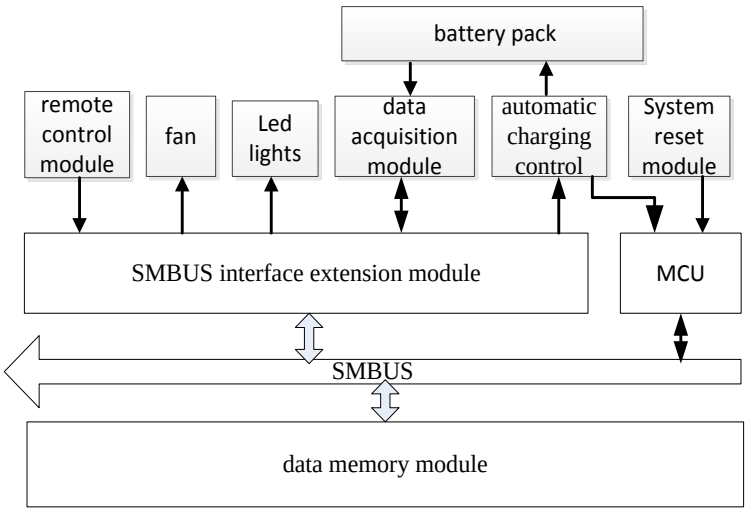


Figure 1. Emergency Light Battery Management Structure Diagram

The system is mainly composed of embedded processor module, data storage module, SMBus bus interface extension module, state display and monitoring module, data acquisition and remote control module, automatic charging control and self-outage of low voltage module, system reset module and other parts. The main hardware modules connected to the SMBus bus which is helpful to realize the standardization and modularization of the circuit [3]. In order to conform to the requirements of the emergency lighting, using nickel zinc D type batteries, nominal capacity 6.50 Ah. The number of single battery is 14, in series, total voltage can reach 26.61V,The structure diagram of hardware system is depicted in Figure 1.

2.2. Processor Circuit

C8051F410 micro controller is the on-chip integration of high frequency oscillation source, and with the multi-level division system to meet the various personalized needs. Port P0~P2 in addition, also included on-chip integrated temperature sensor, power supply and a crystal .Increased the crossbar switch can be flexible on-chip resource allocation to the I/O port, 3.3V low voltage power supply mode, the power consumption of the system kernel is further reduced[4].

The internal oscillator is factory calibrated to 24.5 MHz ±2%. An external oscillator dri ve circuit is also included, allowing an external crystal, ceramic resonator, capacitor, RC, or CMOS clock source to generate the system clock
[5]. A clock multiplier allows for operation at up to 50 MHz. The dedicated smartclock os cillator can be extremely useful in low power applications, allowing the system to maintai n accurate time while the MCU is not powered, or its internal oscillator is suspended. The MCU can be reset or have its oscillator awakened using the smartclock alarm function.

The C8051F410 devices have four operating modes: Active (Normal), Idle, Suspend, a nd Stop. Active mode occurs during normal operation when the oscillator and peripherals are active.Idle mode halts the CPU while leaving the peripherals and internal clocks activ e. Suspend mode halts SYSCLK until a wakening event occurs, which also halts all perip herals using SYSCLK. In Stop mode, the CPU is halted, all interrupts and timers are inact ive, and the internal oscillator is stopped.

The C8051F410 devices include an on-chip 12-bit SAR ADC with a 27-channel single-ended input multiplexer and a maximum throughput of 200 ksps. The ADC system[6] incl udes a configurable analog multiplexer that selects the positive ADC input, which is meas ured with respect to GND. Ports 0-2 are available as ADC inputs; additionally, the on-chip
temperature Sensor output and the core supply voltage (VDD) are available as ADC input s. User firmware may shut down the ADC or use it in Burst Mode to save power.C8051F4 10 minimum microcontroller system diagram is shown in figure 2.

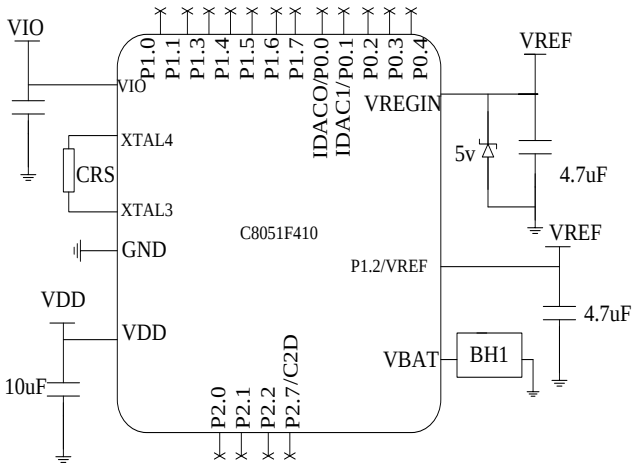


Figure 2. The Minimum System of C8051F410

VIO pins are input port of digital GPIO power, VREGIN pin provides input power source for system operation, P1.2 / VREF pin is a reference voltage output port of ADC, VDD pin provides output port power source of data storage module at the same time as the internal reference voltage. Microcomputer internal has integrated 12 200 Kbps 24 channel ADC, two 12 IDAC, high precision programmable 24.5 MHz internal oscillator, thus, the processor does not need external functional hardware.

2.3. SMBus

SMBus is a two-wire communication patented technology proposed by Intel in 1995, it is fully compliant with the System Management Bus Specification, compatible with I2C serial bus. Compared with the popular high-speed serial protocols, SMBus's slower, but duing to use less hardware to support these protocol products, it still has great application surface in the current computer industry.

(1) SMBus configuration

Figure 3 shows a typical SMBus configuration. Data line SDA and SCL are bidirectional clock line. SMBus interface operating voltage can be between 3.0V and 5.0V, the operating voltage of different devices on the bus can be different. SCL (serial clock) and SDA (serial data) line is bidirectional which must be pulled through a resistor or similar circuit is connected to the power supply voltage [7]. Every device connected to the bus SCL and SDA must be open-drain or open collector, so when the bus is free, both lines are pulled high. SMBus standard transmission rate is 1OOKHz ~ 200KHz.But one tenth up the system clock frequency actually. It depends on the user's settings. When the bus is connected to devices with different speed, it can be used to extend the SCL low time method to synchronize communications between them.

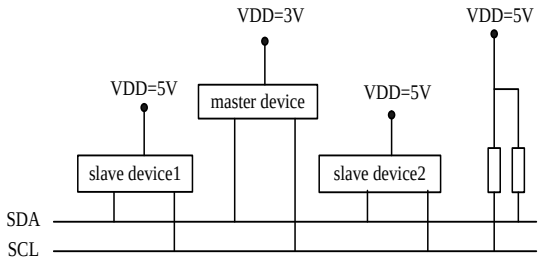


Figure 3. SMBus Configuration

(2) SMBus operation

SMBus interface can operate as a master or slave on the way, the bus can have multiple master devices. If two or more masters initiate a data transfer simultaneously, an arbitration mechanism will ensure that there is a bus master will win. A typical SMBus transaction consists of a START condition (START), an address byte (bits 7-1: seven from the address; Bit 0: R / W direction bit), one or more bytes of data and a Stop condition (STOP)[8]. Each byte received (by a master or slave) must be acknowledgment (ACK) with a low SDA during a high SCL. If the receiving device is not recognized, the transmitting device will read a "not acknowledge" (NACK), which use high SDA during a high SCL representation. Direction bit (R / W) is given at the lowest bit of the address byte. Direction bit is set to logic 1 to indicate "read" (READ) operation, the direction bit is logic 0 to indicate "write" (WRITE) operations. All data are transferred by the master startup, can address one or more the target slave devices. Master generates a start condition, and then sends the address and direction bit. If this data transmitting is a write operation from the master to slave device, the master sends a data byte each and waits confirmation from slave device. If it is a read operation, the slave device sends data and waits for confirmation from the master device. At the end of the data transfer, the master generates a stop condition to terminate the transaction and release the bus.

(3) SMBus transmission

SMBus interface can be configured to operate as a master and / or slave mode. At any one time, it will work in one of the following four ways: the main transmitter, main receiver, the slave transmitter or receiver. SMBus enters the main way in generating initial conditions, and remains in this mode until it generates a stop condition or failure in the bus competition. SMBus generates an interrupt after each byte frames[9]; however, as the receiver interruption generates before the ACK cycle, as a transmitter interruption generates after the ACK cycle time.

2.4. Data Acquisition

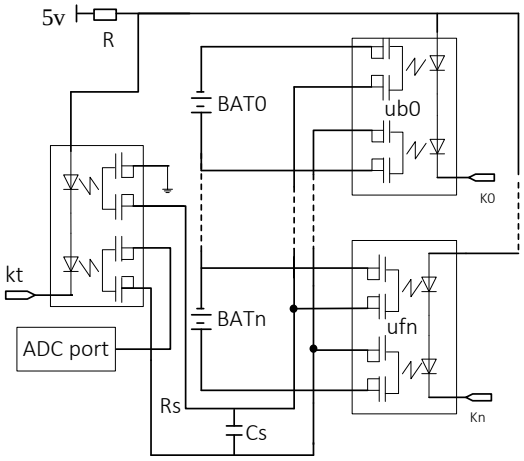
The BMS of emergency light collects data of battery pack, data mainly includes all 14 battery voltage as shown as V0 - V13 , busbar current Is(mA) , battery remaining power SOC (Ah) and the temperature T (K). ADC acquisition ports include two ports of single voltage collection port and busbar current collection port. Busbar current （Is ） is acquired by measuring voltage value of high accuracy sampling resistor Rs (resistance to 3 megohms) , then according to the ohm's law, busbar current (Is) is obtained. Further, since the direction of the current in the battery charge and discharge process is reversed, so as to obtain accurate current values should P1.2 / VREF port provides the reference voltage Vref (2.25V) for the ADC acquisition module. Data collection network adopts PhotoMos Optical Coup solid state relays AQW212 chip of PANASONIC Company. Since PhotoMos using power MOSFET outputs, therefore, compared to the way of conventional optical thyristors and phototransistor, the analog signal acquisition with a shorter time [3], opening and closing the throughput of entire 14 acquisition channels with a total time of less than 15ms. system uses total 16 solid state relays (AQW212), where Ji

(i = 0, 1, 3, ..., 13) are connected in parallel in the battery Bat0-Bat13 positive and negative ends of the individual battery as balancing regulation switch of data collection, voltage and SOC is connected to the side of Cs from N to 1, Jt is connected to the other side of Cs, Jbln uses as a balanced regulatory switch. High-speed CMOS decoder (74HC154 chip) accepts four high effective binary address inputs and provides 16 mutually low outputs. Ji, Jt and Jbln are connected to the output terminals of the chip 74HC154 and control by the chip.74HC154 chip input port connected to the output port of chip PCA9535C[4] IO1 i (i = 0,1, ..., 5).In Which, IO10 and IO11 are respectively connected to / E1 and / E2 to ensure that the received data is correct. IO12, IO13, IO14 and IO15 are respectively connected to the A, B, C, D port, four binary data received from the SMBus I/O bus compiles into 16 kinds of incompatible data to control Ji, Jt, Jbln state [10]. In a complete data collection process, number and serial number of solid-state relays Ji corresponding single BATi, first conduct through Ts(sampling time constant), Vi (voltage value of Single battery) and Cs in parallel Ji off, then make Jt conduction. Sample time constant (Tstc) of flying capacitor calculate formula as (1) and (2), Tcn is conduction delay of AQW212 chip.

$$Tstc = \ln\left|\frac{2^n}{SA}\right| * Rtotal * Cs \quad (1)$$

$$Tsample = Tstc + Tcn \quad (2)$$

The Vi obtained by sampling capacitor Cs is processed by an emitter-follower amplifier circuit and connected to the input of the ADC C8051F410 chip, converted to digital data, upload to SMBus bus. Iron memory chip (FM24C04) receives and saves data. ADC should be set to burst mode to conserve battery consumption. Each round individual voltages acquisition need according to the series order of battery executed the above acquisition steps in sequence. The total voltage of battery is added by the individual voltage, each individual battery voltage is obtained using the width of the signal, many times collection and interval detection [11]. Data collection requires continuous repeat above 16 times of D/A conversion, then using the software algorithm is used to filter out wave value.



A.

Figure 4. Data Acquisition Network

In this design of battery management system , online real-time estimation of remaining capacity SOC rely on ampere-hour (Ah) integration method of battery pack. Battery

temperature protection is adopted the MCU's internal temperature sensor, which output voltage (Vtemp) as ADC inputs., according to the site proposed upper limit of temperature-sensitive, when the thermistor install on the battery pack is sensitive to reach the upper limit of the ADC sample, by the SMBus, MUC immediately start uploading commands of starting fan, when the temperature dropped to below the sensitive lower limit, MCU upload the command of stopping fan. Comparison of the upper and lower temperature by ADC0 window [12], data acquisition network of battery is shown in Figure 4.

Test waveforms of battery management system of emergency light shown in Figure 5. Which, CH1 display switch status timing of Jt, CH2 displays acquisition timing of individual battery voltages. Vi was the enlargement process after collected, and its value is displayed in the oscilloscope. While Jt is low, data acquisition module start collecting individual battery voltages.

B.

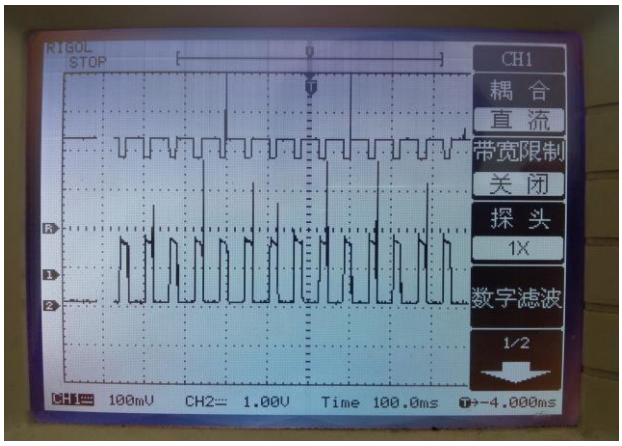


Figure 5. The Photo of the Waveforms of the Model Machine

2.5. Charging Circuit

In order to improve the charging efficiency and life of the battery, the charging process requires an optimal control. Hardware of charging circuit basically is consists of three parts: 220V/380V AC to 30V DC transformer, switch control module, DC power converter.

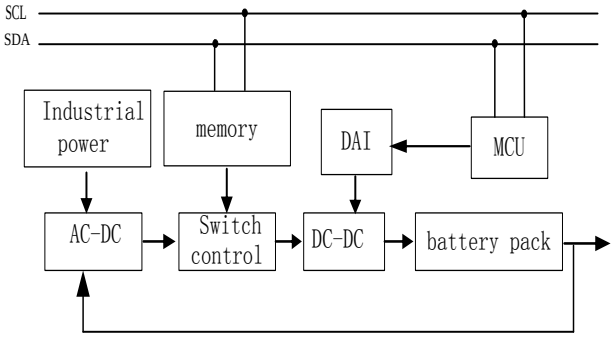


Figure 6. Schematic Diagram of the Charging Circuit and the Control Flow

The charging circuit and the control process are shown in Figure 6.Among them, the DC power converter with XL4016 chip as the design core. XL4016 chip in low-power mode can be used with the characteristics of an adjustable load, linear output and low ripple. DC step-down circuit with typical voltage regulator circuit and switch control

section are provided with XLSEMI, MODFET chip(STN607D) of enhanced insulated gate connects photoelectric coupling chip (PC817) to constitute a switch control part[13] .Going through ACDC transformer Industrial power can be used to supply emergency light. Current output is from the ACDC, to input from the VIN pin of XL4016 chip, whether through source and drain electrodes of STN607D chip, depending on the value of the gate level. The SMBus bus transmits command information to control the open-close state of PC817 chip which connects the gate of STN607D chip, the command status is passed to STN607D [14] to control its gate level. SW end of XL4016 is DC output port, the output current of XL4016 chip pass the LC circuit, then enter the battery charging circuit. FB end is feedback regulation port and connects output port of DAI module of MCU. MCU by constantly rewriting the data word of IDAC's data registers to adjust DC output of SW port can be achieved effects of constant current charging (CC) constant voltage (CV). Charging step: 0.5 C constant current charging 120 min, by the voltage of 1.900 V + / - 0.004 V, then turned to constant voltage of 1.900 V + / - 0.004 V rechargeable 180 min, cut-off current 0.05 C.

2.6. Lamp Charging and Discharging Tests

In this paper, the charging of Miner's lamp were tested, consisting of two 68SC4300mAh batteries[15] in series, content of the test are: charging and discharging process control methods are executed according to expectations.

(1) Charging process

Pre-charge: When the battery voltage is too lower than 3.4V, with a 250mA charge until the charging voltage is greater than 3.4V with 800mA constant current charging.

Constant current charge: 800mA constant current until the voltage to at 3.8V, 3.78V into constant voltage charging. There are four charging cut-off condition to meet any one that stops charging: charging current is less than 250mA; Continuous charging time is more than six hours; Battery voltage greater than 3.8V; SOC value greater than 4.1Ah.

(2) Test method

a. To light when charging, the battery performance testing cabinet records charging time and charging voltage curve;

b. Charging process, with UT805 multi meter to monitor current draw charging current curve;

c. TO light, battery performance testing cabinet records connected discharge voltage curve and discharge time;

(3) Laboratory instruments and equipment

a. UT1805 multi meter, precision four and a half.

b. Model Blue odd 7-120A performance testing cabinets (0.05% FS + 0.05% RD), the resolution 0.1Mv.

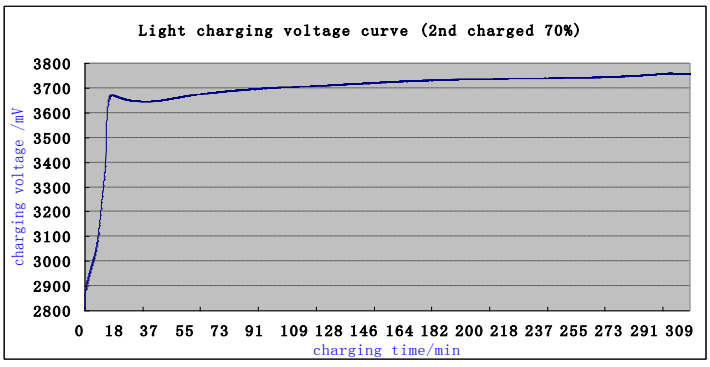


Figure 7. Light Charging Voltage Curve (70% Capacity Battery)

As can be seen from the figure 7, the charging of the battery reaches 70% capacity, in turn charge 30 minutes after the start of the constant voltage charging, constant value of about 3.75V, after charging three hours reaching the cut-off condition, to stop charging. In this case, the battery should be charged fully saturated.

3rd and 4th Test: The following Figure 8 shows charging voltage rises between 3.750V-3.760, followed by constant voltage charging 3rd constant voltage charging time is only 9 minutes, then stop charging. The fourth constant voltage charging time is 26 minutes, then stop charging, the total time between the charging process for 309 minutes and 315 minutes respectively.

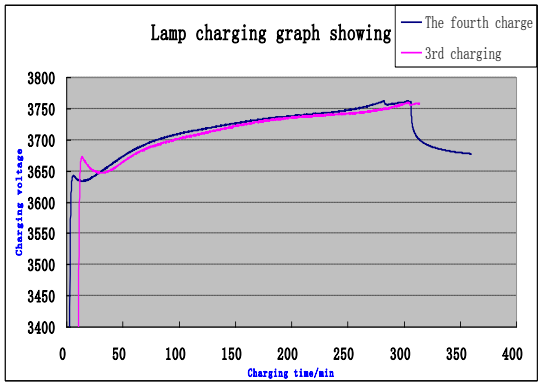


Figure 8. Lamp Charging Graph

2.7. System Self-Shutdown Protection Measures

The BMS of battery can provide protection mechanism based on real-time acquisition of the remaining battery SOC and battery voltage. Mechanism circuit is shown in Figure 9. PP dot is connected to digital input of processor in order to accurately reflect whether the system has power. VO+ is connected to a battery positive terminal, TT port is the switch of system self-shutdown, which is control by SMBus. When the battery pack's remaining electric quantity SOC or individual cell voltage is lower than the lower limit of safe range, the system directly shut down to prevent battery over discharge.

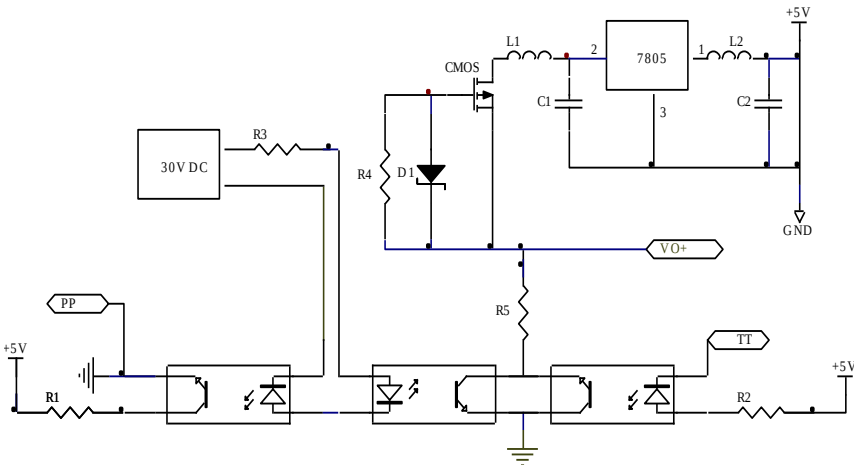


Figure 9. The Schematic Circuit Diagram Of the Low Voltage Detection and System Self-Shutdown Strategy

2.8. Status Display and Remote Control Module

Status display and remote control module by connecting expansion modules of the SMB incorporated into the SMBus interface. the combination of three different colors light-emitting diodes have red, green and blue ,which shows backup and emergency working modes of the emergency light , as well as the SOC and voltage. Remote control module selects HS2272 as remote control decoding circuitry [16], working in radio way, to latch-type or momentary-type data output. After latch type H2272 received an efficient coded the data output which is retained until the next valid received coded. After the transient type H2272 receives a valid encoding, it only instantaneous output data, not retained.

3. Software's Design

BMS software design is based on the FSM machine to optimize. FSM is an abstract mathematical model concept [17] which represents the states of a finite number of stable and non-overlap, also transfers and moves behavior between these states. The idea of finite state machines uses in emergency light battery management system software architecture design, compared with the traditional design process, it brings more benefits. First, predictability and stability, through the system's current state and input trigger events, we can convert the state to the defined other state [18]. Second, improving CPU efficiency, process will be provided minimum system resources and logic code to maintain the current status or action. Third, maintainability, developers methodically analysis of all the state of the system can be achieved, and listed in the table, the benefit in the latter part of software maintenance program modifications. In practical engineering applications, for different instruction data to identify and control to achieve control and scheduling states.

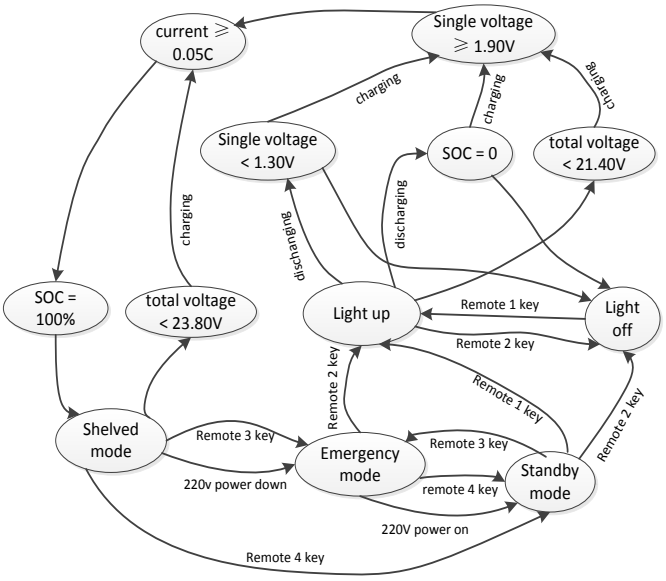


Figure 10. The FSM of the Software Design of the BMS for Emergency Light

Use graphics software to software programs finite state machine (FSM) designed to draw the state transition diagram, which can be complex information, systems and processes to visualize, analyze and communicate. To deepen the understanding of complex information, to make system better optimization, Based on the transfer of state relations and conditions of FSM, A complex program can be turned into multi-branch structure based on a content transfer encoding condition; it is easy to use C language to

achieve [19]. Figure10 shows the emergency light software design model using finite state machine thought.

After power-up, the system is initialized, and then enters a certain cycle management process. Emergency light has three work mode: shelved mode , emergency mode and standby mode, the power of emergency light work mode is supplied by battery, the power of light standby mode is supplied by AC 220V, at the same time the battery is charged, the work mode conversion of emergency light is control by remote and 220V voltage ,when any one state of the single voltage, SOC and the total voltage is below the threshold voltage , the battery is charged until the SOC is 100%, the charge is turned off.

4. Conclusion

By using synchronous sampling Stagecoach capacitance measurement technology, designed battery management system of emergency light. Which the processor parts, battery status data collection network, the charge control system low voltage shutdown protection mechanism, the system is well realized the power management of emergency light, and put into the industrial field use, reflecting in good condition.

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