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FPGA Based Energy Efficient Universal Asynchronous Receiver Transmitter Design Using Thermal Scaling

Rashmi Sharma, Shivani Sharma, Paresh Khaneja, Navya Bhasin and Vanshaj Taxali

Department of electronics and communication
Chitkara University, Chandigarh, India
{rashmisharma1505, shalu16sharma, pareshkhaneja, navya27bhasin, vanshaj1994}@gmail.com
Vaashu Sharma
Department of electronics and communication
NIT Hamirpur, Hamirpur, India
vaashu.sharma@gmail.com

Abstract

This paper throws light on the behavior of the UART in response to the variations in the junction temperature. Analysis has been done to find the most ideal temperature range for the operation of the UART. After all the calculations, deduction comes to a point that lowering the temperature values increases the efficiency of the UART significantly since the losses due to the leakage power are reduced to a minimum value when the temperature is decreased. Significant reduction in the percentage of leakage power is seen as the temperature is lowered. Implementation has been done on the FPGA generations Virtex-6, Virtex-5, Virtex-4 using XILINX simulator and Verilog Hardware Description Language. Different reduction percentages have been observed within a range of 8% to 37.4% for the leakage power and 16.8% to 69.3%for the ambient temperature as the results are obtained for frequency values of 1GHz and 1MHz. Thus various power loss parameters have been studied to get the best energy efficient UART.

Keywords*-FPGA, Energy Efficient, Universal Asynchronous Receiver Transmitter, Thermal Scaling.*

1. Introduction

We have worked on the various generations of the FPGA which stands for field programmable gate array. We have majorly analyzed three generations of FPGA namely Virtex-6, Virtex-5 and Virtex-4.These utilize lesser power, give more performance while absorbing equal power, use low costing materials and has low lead time since the chip can be easily reprogrammed. These are the most recent category of programmable logic devices. The thermal efficiency refers to the useful power divided by the total input power at some specified temperatures. We have analyzed the behavior of UARTa universal asynchronous receiver transmitter, which is a device basically used to transfigure the parallel data to the serial format. The power parameters of the UART have been studied with respect to the leakage power (energy loss via the charged capacitor) and the ambient temperatures (favorable room temperature for carrying out a specific operation). UART is an IC that commune synchronously. It takes data in the form of bytes and transmits it in a sequence. It is used for communication in all the three modes: simplex, half duplex as well as the full duplex mode. We have examined the behavior at 20^{o}C to 60^{o}C temperature ranges. After the research, we conclude that the thermal efficiency increases as we lower the temperatures. As cited here, at a temperature of 20^{o}C, the efficiency is maximum as and when compared to the higher temperatures. By relation:

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$$I_{subthresho\ ld} = A_s \frac{W}{L} v_T^2 (1 - e^{\frac{-V_{DS}}{v_T}}) e^{\frac{(V_{GS} - V_{Th})}{nV_T}} \quad [8]$$

- A_s is a constant whose value depends on temperature.
- V_{th} is the threshold Voltage.
- L is the effective length.
- W is the effective width.
- V_{GS} is the gate to source voltage.
- V_{DS} is the drain to source voltage.
- n is the threshold swing constant.
- V_T is the thermal voltage.

Thus, we infer that as the temperature of the UART is increased, the junction and the leakage power increases. Therefore, the junction temperature as well as the leakage power are directly related to each other.

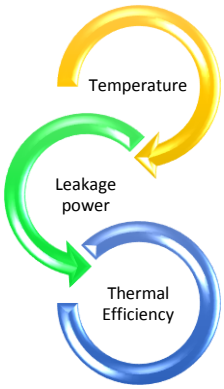


Figure 1. Major Research Parameters

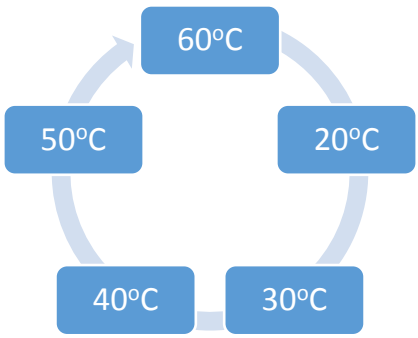


Figure 2. Range of Temperature Used

2. Related Work

A designer had researched on UART [1-2, 4-5, 9-10] some while ago. His basic domain of research was to study the speed matching of the UART and the processor interface however he had not worked upon the power analysis of the UART which has been taken care of in our research [1]. Another researcher had focused on the advantageous implementation of UART using the asynchronous design techniques [2] whereas we have worked on the junction temperature scaling of the UART [2]. Additionally scientist had worked on developing a communication circuit between his personal computer and the microenergy pulse power supply. He had made use of the UART but we have indeed used it differently wherein the behavior of the UART is being observed in context with the

variations in the temperature[3]. Also an analyst had analyzed the UART operation using the asynchronous clock whereas we have mainly dealt with the analysis of the leakage and total power of UART [4]. Another tester had worked on the error detection and the error correction of the UART however we mainly emphasize on the power efficiency of the UART[5].

Another research scholar had worked on energy efficient ROM design based on the ambient temperature however we have worked on the energy saving UART using the varied junction capacitances [6]. Some other researcher had worked on designing an efficient FIR filter for the processing of the digital signals but we have designed an efficient UART and verified it for different temperature values [7].

3. Objective

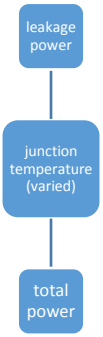


Figure 3. Objective of Energy Efficient UART Design

The major objective of the research is to analyze the changes in the leakage power as well as the total power while maintaining a particular ambient temperature by varying the junction temperature. We aim at perceiving a specified temperature at which the UART behaves to be of maximum utilization i.e. the most energy efficient. This minimizes the losses and increases the productivity of the device hence making it work at its best possible level.

4. Results

Table 1. Results on 1MHz: (Virtex 6)

Temperature	20°C	30°C	40 °C	50 °C	60 °C
Leakage	0.506	0.561	0.623	0.694	0.775
Total	0.506	0.561	0.623	0.694	0.775
Ambient	18.4°C	28.2 °C	38°C	47.8°C	57.6°C

There is 37.4%, 27.6%, 19.6%, 10.4 % reduction in leakage power when we scale down junction temperature from 60 to 20°C, 30°C, 40°C, 50°C respectively as shown in Table 1. There is 68.1%, 51.4%, 34.1%, 17.1% reduction in ambient temperature when we scale down junction temperature from 60 to 20°C, 30°C, 40°C, 50°C respectively as shown in Table 1 and chart 1.

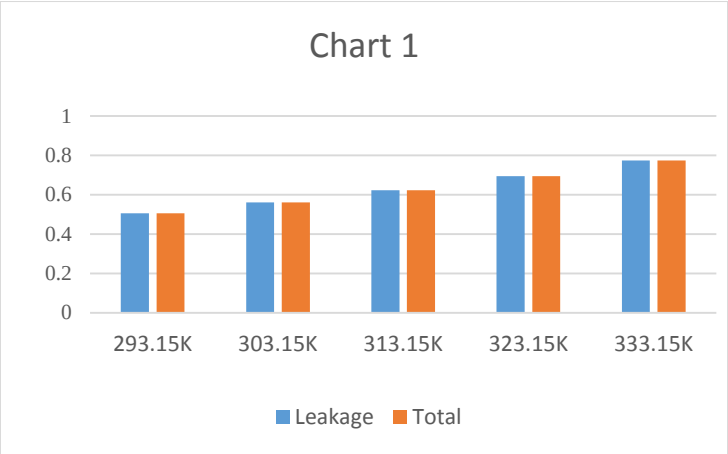


Table 2. Results on 1MHz: (Virtex 5):

Temperature	20°C	30°C	40 °C	50 °C	60 °C
Leakage	0.270	0.299	0.334	0.374	0.422
Total	0.271	0.301	0.335	0.376	0.423
Ambient	19.2°C	29.1°C	39°C	48.9°C	58.8°C

There is 36.1%, 29.1%, 20.9%, 11.4 % reduction in leakage power when we scale down temperature from 60 to 20°C, 30°C, 40°C, 50°C respectively as shown in Table 2. There is 67.3%, 50.5%, 33.4%, 16.8% reduction in ambient temperature when we scale down temperature from 60 to 20°C, 30°C, 40°C, 50°C respectively as shown in Table 2 and chart 2.

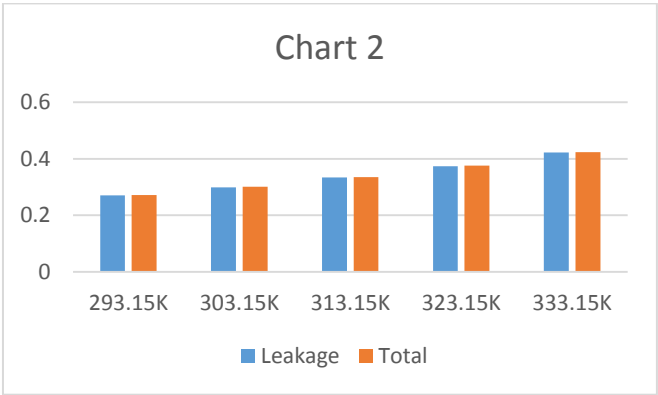


Table 3. Results on 1MHz: (Virtex 4):

Temperature	20°C	30°C	40 °C	50 °C	60 °C
Leakage	0.132	0.140	0.150	0.161	0.175
Total	0.142	0.150	0.160	0.172	0.185
Ambient	17.9°C	27.8 °C	37.6°C	47.5°C	57.3°C

There is 24.5%, 20%, 14.2%, 8 % reduction in leakage power when we scale down junction temperature from 60 to 20°C, 30°C, 40°C, 50°C respectively as shown in Table 3. There is 68.7%, 51.4%, 34.1%, 17.1% reduction in ambient temperature when we scale down junction temperature from 60 to 20°C, 30°C, 40°C, 50°C respectively as shown in Table 3 and chart 3.

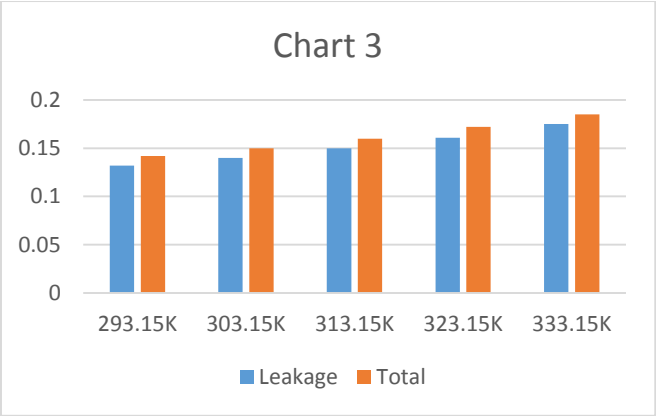


Table 4. Results on 1GHz: (Virtex 6):

Temperature	20°C	30°C	40 °C	50 °C	60 °C
Leakage	0.506	0.561	0.623	0.694	0.775
Total	0.538	0.593	0.656	0.727	0.808
Ambient	18.3°C	28.1 °C	37.9°C	47.7°C	57.5°C

There is 37.4%, 27.6%, 19.6%, 10.4 % reduction in leakage power when we scale down temperature from 60 to 20°C, 30°C, 40°C, 50°C respectively as shown in Table 4. There is 68.1%, 51.1%, 34.1%, 17.1% reduction in ambient temperature when we scale down temperature from 60 to 20°C, 30°C, 40°C, 50°C respectively as shown in Table 4 and chart 4.

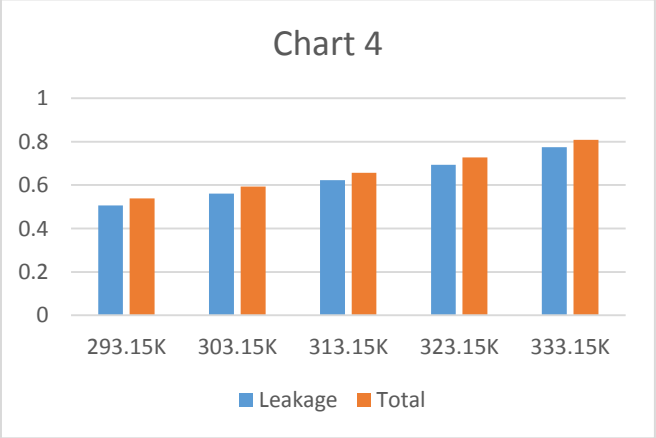


Table 5. Results on 1GHz: (Virtex 5):

Temperature	20°C	30°C	40 °C	50 °C	60 °C
Leakage	0.270	0.299	0.344	0.374	0.422
Total	0.294	0.323	0.358	0.398	0.446
Ambient	19.1°C	29.1 °C	39.0°C	48.8°C	58.7°C

There is 36.1%, 29.1%, 20.9%, 11.4 % reduction in leakage power when we scale down temperature from 60 to 20°C, 30°C, 40°C, 50°C respectively as shown in Table 5. There is 67.3%, 50.5%, 33.5%, 16.8% reduction in ambient temperature when we scale down temperature from 60 to 20°C, 30°C, 40°C, 50°C respectively as shown in Table 5 and chart 5.

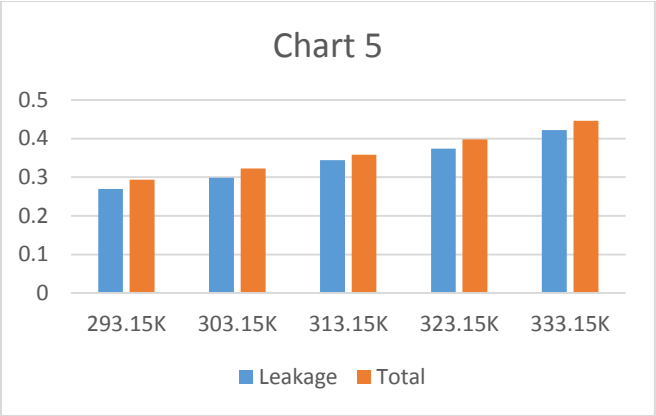
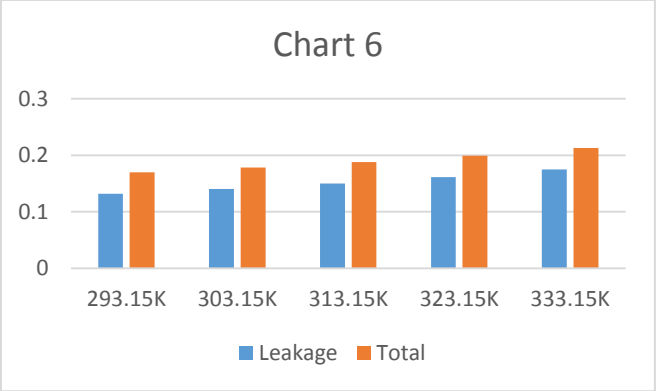


Table 6. Results on 1GHz: (Virtex 4):

Temperature	20°C	30°C	40 °C	50 °C	60 °C
Leakage	0.132	0.140	0.150	0.161	0.175
Total	0.170	0.178	0.188	0.199	0.213
Ambient	17.5°C	27.4 °C	37.2°C	47.1°C	56.9°C

There is 24.5%, 20%, 14.2%, 8 % reduction in leakage power when we scale down temperature from 60 to 20°C, 30°C, 40°C, 50°C respectively as shown in Table 6. There is 69.3%, 51.8%, 34.6%, 17.2% reduction in ambient temperature when we scale down temperature from 60 to 20°C, 30°C, 40°C, 50°C respectively as shown in Table 6 and chart 6.



5. Conclusion

We conclude that UART as a device for serial to parallel conversion best operates at lower values of temperatures since at these values the losses due to the leakage power as well as some other reasons tend to be minimum. At a specified ambient temperature, the observation concludes to the fact that lessening the junction temperature in all, helps to increase the efficiency of the UART. The losses due to the leakage power are minimized and the device undergoes the most optimum utilization when subjected to comparatively lower temperatures. As observed, there is reduction of 36.1% leakage power when changes in the temperature are made from 60°C to 20°C. Correspondingly, there is 29.1%, 20.9%, 11.4% reduction in the leakage power for every 10°C corresponding rise in the temperature for virtex 5 (and so on for every FGPA generation), thereby aiding us to conclude that the value of the junction temperature should be kept as low as possible. This would in turn reduce the losses and therefore would increase the efficiency.

6. Future Scope

For this particular research arena, we have used a FPGA which is a 2-D IC. In the near succeeding times, we could possibly be working on a 3-D IC. This would take the precision framework a step ahead since we would be able to scrutinize the IC in terms of all the three parameters *i.e.*, the length, the breadth as well as the height. Also instead of the UART we could work on the usage of the router protocols and some other networking devices like hubs, bridges, repeaters and many more. Also virtex 7 could be incorporated as a part of the research in the upcoming era. Furthermore, research couldprobably be carried out for the capacitive scaling. FPGA could also possibly be replaced by some newer IC which would then come into existence to obtain better results on power efficiency itself. Relationship could be established between capacitive power and temperature as well. Therefore, it could provide many newer avenues in the field of research.

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