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FPGA-Based Real-Time System for Demodulating FBG Wavelength

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Abstract

In order to detect the wavelength drift of FBG (fiber Bragg grating) sensors, the real-time demodulating system based on tunable F-P filter (TFPF) was built. The optical parts of the demodulation system include broadband optical source, TFPF unit, reference grating model, sensing grating array, and couplers. The electronic parts of the demodulation system consist of AD converting unit, DA converting unit, field programmable gate array (FPGA) unit and human-computer interaction unit. With the high-speed data processing capacity, FPGA was utilized to realize digital logic circuits of the demodulation system. It includes resetting unit, phase locked loop (PLL) unit, driving TFPF unit, detecting keys unit, LCD displaying unit, FIR filtering unit and data calculating unit. The demodulating system has such features as high reliability and speed, instantaneity, and programmability. It can satisfy the requirements of wavelength demodulation of FBG sensors in practical engineering.

Keywords: *fiber Bragg grating, tunable Fabry-Perot filter, demodulation system, field programmable gate array*

1. Introduction

Being compared to other sensors, the fiber Bragg grating (FBG) sensor has many advantages, such as small volume, light weight, high precision, insensitivity to electromagnetic interference and long distance transmission [1-4]. It is the key to utilizing FBG sensors to accurately detect small shift of reflection wavelength. The demodulation method based on tunable F-P filter (TFPF) is widely applied in practical projects at present. It has such advantages as high sensitivity and wide tuning range [5-8]. With the advantage of high-speed parallel data processing capacity, field programmable gate array (FPGA) is widely used to design real-time system [9-10]. In this paper, FPGA was chosen to implement digital logic circuits of the FBG wavelength demodulation system including resetting unit, phase locked loop (PLL) unit, TFPF driving unit, key detection unit, LCD display unit, FIR filter unit and data calculation unit.

2. Design of Real-time Demodulation System

Real-time system based on FPGA for demodulating FBG wavelength is shown in Figure 1. The light emitted by broadband optical source enters TFPF. The light wave, which meets the TFPF transmission condition, will pass TFPF and coupler, and incidence reference gratings and sensing grating array. The sensing gratings are located in measurement environment, and reference gratings are located in non measurement environment. Then the light satisfying Bragg equation of some FBG sensor will be reflected back into the photo detector (PD) via the coupler. The direct digital frequency synthesis (DDS) technology is applied to generate triangular wave signal through FPGA

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device. Then the signals are transformed into analog signal by D/A converter. The frequency and amplitude of the signal can be set by input keys. The TFPF is scanning periodically under driving of the triangular wave. The PD output signal is sampled into FPGA by A/D converter. The wavelength of sensing FBG is demodulated by data calculating component in FPGA. Then the corresponding physical information will be displayed in LCD. In order to improve the precision of the demodulation system, the function between transmission wavelength and driving voltage of TFPF is adjusted in real time with references grating model.

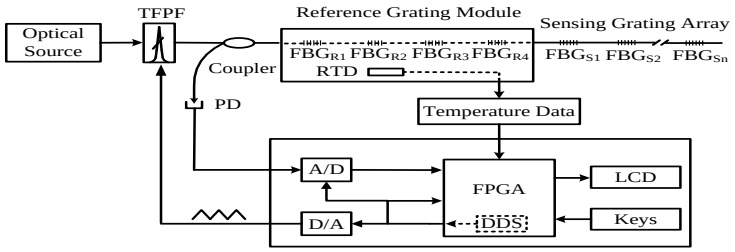

Figure 1. Real-Time System Based FPGA for Demodulating FBG Wavelength

3. Hardware Design

3.1. D/A Conversion Circuits

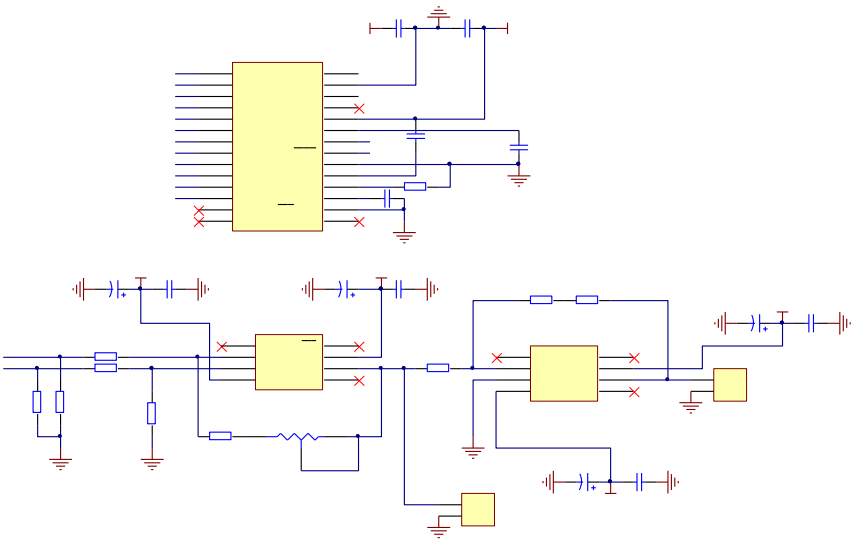

Figure 2. D/A Conversion Circuits

We use a DAC902 conversion chip designed by TI, which is a 12-bit high speed D/A conversion chip, and its conversation frequency can reach up to 165 MHz It has been applied in a variety of fields. It can be powered by a power cell or a portable power system. It runs under 5 V voltage. As shown in Figure 2, a 12-bit data port of DAC902 is linked to corresponding pins of FPGA. Its analog output signal is outputted after two level amplifiers to generate the triangular wave driving signal. The amplitude of output signal can be adjusted with potentiometer in the rage of 0-12 V.

3.2. A/D Conversion Circuits

We use an ADS805 conversion chip designed by TI Corporation, which is a 12-bit A/D conversion chip, and its sampling frequency can reach up to 20 MHz It has a high signal to noise ratio of 68db, and its power dissipation is lower than 300 mW. It runs under 5 V voltages. As the Figure 3 shows, a 12-bit data port of ADS805 is linked to corresponding pins of FPGA. It can process the input signal in the range of 0-5 V. The RLED will shin and the OVA will be set to high potential when input signal exceeds the maximum voltage range.

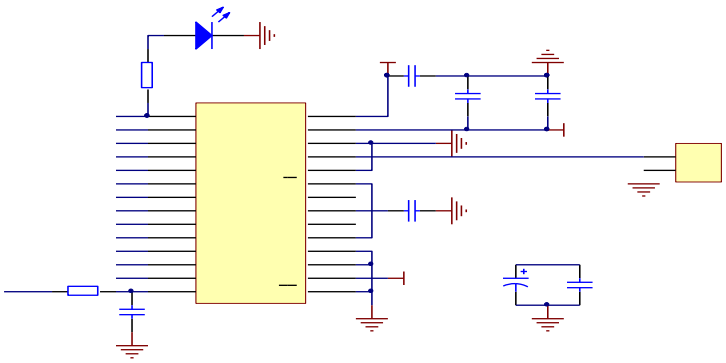

Figure 3. A/D Conversion Circuits

3.3. Human-computer Interaction Unit

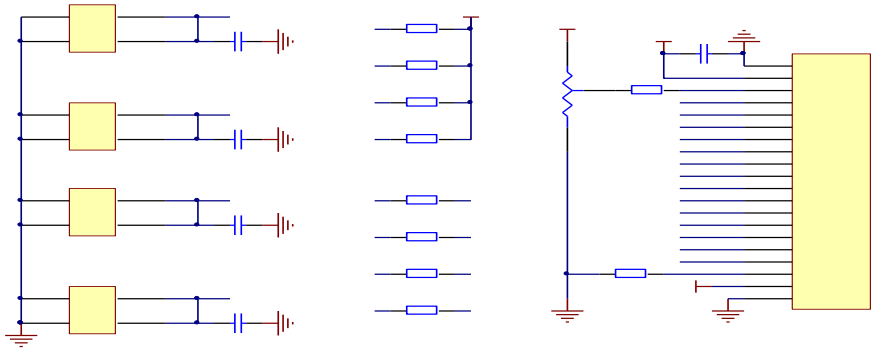

Figure 4. Human-Computer Interaction Circuits

We use the keys to input information, adjust parameters and give orders as a human-computer interaction interface. There are two key detection methods, the direct keyboard and matrix encoding keyboard. In this system, four direct keys were adopted. The LCD module with 128× 64 dot array was employed. It can show Chinese characters and graph. It has the feature of flexible connection and simple command. Circuit diagram of human-computer interaction is showed in Figure 4.

4. Design of System Program

The FPGA unit of the demodulation system is shown in Figure 5. All function modules in FPGA can be reset by resetting unit. The clock of every function unit is produced by PLL unit. The TFPF is driven under triangular wave signal generated by DDS technology. The frequency of the driving signals is set by key detection circuits. The temperature of the resistance temperature detector (RTD) is collected into FPGA by the temperature

collector. The PD output signal is sampled by controlling the A/D converter. The signal collected by A/D converter will be filtered by FIR low-pass filter. In order to improve the operation speed, the fitting data will be cut under threshold. The peak-searching algorithm is applied to the data above the threshold. The data mapping and count is realized through FPGA. The sensing information after demodulating will be outputted by LCD display unit.

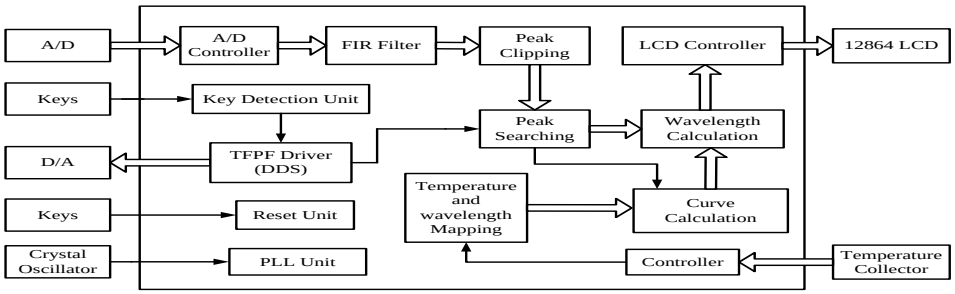

Figure 5. FPGA Unit Of The Demodulation System

4.1. Resetting Unit

The resetting circuits were designed as shown in Figure 6.

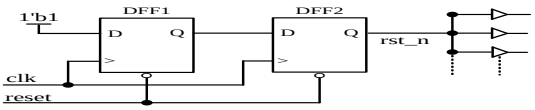

Figure 6. Circuits of Asynchronous Resetting And Synchronous Releasing

It can realize asynchronous resetting and synchronous releasing. When the reset signal is valid, the two registers (DFF1 and DFF2) will be asynchronously reset. Then the output signal rst_n of DFF2 will become into low level. As a result, each register in FPGA will be reset by the signal rst_n. So the resetting unit is asynchronous circuit. After the reset signal is released, the DFF1 will output high level in the clock edge. When the next clock edge comes, the output of DFF2 will also become into high level. Then each register in FPGA is out of the resetting state. Therefore the resetting unit is synchronous releasing circuit. So the resetting circuits designed in this paper can deduce the incidence of metastable state, which often arise in purely asynchronous resetting circuits, and have a high reliability.

4.2. PLL Unit

The clock synchronization between different modules can be realized by PLL unit. The setup time and delay time of the clock signal can also be reduced by PLL unit. So the design of PLL unit with a stable performance is necessary in practical system. The parameters of PLL unit are set in Quartus II as shown in Figure 7. It can set many parameters, such as division coefficient, multiplier factor, phase shift and duty ratio.

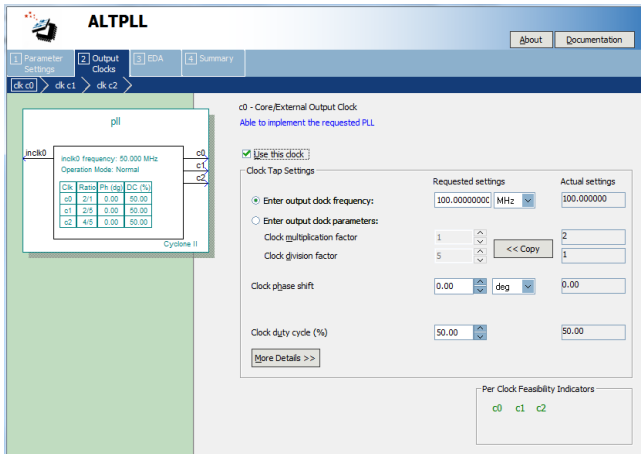

Figure 7. Parameters Configuration of PLL

4.3. Key Detection Unit

The key detection unit is an important function module in demodulation system based on FPGA. The debounce of the keys relates to the interaction and stability of the whole system. The key detection circuits are designed as shown in Figure 8. When the button is pressed, the signals key_in will become to be low level. Then the CNT begins to count until the counting time reached 20 ms. If the signal key_in still keep a low level, it is determined that the key is really pressed. The two-stage trigger synchronization circuit is constituted by DFF1 and DFF2. The rising edge detection function is realized by DFF3 and gate circuit. The rising edge of the signal key_rise shows that the button has been pressed. Not only do the key detection circuits have debounce function, but also deduce the probability to propagate metastable state.

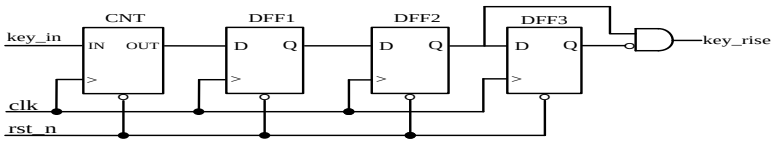

Figure 8. Key Detection Circuits

4.4. TFPF Driving Unit

The DDS technology is applied to realize TFPF diving unit. The top schematic of TFPF driving unit is shown in Figure 9. It mainly includes PLL module, key detection module, driving signal generating module and LCD display module. The frequency of the driving signals can be changed by the input keys. The frequency regulation range of the driving signals is 0~1 MHz, and the minimum resolution is 0.01 Hz.

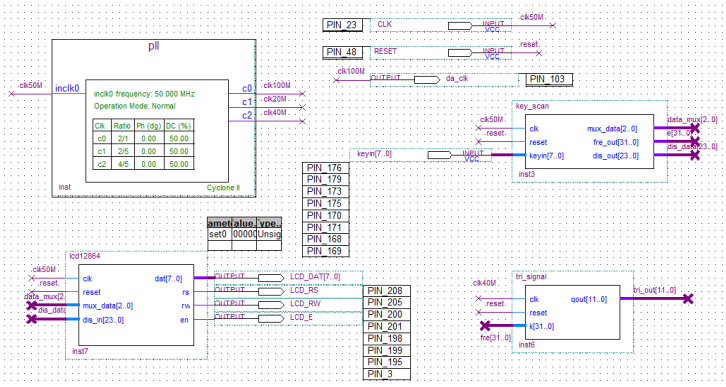

Figure 9. Top Schematic Of Driving Signal Unit

4.5. FIR Filtering Unit

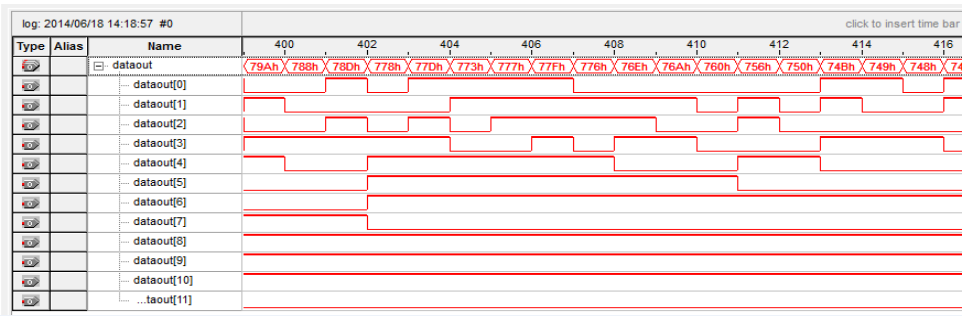

Figure 10. A/D Sampling Signal Captured By Signal tap II

In order to improve the location accuracy of FBG peak, the filtering technology is applied to the collected signals. The Figure 10 shows that the A/D sampling signal captured by signal Tap II. Since the noise in the FBG demodulation system is mainly Gauss white noise, the FIR low-pass filter is designed to process sampled signals. The parameters setting is shown in Figure 11, and the sampling frequency is set to 4 MHz The cut-off frequency of the low-pass filter is 5 KHz and the order is 32.

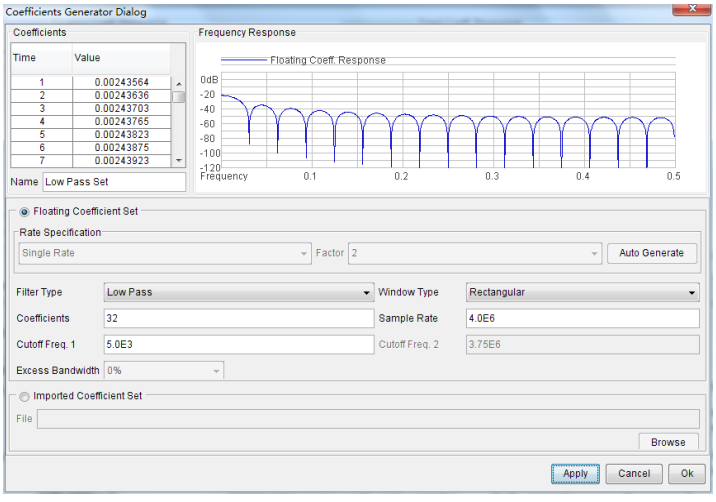

Figure 11. Parameters Configuration of FIR Filter

4.6. Peak Clipping Unit

To process the output signal of PD, the detection of FBG peak occurrence is a main task. It is more effective that the peak-searching algorithm is only applied to the data near the peak position. So the peak clipping unit is designed. In practical application, the data fitting and peak-searching algorithm is applied to the data above the threshold [11]. By this way, the amount of the fitted data is reduced. The operation speed of the demodulation system is also improved.

4.7. LCD Display Unit

The main control chip of LCD adopted in this paper is ST7920. The writing timing diagram of LCD under parallel mode is shown in Figure 12.

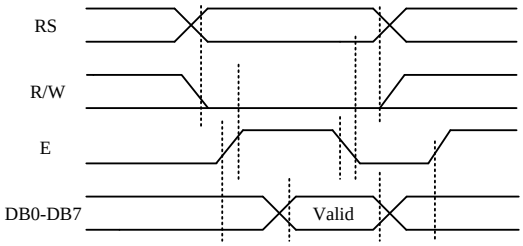

Figure 12. Writing Timing Diagram of LCD

The reading or writing of LCD is controlled by the signal R/W. The low level of the signal R/W executes writing function. The low level of the signal RS is writing instruction. The high level of the signal RS is writing data. When the signal RS and R/W has stabilized, the enable signal E needs to keep high potential for a period. Then the instruction or data is transmitted to the data bus DB0-DB7.

The LCD display unit is controlled by finite state machine. The Figure 13 shows the state diagram for LCD controlling. When the reset signal is valid, LCD display unit is in the state IDLE. Or else the LCD display unit stays at the state INIT, the address register of DDRAM will be reset, and the cursor will also be homing. Then the LCD display unit entries the state DIS_ON, and the whole display function is turned on. The next stare is RI_ADD, the moving direction of cursor is set to be right, and the DDRAM address plus 1 with each moving. Then the LCD display unit steps in the state CLR_DIS, the LCD interface is cleaned up. The next state is ADDRESSS, it is needed to write the address of the display data. At last it is completed to write the display data in the state DATA.

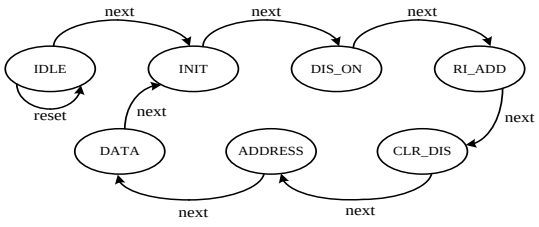

Figure 13. State Diagram for LCD Controlling

5. Experimental Results

The commercial demodulator with the accuracy 1 pm is used as a basis. The demodulation system designed in this paper is applied to demodulate FBG wavelengths. The absolute values of measurement errors are shown in Figure 14. It can be seen from the picture, the maximum error of the demodulation system is 5 pm. The experimental

results show that the FAGA-based real-time demodulation system for FBG wavelength has good measurement accuracy.

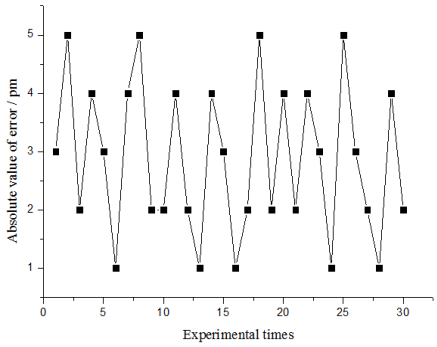

Figure 14. Absolute Values Of Measurement Errors

6. Conclusion

The demodulation technology for FBG wavelength was studied in this paper. The FPGA-based real-time demodulation system for FBG wavelength was built. The optical unit includes the broadband light source, the fiber coupler, the TFPF, the reference gratings module and sensing grating array. The circuit unit is composed of A/D conversion circuit, D/A conversion circuit and human-computer interaction circuit. The signal processing unit was designed based on FPGA. It realizes many functions, such as data acquisition, FIR filtering, peak clipping, peak searching, TFPF driving and data calculation. And it has the advantages of high reliability, real-time, fast and programmable.

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