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High-Gain and Low-Power Power Amplifier for 24-GHz Automotive Radars

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Abstract

This paper presents a high gain and low power 24-GHz power amplifier (PA) for the short range automotive radar. The proposed circuit is implemented using TSMC 0.13-μm RF CMOS (f_T/f_{max}=120/140 GHz) technology, and it is powered by a 1.5-V supply. To improve power gain of the amplifier, it has a 2-stage cascode scheme. This circuit uses transmission lines to reduce total chip size instead of real bulky inductors for input and output impedance matching. The layout techniques for RF (radio frequency) are used to reduce parasitic capacitances at the band of 24 GHz. The proposed RF amplifier has low cost and low power dissipation since it is realized using all CMOS processes. The proposed circuit showed the smallest chip size of 0.12 mm^2, the lowest power dissipation of 44.3 mW and the highest power gain of 24.04 dB as compared to recently reported research results.

Keywords: *RF Power Amplifier, 24-GHz, short range automotive radar, CMOS*

1. Introduction

The rapid growth of wireless communications has resulted in a strong motivation toward developing high performance RF (radio frequency) systems. These systems contain various portable products, automotive collision avoidance radars, wireless local networks, local multi-point distribution service (LMDS), and other ISM band applications. The radar-based ACC (autonomous cruise control) first introduced from Mercedes-Benz in 1999 is widely available in many high and mid class automotive models. This system using 24-GHz radar sensor offers safety functions such as pre-crash sensing and collision. Most of well-known car companies and supplies are already working on the development of the next generation vehicle known as ASV (Advanced Safety Vehicle). The ASV consists of LRR (long range radar) with coverage up to 150 meters and SRR (short range radar) with coverage up to 30 meters. In the last 15 years, silicon-based 24-GHz short-range automotive radars have been investigated both by industry and academia [1-6]. Therefore, next generation radar sensors may well be required to support 24-GHz band for compatibility and lower overall cost [7-14].

In this paper, we proposes a high gain and low power 24-GHz power amplifier (PA) for the automotive radar. The proposed circuit is fabricated using TSMC 0.13-μm RF CMOS (f_T/f_{max}=120/140 GHz) technology. The circuit is powered by a 1.5-V supply. It is designed using a 2-stage cascode scheme to improve power gain of the amplifier.

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Especially to reduce total chip size instead of real bulky inductors transmission lines are used. We used the unique layout technique for 24-GHz RF band to reduce parasitic capacitances.

2. Power Amplifier Analysis

Lower intrinsic gain of transistors makes it more difficult to achieve low power and high gain at very high frequencies, so RF PA design and analysis require several novel techniques.

2.1. Power Requirement in the 24-GHz Band

The Federal Communications Commission (FCC) permits point-to-point wireless communication in the 24~24.25-GHz band, subject to limitations on the transmitted power and directionality of the transmitter. At a distance of 3 m from the transmitter, the maximum electric field permitted is 2.5 V/m. This translates to an average effective isotropically radiated power (EIRP) of 29.7 dBm [13].

The FCC has also opened up 7 GHz of bandwidth from 22 to 29 GHz for vehicular short range radar applications. In this case, there is an average radiated power limit of -41 dBm/MHz which, if used over the entire 7-GHz bandwidth, corresponds to an EIRP of -2.5 dBm. Therefore, an amplifier designed for this application does not need to generate high output power and must instead be designed to have large bandwidth [13].

2.2. Proposed Power Amplifier Scheme

The proposed PA is designed using TSMC 0.13-μm RF CMOS process. The cutoff frequency (f_T) and maximum oscillation frequency (f_{max}) have 120 GHz and 140 GHz, respectively. Important performance parameters of RF PA contain power gain, output-referred 3rd-order intercept point (OIP3) to test linearity, maximum power-added efficiency (PAE) over the whole band of interest, saturated output power (P_{sat}), reverse isolation (S12), input/output return loss (S11/S22), power consumption and chip size.

Figure 1 shows the proposed 24-GHz CMOS power amplifier. The PA consist of common-source stage with inter-stage conjugate matching operating in Class-A mode, and it is powered by a 1.5-V supply. This circuit also has 2-stage cascade structure to achieve higher gain due to the larger output impedance and the alleviated miller capacitance. It uses transmission lines (T-lines) to reduce total chip size instead of real bulky inductors for input and output impedance matching. To input impedance matching, we use T-lines (T_1~T_3) and MIM capacitor (C_1). The inter-stage matching networks are designed using T_4~T_9 and C_5. The T_{10}~T_{12} and C_8 are used for output matching network. To reduce RF noise, power supply noise and EMI, we used decoupling capacitors (C_2～C_4 and C_6～C_7). We designed optimization in width and length of T-lines to supply stable DC power at the drain regions using T_4～T_6 and T_{10}～T_{12}.

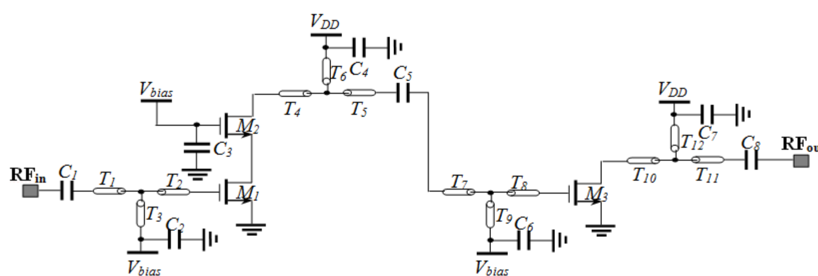

Figure1. 24-GHz CMOS Power Amplifier

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2.3. Layout Issues

The layout technique at the band frequency of 24GHz is very important to reduce parasitic capacitances. Figure 2 shows transistor arrangement layout with folded structure. A parasitic capacitance exists between every two of the four terminals of a MOSFET. Moreover, the value of each of these capacitances may depend on the bias conditions of the transistor, so these capacitances are very critical to degrade performance at high frequencies. Called a “folded” structure, the geometry in Figure 2(b) exhibits substantially less drain junction capacitance than that in Figure 2(a) while providing the same *W/L*.

For the transistor in Figure 2(a), we have

$$C_{DB} = C_{SB} = WEC_j + 2(W + E)C_{jsw}, \tag{2.1}$$

where C_{DB} and C_{SB} are drain-to-bulk and source-to-bulk capacitances, respectively. We typically specify C_j and C_{jsw} as capacitance per unit area and unit length, respectively.

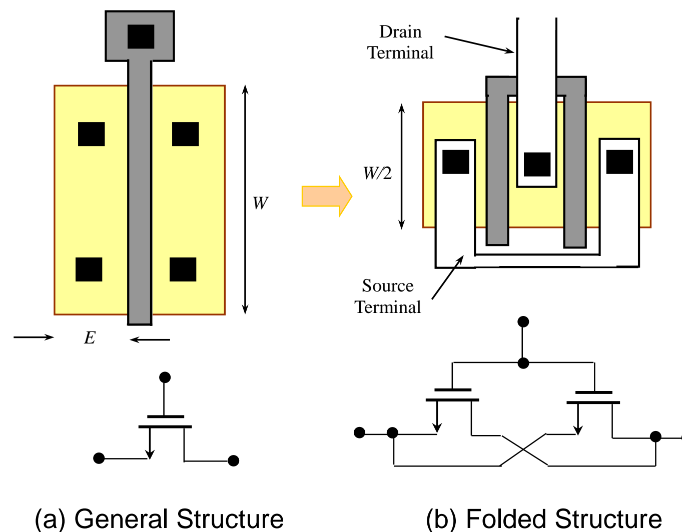
whereas for that in Figure 2(b),

$$C_{DB} = C_{SB} = \frac{W}{2}EC_j + 2\left(\frac{W}{2} + E\right)C_{jsw} \tag{2.2}$$

$$C_{SB} = 2\left[\frac{W}{2}EC_j + 2\left(\frac{W}{2} + E\right)C_{jsw}\right] \tag{2.3}$$

$$= WEC_j + 2(W + 2E)C_{jsw}. \tag{2.4}$$

In the above calculations, we have assumed that the total source or drain perimeter, 2(*W*+*E*), is multiplied by C_{jsw}. In reality, the capacitance of the sidewall facing the channel may be less than that of the other three sidewalls because of channel-stop implant [7]. Nonetheless, we typically assume all four sides have the same unit capacitance. The error resulting from this assumption is negligible because each node in a circuit is connected to a number of other device capacitances as well [7].



(a) General Structure (b) Folded Structure

Figure 2. Transistor Layout with Folded Structure

3. Results

The circuit is simulated using Agilent ADS and full-wave EM analysis is performed for all the passive structures. The speed of the bias mechanism is determined by the bias

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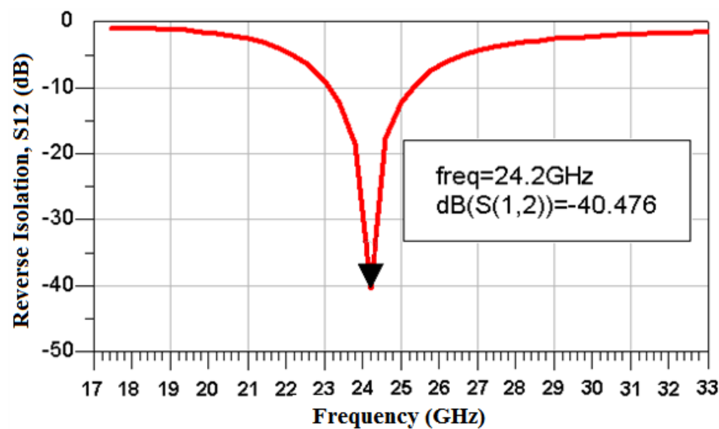
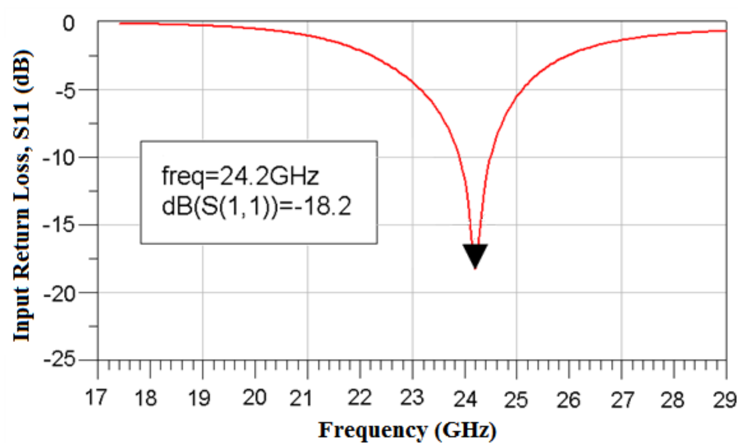
resistor and gate-source parasitic capacitor at the gate of the lower FET, and the settling time is about 4 ns based on the time-domain simulation when the input power of the PA changes from 5 to -5dBm. The amplifier is tested with a power supply of 1.5 V, and the DC current drawn with no RF input signal applied is 29.53 mA.

S-parameters (S11 and S12) of the amplifier in the test are plotted in Figure 3. The S11 indicates how well the input is matched to 50 Ω. The S11 showed excellent value of -40.48 dB in the 24-GHz ISM band, but it was not designed for an input match to 50 Ω for the entire 21~26-GHz band. It should be noted that the requirement on S11 can be relaxed if the amplifier is integrated with the transmitter stages. The S12 indicates that the isolation from the output to the input is also excellent, exceeding –18 dB in the 24 GHz.

Figure 4 shows power gain versus frequency when the amplifier is operating under saturated output power condition driven by a 13.8-dBm input. Maximum output power of 22 dBm (158.5 mW) is achieved at 24GHz, and over 20-dBm output power is available between 21 and 25 GHz. When biased at 14.77 mA (i.e., 50 % of 29.53 mA DC current with no RF signal applied), there is less than 3-dB reduction in output power, despite the transistor trans-conductance g_m being reduced by half for all two stages. As shown in Figure 4, the PA showed high power gain of 24.04 (12.02 x 2) dBm.



(a) Reverse Isolation (S12)



(b) Input Return Loss (S11)

Figure 3. S-parameters (S11 and S12)

Figures 5(a) and 5(b) show power-added efficiency (PAE) and saturated output power (P_{sat}) versus input power when the amplifier is operating under saturated output power

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condition driven by a 13.8-dBm input. At 24 GHz, the final gain stage of the power amplifier achieves a maximum output power density (power per source area) of 2 mW/μm^2. The PAE exceeds 6 % between 22 and 25 GHz. The amplifier has over 22-dB power gain from 22 to 25 GHz with 3-dB gain flatness. Over 15-dB gain at maximum output power level facilitates integration of the amplifier in a transceiver as fewer pre-driver stages are required. When biased at 14.77 mA (i.e., 50 % of 29.53 mA DC current with no RF signal applied), there is less than 3-dB reduction in output power and slightly power PAE, despite the transistor trans-conductance g_m being reduced by half for all two stages. As shown in Figures 5(a) and 5(b), the PA showed high saturated output power of 21.5 dBm and maximum PAE of 7.1 %, respectively.

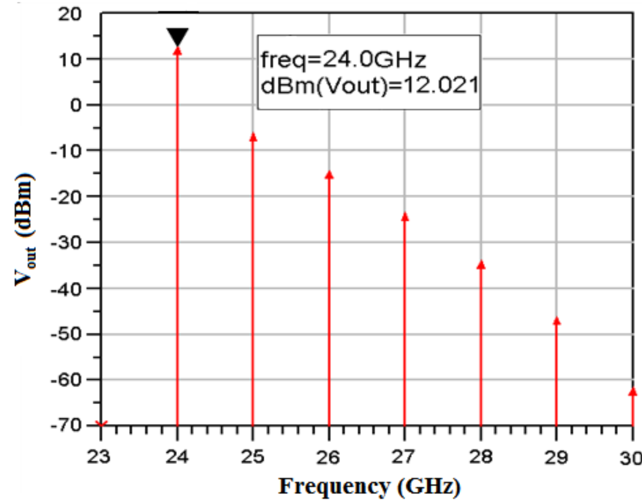
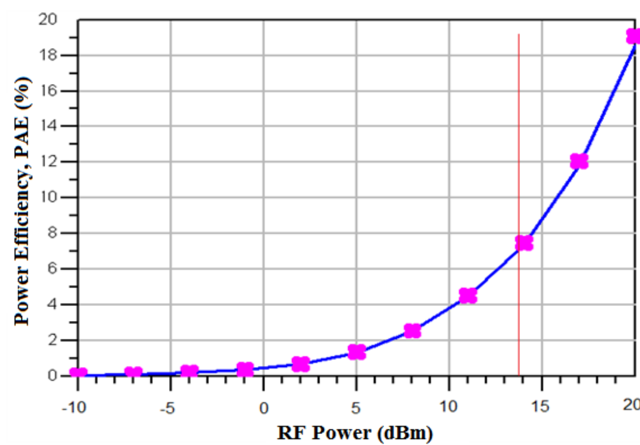


Figure 4. Output Power Gain versus Frequency



(a) Power-added Efficiency

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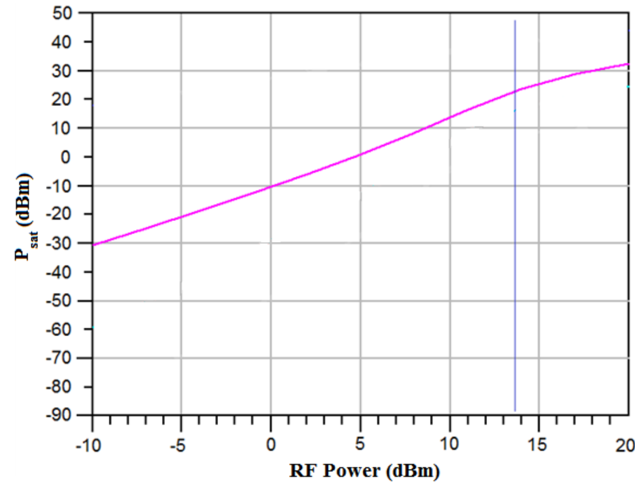

(b) Saturated Output Power

Figure 5. Power-added Efficiency and Saturated Output Power versus Input Power

Table 1 shows comparison results to recently reported 24-GHz power amplifiers. To test the linearity of the amplifier, a two-tone test was performed with a tone spacing of 100 MHz. As shown in Table 1, the OIP3 is good linearity of 16.5 dBm. The proposed circuit showed highest power gain of 24.04 dB, the highest saturated power gain of 21.5 dBm, the lowest input/output return loss of -18.2 dB/-20.1 dB, the lowest power dissipation of 44.3 mW, and the smallest chip size of 0.12 mm^2 as compared to recently reported research results in [11-14].

Table 1. Comparison to Recently Reported 24-GHz Power Amplifiers

Reference	[11]	[12]	[13]	[14]	This work
Frequency (GHz)	24	22	24	24	24
Technology (μm)	0.18	0.18	0.18	0.2	0.13
OIP3 (dBm)	7	15.4	14	**23**	16.5
Power Gain (dB)	22.8	11.9	7	19	**24.04**
P_{sat} (dBm)	15.9	17.4	14.5	15	**21.5**
Maximum PAE (%)	**14.6**	12	6.5	13	7.1
S11 (dB)	-14.3	-8	-6.9	-12.4	**-18.2**
S22 (dB)	-17	-10	-16	-	**-20.1**
S12 (dB)	**-64**	-	-40	-10.5	-40.48
Power Consumption (mW)	163.8	108	280	939	**44.3**
Chip Size (mm^2)	0.84	0.4	1.26	6.003	**0.12**

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4. Conclusions

This paper proposed 24-GHz power amplifier with a high gain, low power and low chip size for the short range automotive radar. The proposed circuit was fabricated using TSMC 0.13-μm RF CMOS (f_T/f_{max}=120/140 GHz) process, and it was powered by a 1.5-V supply. To reduce total chip area and parasitic capacitances, we used transmission line matching and RF layout technique, respectively. The proposed CMOS power amplifier showed the smallest chip size of 0.12 mm^2, the lowest power dissipation of 44.3 mW and the highest power gain of 24.04 dB as compared to recently reported research results.

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