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Energy Efficient Traffic Light Controller Design on 28nm FGPA

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Abstract

In this work, our focus is on study and analysis of power and junction temperature at different temperatures and at different capacitance values. Kintex7 is 28-nm FPGA on which we implement our circuit to re-assure power reduction and reduction in junction temperature in sequential circuit. Varying the values of capacitance and temperature enhance the efficiency of the Energy Efficient Traffic Light Controller design. This paper basically deals with FSM (Finite State Machine) and is implemented on FPGA. FGPA is preferred because of its high speed and is inexpensive. Traffic lights are beneficial in managing the traffic, reducing accidents rate, relaxing traffic cop's job, minimizing fuel consumption and emission and save time. The performance of our energy efficient traffic lights is evaluated and tested through simulations on Xilinx software development kit. For 2.4GHz operating frequency, there is 47.71% reduction in total power dissipation, 69.94% reduction in IOs power dissipation, and 0.78% reduction in junction temperature when we use 28nm FPGA and temperature is 25 degree Celsius and capacitance is scaled down from 100pF to 20pF. For 10GHz operating frequency, there is 54.81% reduction in total power dissipation, 70.11% reduction in IOs power dissipation, 3.52% reduction in leakage power dissipation and 1.92% reduction in junction temperature when we use 28nm FPGA and temperature is 50 degree Celsius and capacitance is scaled down from 100pF to 20pF.

Keywords: *FSM, Traffic Light Controller, Energy Efficient, FPGA*

1. Introduction

Traffic lights also called stop lights are most commonly found at intersections of roads. Nowadays Traffic lights are essential to manage a huge traffic. Traffic lights are followed by using 3 standard colors as shown in Figure 1.

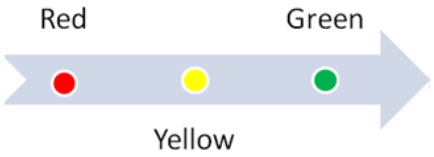

Figure 1. Colors in Traffic Light Management

Whenever we are out from our place we face traffic lights. These traffic lights are beneficial in managing the traffic, reducing accidents rate, relaxing traffic cop's job, minimizing fuel consumption and emission and save time. Earlier when there were no traffic lights the whole management of traffic was done manually and this was an inefficient method. Traffic rules are meant to be followed to avoid collisions and other hazards. Traffic lights can be implemented using microcontroller but using FPGA is advantageous over microcontroller because of its high speed, number of input/output and

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using microcontroller is more expensive than FPGA[1].The main focus is for switching the traffic lights according to vehicle density and reducing the traffic congestion on roads which will help to lower down the number of accidents [2].In our research work we have used Xilinx ISE and have used finite state machine (FSM) concept and designed an automatic traffic lights which keeps on changing among three states according to the logic given to it. Vehicle detection is used for monitoring and surveillance of traffic and this is done by using concept of finite state machine [3]. Traffic lights can also be communicated with cars to dynamically operate the lights so as to reduce fuel consumption, traffic jams and etc. [4].In reference [4], the code is written in Python and is connected with traffic simulator to manage the traffic. This paper basically deals with FSM and is implemented on FPGA. This is energy efficient traffic light controller and is tested on Kintex7 which is 28nm FPGA. We have done its power analysis and as well as thermal analysis. The power performance of energy efficient traffic controller is based on Verilog. The performance is evaluated by performing simulations on a magnetic recording channel [5].The performance of our energy efficient traffic lights is evaluated and tested through simulations on Xilinx software development kit.

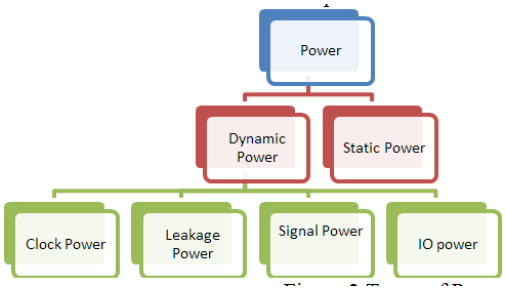

Figure 2. Types of Power

Dynamic power or total on-state power is further classified as Clock power, Leakage power, Signal power, IO power. The operating temperatures taken for the thermal analysis are 25 degree Celsius and 50 degree Celsius. Thermal Aware design is current research area. There is already work is going on in thermal aware design of FIR Filter [6], thermal aware Key Generator in Green Communication [7] and design of thermal aware ROM [8]. Power is of 2 types: Dynamic power (ON state power) and Static power (OFF state power).

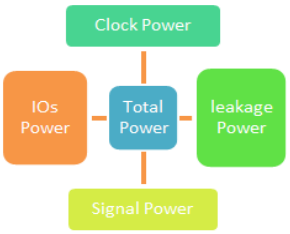

Figure 3. Dynamic Power's Classification

Along with thermal aware design, our prime focus is on capacitance scaling [9-10]. Our traffic light controller as shown in Figures 4-5, is a Finite State Machine (FSM) of 3-states (Red, Yellow and Green) implementation on FPGA.

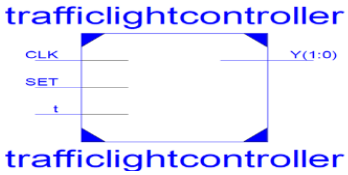

Figure 4. Symbol of Traffic Light Controller

As shown in Figure 4, RTL schematic is using BUFGP as global clock buffer, D Flip-Flop and Look up Table (LUTs), Input buffer (IBUF) and Output buffer (OBUF).

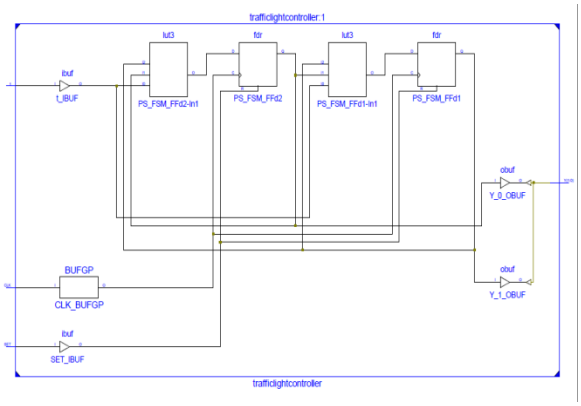

Figure 5. Schematic of Traffic Light Controller

2. Power and Junction Temperature Anaysis

A. IO Power and Thermal Analysis for 1GHz Frequency

Table 1. Power Analysis and Junction Temperature Analysis at 25oCelsius

C in pF	Total Power	Clock Power	Signal Power	IOs Power	Leakage power
20	0.106	0.006	0	0.024	0.076
40	0.120	0.006	0	0.038	0.076
60	0.135	0.006	0	0.052	0.076
80	0.149	0.006	0	0.066	0.076
100	0.163	0.006	0	0.080	0.076

There is 34.96% reduction in total power dissipation, No reduction in clock and signal power dissipation, 70% reduction in IOs power dissipation, and 0% reduction in leakage power,when we use 28nm FPGA and temperature is 25 degree Celsiusand capacitance is scaled down from 100pF to 20pF as shown in Table 1 and Figure 6.

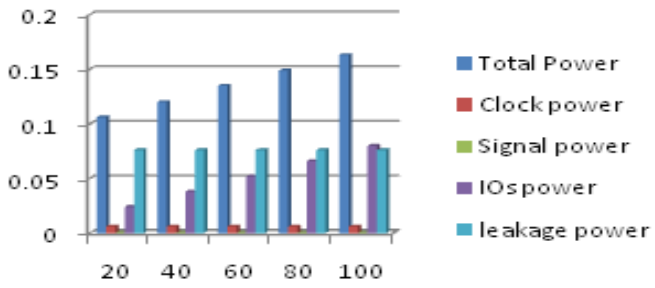

Figure 6. Power Dissipation at 25oCelsius Temperature for 1GHz

Table 2. Power Analysis and Junction Temperature Analysis at 50oCelsius

C in pF	Total Power	Clock Power	Signal Power	IOs Power	Leakage Power
20	0.191	0.006	0	0.024	0.161
40	0.205	0.006	0	0.038	0.161
60	0.220	0.006	0	0.052	0.161
80	0.234	0.006	0	0.066	0.161
100	0.248	0.006	0	0.080	0.161

There is 22.98% reduction in total power dissipation, 0% reduction in clock and signal power dissipation, 70% reduction in IOs power dissipation, and 0% reduction in leakage power, when we use 28nm FPGA and temperature is50 degree Celsius and capacitance is scaled down from 100pF to 20pF as shown in Table 2 and Figure 7.

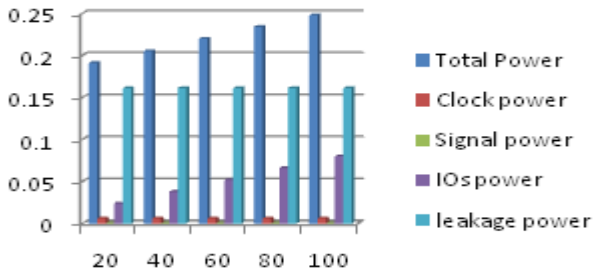

Figure 7. Power Dissipation at 50oCelsius Temperature for 1GHz

There is 0.19% reduction in junction temperature for 50 degree Celsius and 0.3% reduction in junction temperature for 25 degree Celsius and capacitance is scaled down from 100pF to 20pF as shown in Table 3 and Figure 8.

Table 3. Junction Temperature Analysis at Various Capacitances for 1GHz

	20pF	40pF	60pF	80pF	100Pf
25°C	25.2	25.2	25.3	25.3	25.3
50°C	50.4	50.4	50.4	50.4	50.5

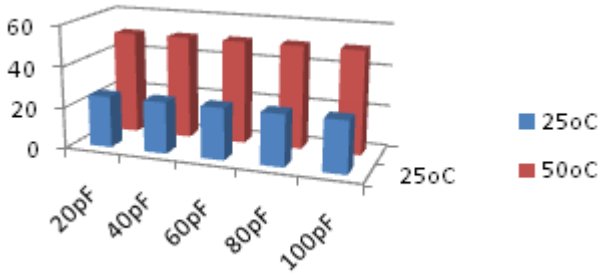

Figure 8. Junction Temperature Analysis for 1GHz at Various Capacitances

B. IO Power and Thermal Analysis for 10GHz Frequency

Table 4. Power Analysis and Junction Temperature Analysis at 25oCelsius

C in pF	Total Power	Clock power	Signal power	IOs power	Leakage Power
20	0.382	0.063	0.002	0.240	0.077
40	0.523	0.063	0.002	0.301	0.077

60	0.665	0.063	0.002	0.522	0.078
80	0.806	0.063	0.002	0.663	0.078
100	0.945	0.063	0.002	0.803	0.079

There is 59.57% reduction in total power dissipation, 0% reduction in clock power dissipation, 0% reduction in signal power dissipation, 70.11% reduction in IOs power dissipation, and 2.53% reduction in leakage power dissipation, when we use 28nm FPGA and temperature is 25 degree Celsius and capacitance is scaled down from 100pF to 20pF as shown in Table 4 and Figure 9.

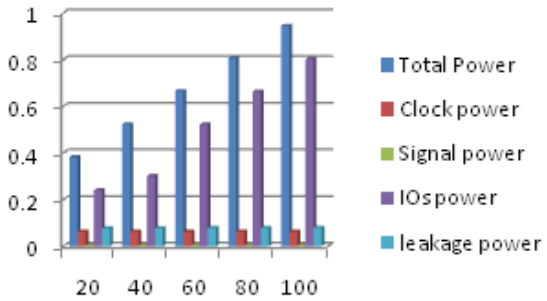

Figure 9. Power Dissipation at 25oCelsius Temperature for 10GHz

Table 5. Power Analysis and Junction Temperature Analysis at 50oCelsius

C in pF	Total Power	Clock Power	Signal Power	IOs Power	Leakage Power
20	0.469	0.063	0.002	0.240	0.164
40	0.611	0.063	0.002	0.301	0.165
60	0.754	0.063	0.002	0.522	0.167
80	0.896	0.063	0.002	0.663	0.168
100	1.038	0.063	0.002	0.803	0.170

There is 54.81% reduction in total power dissipation, 0% reduction in clock and signal power dissipation, 70.11% reduction in IOs power, 3.52% reduction in leakage power dissipation, when we use 28nm FPGA and temperature is 50 degree Celsius and capacitance is scaled down from 100pF to 20pF as shown in Table 5 and Figure 10.

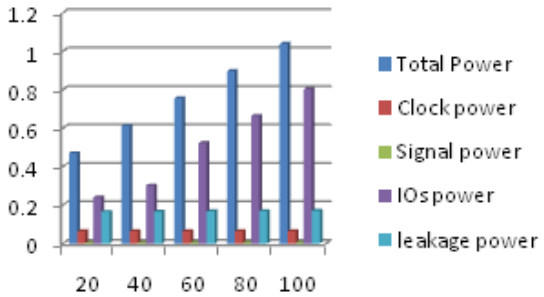

Figure 10. Power Dissipation at 50oCelsius Temperature for 10GHz

C. IO Power and Thermal Analysis for 6 MHz Frequency

Table 6. Power Analysis and Junction Temperature Analysis at 25oCelsius

C in pF	Total Power	Clock Power	Signal Power	IOs Power	Leakage Power
20	0.076	0	0	0	0.076
40	0.076	0	0	0	0.076

60	0.076	0	0	0	0.076
80	0.076	0	0	0	0.076
100	0.076	0	0	0	0.076

There is 0% reduction in total power dissipation, clock power dissipation, signal power dissipation, IOs power dissipation, leakage power dissipation and also in junction temperature when we use 28nm FPGA and temperature is 25 degree Celsius and capacitance is scaled down from 100pF to 20pF as shown in Table 6 and Figure 11.

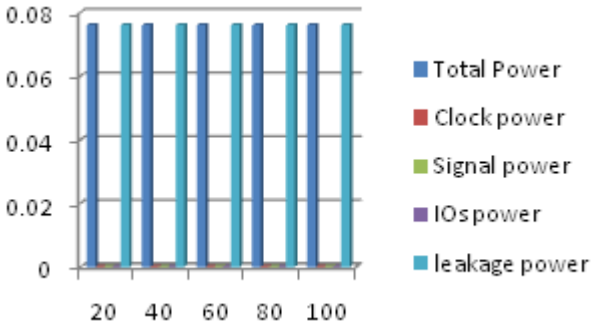

Figure 11. Power Dissipation at 25oCelsius Temperature for 6MHz

Table 7. Power Analysis and Junction Temperature Analysis at 50oCelsius

C in pF	Total Power	Clock Power	Signal Power	IOs Power	Leakage Power
20	0.161	0	0	0	0.160
40	0.161	0	0	0	0.160
60	0.161	0	0	0	0.160
80	0.161	0	0	0	0.160
100	0.161	0	0	0	0.160

There is 0% reduction in total power dissipation, clock power dissipation, signal power dissipation, IOs power dissipation, and also in leakage power dissipation along with 0% reduction in junction temperature, when we use 28nm FPGA and temperature is 25 degree Celsius and capacitance is scaled down from 100pF to 20pF as shown in Table 7 and Figure 12.

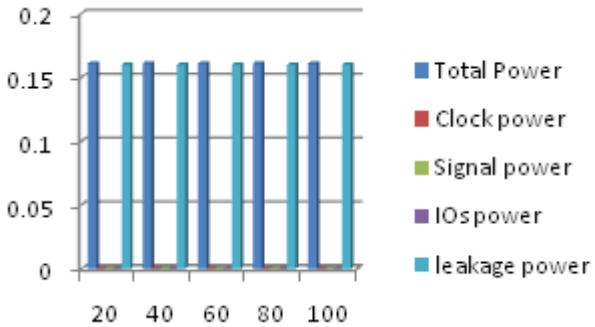

Figure 12. Power Dissipation at 50oCelsius Temperature for 6MHz

Table 8. Junction Temperature Analysis at Various Capacitances for 6MHz

	20pF	40pF	60pF	80pF	100pF
25°C	25.1	25.1	25.1	25.1	25.1

50°C	50.3	50.3	50.3	50.3	50.3

There is 0% reduction in junction temperature, when we use 28nm FPGA and temperature is 25 degree and 50 degree Celsius and capacitance is scaled down from 100pF to 20pF as shown in Table 8 and Figure 13.

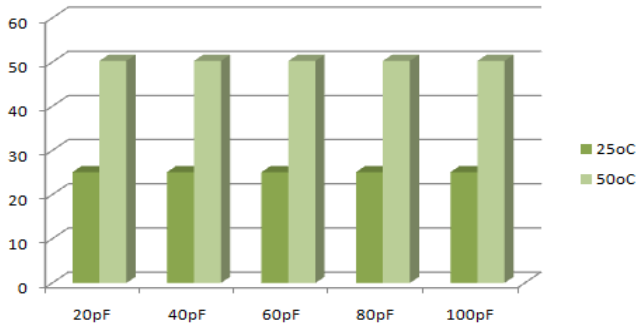

Figure 13. Junction Temperature Analysis for 6MHz at Various Capacitances

D. IO Power and Thermal Analysis for 2.4 GHz Frequency

Table 9. Power Analysis and Junction Temperature Analysis at 25oCelsius

C in pF	Total Power	Clock Power	Signal Power	IOs Power	Leakage Power
20	0.149	0.015	0.001	0.058	0.076
40	0.183	0.015	0.001	0.091	0.076
60	0.217	0.015	0.001	0.125	0.076
80	0.251	0.015	0.001	0.159	0.076
100	0.285	0.015	0.001	0.193	0.076

There is 47.71% reduction in total power dissipation, 0% reduction in clock& signal power dissipation, 69.94% reduction in IOs power dissipation, and % reduction in leakage power dissipation,when use 28nm FPGA and temperature is 25 degree Celsius and capacitance is scaled down from 100pF to 20pF as shown in Table 9 and Figure 14.

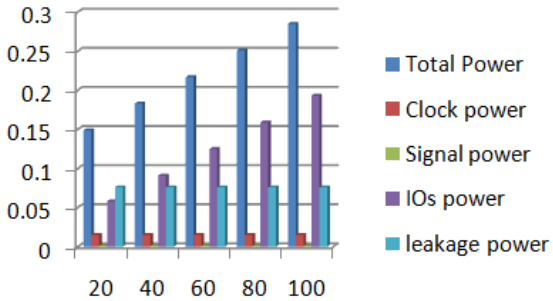

Figure 14. Power Dissipation at 25oCelsius Temperature for 2400MHz

Table 10. Power Analysis and Junction Temperature Analysis at 50oCelsius

C in pF	Total Power	Clock power	Signal power	IOs power	Leakage power
20	0.234	0.015	0.001	0.058	0.161
40	0.269	0.015	0.001	0.091	0.162

60	0.303	0.015	0.001	0.125	0.162
80	0.337	0.015	0.001	0.159	0.162
100	0.371	0.015	0.001	0.193	0.163

There is 36.92% reduction in total power, 0% reduction in clock power and signal power dissipation, 69.94% reduction in IOs power dissipation, and 1.22% reduction in leakage power, when we use 28nm FPGA and temperature is 25 degree Celsius and capacitance is scaled down from 100pF to 20pF as shown in Table 10 and Figure 15.

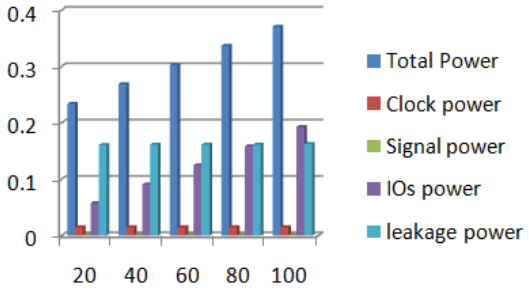

Figure 15. Power Dissipation at 50oCelsius Temperature for 2400MHz

Table 11. Junction Temperature at various Capacitances for 2400MHz

	20pF	40pF	60pF	80pF	100pF
25°C	25.3	25.3	25.4	25.5	25.5
50°C	50.4	50.5	50.6	50.6	50.7

There is 0.59% reduction in junction temperature when we use 28nm FPGA and temperature is 25 degree Celsius and capacitance is scaled down from 100pF to 20pF as shown in Table 11 and Figure 16.

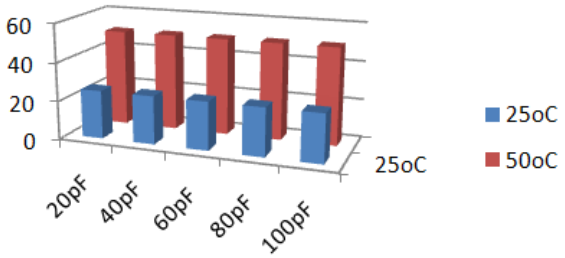

Figure 16. Junction Temperature for 2400MHz at Various Capacitances

E. IO Power and Thermal Analysis for 1.5 GHz Frequency

Table 12. Power Analysis and Junction Temperature Analysis at 25oCelsius

C in pF	Total Power	Clock Power	Signal Power	IOs Power	Leakage Power
20	0.122	0.009	0.001	0.036	0.076
40	0.143	0.009	0.001	0.057	0.076
60	0.164	0.009	0.001	0.078	0.076
80	0.185	0.009	0.001	0.099	0.076
100	0.206	0.009	0.001	0.121	0.076

There is 40.77% reduction in total power dissipation, 0% reduction in clock & signal power dissipation, 70.24% reduction in IOs power dissipation, and 0% reduction in leakage power, when we use 28nm FPGA and temperature is 25 degree Celsius and capacitance is scaled down from 100pF to 20pF as shown in Table 12 and Figure 17.

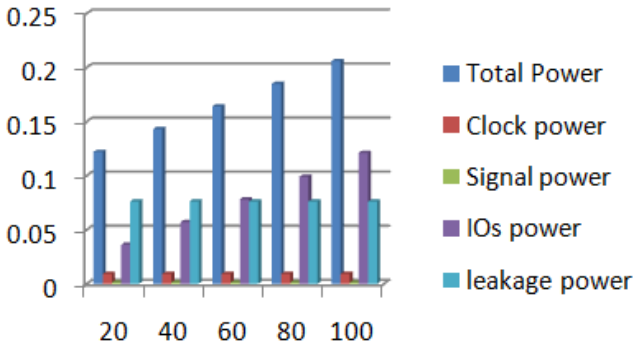

Figure 17. Power Dissipation at 25oCelsius Temperature for 1500MHz

Table 13. Power Analysis and Junction Temperature Analysis at 50oCelsius

C in pF	Total Power	Clock Power	Signal Power	IOs Power	Leakage Power
20	0.207	0.009	0.001	0.036	0.161
40	0.228	0.009	0.001	0.057	0.161
60	0.249	0.009	0.001	0.078	0.161
80	0.271	0.009	0.001	0.099	0.162
100	1.292	0.009	0.001	0.121	0.162

There is 83.97% reduction in total power dissipation, 0% reduction in clock power dissipation, 0% reduction in signal power dissipation, 70.24% reduction in IOs power dissipation, and 0.61% reduction in leakage power dissipation, when we use 28nm FPGA and temperature is 25 degree Celsius and capacitance is scaled down from 100pF to 20pF as shown in Table 13 and Figure 18.

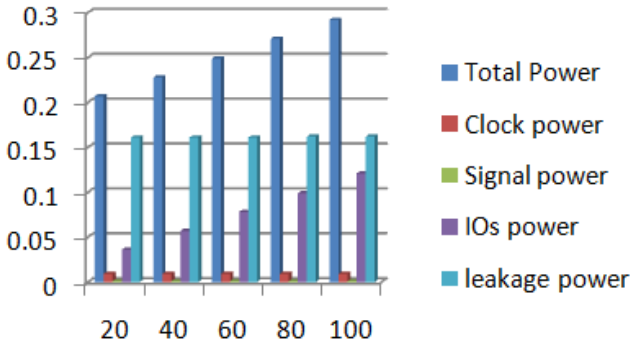

Figure 18. Power Dissipation at 50oCelsius Temperature for 1500MHz

Table 14. Junction Temperature at various capacitances for 1500MHz

	20pF	40pF	60pF	80pF	100pF
25°C	25.2	25.3	25.3	25.3	25.4
50°C	50.4	50.4	50.5	50.5	50.5

There is 0.19% reduction in junction temperature when we use 28nm FPGA and temperature is 25 degree Celsius and capacitance is scaled down from 100pF to 20pF as shown in Table 14 and Figure 19.

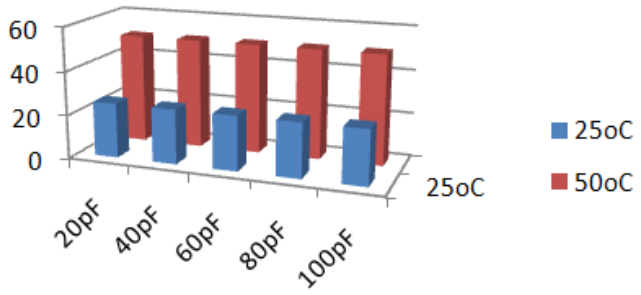

Figure 19. Junction Temperature for 1500MHz at various Capacitances

3. Conclusion

Our traffic light controller is the most energy efficient using capacitance scaling because power is directly proportional to capacitance. For 2.4GHz operating frequency, there is 47.71% reduction in total power dissipation, 69.94% reduction in IOs power dissipation, and 0.78% reduction in junction temperature, when we use 28nm FPGA and temperature is 25 degree Celsius and capacitance is scaled down from 100pF to 20pF. For 10GHz operating frequency, there is 54.81% reduction in total power dissipation, 70.11% reduction in IOs power dissipation, 3.52% reduction in leakage power dissipation and 1.92% reduction in junction temperature, when we use 28nm FPGA and temperature is 50 degree Celsius and capacitance is scaled down from 100pF to 20pF. Thermal stability of our design is tested for different ambient temperature of 25^{o}C and 50^{o}C.

4. Future Scope

The future scope of Energy efficient automatic traffic light controller design is we can check the speed of vehicles with the help of special sensor. We can also include surveillance system and video monitoring to check whether the rules and regulations are followed or not. We have focused on only 1 FPGA design family that is Kintex7. Others can work on automotive Artix7, automotive Coolrunner2, automotive Spartan, automotive Spartan-3A DSP, automotive Spartan 3A, automotive Spartan 3E, automotive Spartan6, Spartan3, Spartan3E, Spartan low power, Kintex7 low voltage, Virtex5, Virtex4, Virtex6 and many others. We have taken a very short temperature so one can increases temperature range as much as they want same is with capacitance it can be varied and tested to achieve more efficient automatic traffic lights.

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