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Programmable RF Built-In Self-Test Circuit for 5GHz Wireless LAN

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Abstract

This paper proposes a new programmable RF Built-In Self-Test (BIST) circuit for 5GHz Wireless LAN. It is fabricated using 0.18-μm SiGe technology. This circuit is useful for testability of GHz-band RF IC devices in a complete RF transceiver environment. The proposed circuit helps it to provide DC output voltages and accurate phase difference. It contains two peak detectors and a phase detector. The proposed circuit showed excellent performance.

Keywords: *RF Built-In Self-Test (BIST), Wireless LAN, peak detector, phase detector*

1. Introduction

RF integrated circuits have grown their usability providing high density, high speed and low-cost RF systems. To realize these recent trends, system-on-a-chip (SoC) has become a suitable solution in recent RF IC industry. However, the suitable test technique to reduce test cost for SoC still remains to be the major bottleneck to make affordable wireless systems. To solve this problem, the test technique using BIST (Built-In Self-Test) circuit in the RF and mixed-signal domain is applied as a suitable test structure on SoC [1-6].

To design an effective RF BIST structure, proper identifications of parametric variations in RF system play an integral part of the design. Analog systems have only a few inputs and outputs, and their internal states exhibit low time constants compared to digital circuits [4-6]. To test point-to-point transceiver, loop-back technique using spectral signature analysis is generally used with lower effort and very small test overhead. However, this test approach has disadvantages such as lower test coverage due to the fact that the complete transceiver is tested as a whole and the need of an additional DSP due to the higher complexity of the test signature generation.

In this paper, a new low-cost alternative approach for SoC testing to adjust catastrophic defects is proposed. The alternative method utilizes BIST circuit for RF circuit as a typical RF front-end chip. The circuit involves band-gap reference, test amplifier, two peak detectors and a phase detector. The RF BIST circuit helps it to provide DC output voltages and accurate phase difference, hence, making the test circuit automatic.

2. Circuit Design and Analysis

The proposed BIST circuit is shown in Figure 1. It is designed using 0.18 μm SiGe technology. It contains band-gap reference for bias stage, test amplifier (TA) with programmable capacitor banks (C_B), peak detector (PD2) and phase detector (PHD). The

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other peak detector circuit (PD1) is also a part of the BIST circuit and it has the same topology as the PD2 circuit shown in Figure 1. These RF peak detectors are used for converting from RF signal to DC voltage. The bias stage utilizes band-gap reference circuit for a low supply voltage and low power dissipation [7-9]. It controls the base current of the test amplifier. It is designed to provide stable band-gap reference voltage for the temperature drift and power supply variation. The test amplifier is used for amplifying and observing variations of input impedance of GHz-band RF circuits due to their catastrophic faults or parametric variations. The simultaneous matching for input and output impedances including the effect of the load impedance is considered to reduce RF signal loss. The inductor (L_{c01}) is used for input and output impedances matching. The capacitors (C_{c02} and C_{c03}) are used for output impedance matching. The bias resistors (R_{05} and R_{06}) shown in Fig. 1 are used to keep transistor Q_{04} in the active region so that the transistor acts as a rectifier. The capacitor C_{04} is used for DC blocking of DC bias voltage across bias resistors. We selected R_{07} and C_{05} with large values to reduce the output ripple voltage. The variable capacitor, C_B, is used for self-calibrating parametric variations with RF circuits.

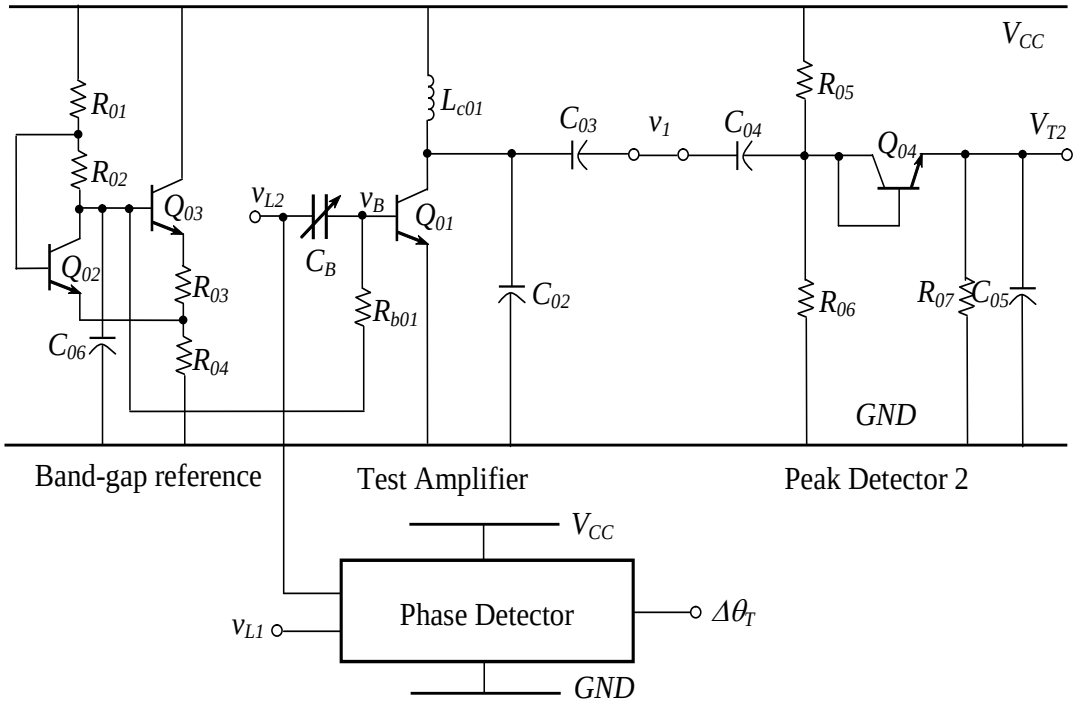

Figure 1. Schematic Diagram of Programmable RF BIST

The BIST circuit can handle fine parametric variations by adjusting the value of the capacitance (C_B) as shown in Figure 2. It has 3-bit programmable capacitor banks for self-calibrating. The capacitor banks are controlled by using digital signals, ($D_1D_2D_3$), from the DPU. The input data streams have different eight levels of from ($D_3D_2D_1$) = (001) to (111). It is powered by 1.8volts supply voltage. The transistors M_1, M_2 and M_3 are designed for operating in deep triode region so that they exhibit no dc shift between the input and output voltages.

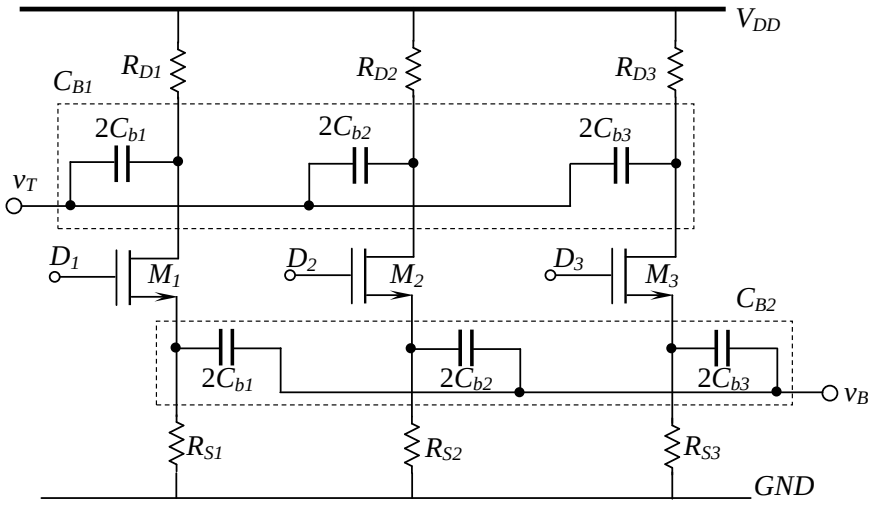

Figure 2. Schematic Diagram of Capacitor Banks, C_B

Figure 3 shows schematic diagram of phase detector. We used an RF phase detector to detect phase difference ($\Delta\theta_T$) and control imaginary factors of RF circuit parameters. It provides the output minimum voltage of 30mV for phase difference of 180°, and the output maximum voltage of 1.8V for phase difference of 0°. When $\theta_2 = \theta_1 \pm 90°$, phase center point is 900mV. The output current driving for source/sink condition is 10mA, and slew rate is 5V/ns. The small signal envelope bandwidth is 50MHz, and the response time for 15° change condition in 10%~90% is 10ns. The bias stage utilizes a band-gap reference circuit for the low supply voltage and low power dissipation.

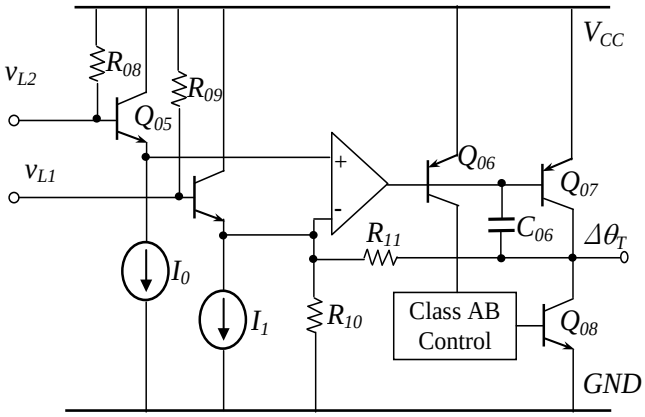

Figure 3. Schematic Diagram of Phase Detector

Figure 4 shows high-frequency small-signal model for the test amplifier and peak detector. Simultaneous matching is performed, and the effect of the load impedance is taken into account in the simplified small-signal bipolar junction transistor (BJT) and inductor models shown in Figure 4 [7-9]. To verify and compare the accuracy of the designed BIST circuit, accurate modeling is performed. The transistor is replaced with hybrid-π model, and the inductor is replaced with series resistance *R* and its inductance *L*. From an analytical analysis of BIST circuit, the input impedance, voltage gain and transfer functions are obtained. The output resistance r_{o01} of the transistor Q_{01} due to its high value is neglected.

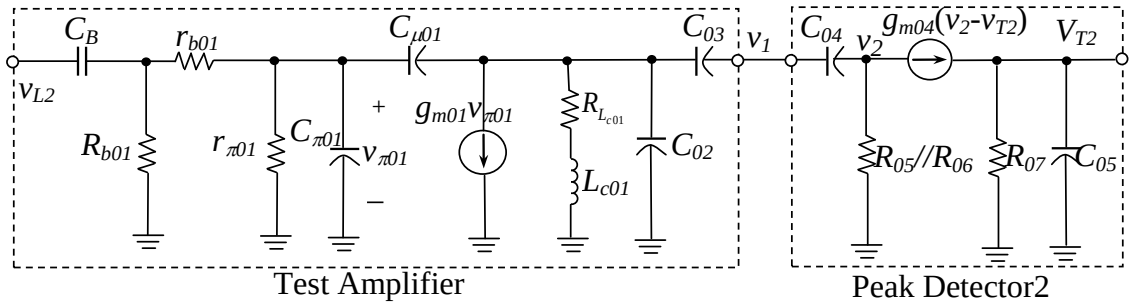

Figure 4. High-frequency Small-signal Model for BIST Circuit

Let's consider Figure 5 with the source (V_{in}) forming part of a network analyzer with a matched load (Z_L = 50Ω) at port 2 to measure transfer function (S_{21}) for the peak detectors (PD1 and PD2). S_{21} can be found by applying an incident wave at port 1, V_1^+, and measuring the out-coming wave at port 2, V_2^-. This is equivalent to the transmission coefficient from port 1 to port 2. Since S_{21} is a measurement of the gain at the network analyzer output, the transfer function $H(f)$ can be derived to be as expressed in Equation (1).

$$H(f) = S_{21} = \left.\frac{V_2^-}{V_1^+}\right|_{V_2^+=0} . \tag{1}$$

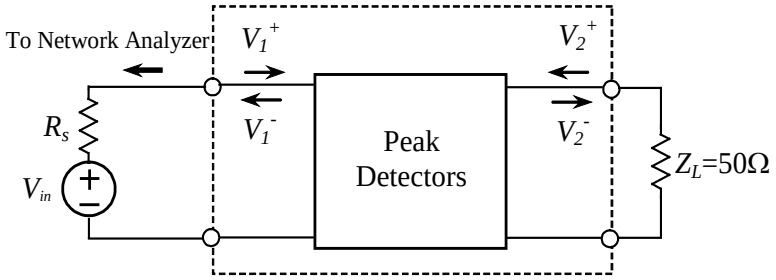

Figure 5. Measurement set-up for S_{21} Measurement of the PD1 and PD2

From the fact that S_{11} = S_{22} = 0, we know that V_2^- = 0 when port 2 is terminated in Z_L = 50Ω, and that V_2^+ = 0. In this case we then have that $V_1^+ = V_1$ and $V_2^- = V_2$ as the voltage across the 50Ω load resistor at port 2:

$$V_2^- = V_2 = S_{21}V_1 \tag{2a}$$

$$V_{T1} = S_{21}V_{in(1)} \text{ (for PD1)} \tag{2b}$$

$$V_{T2} = S_{21}V_{in(2)} \text{ (for PD2)} \tag{2c}$$

For the peak detector, PD1, input power, $P_{in(1)}$ is adjusted as Equations (3a) and (3b) to provide input voltage of 125 to 800 mV.

$$P_{in(1)} = \frac{V_{in(1)}^2}{R_s} = \frac{(0.125)^2}{50} = 0.3125mW = -5.05dBm \quad (3a)$$

$$P_{in(1)} = \frac{(0.8)^2}{50} = 12.8mW = 11.07dBm \quad (3b)$$

For the peak detector, PD2, input power, $P_{in(2)}$ is adjusted as Equations (4a) and (4b) to provide input voltage of 10 to 300 mV.

$$P_{in(2)} = \frac{(0.01)^2}{50} = 0.002mW = -26.99dBm \quad (4a)$$

$$P_{in(2)} = \frac{(0.3)^2}{50} = 1.8mW = 2.55dBm \quad (4b)$$

Using these measurement methods, DC voltage outputs V_{T1} and V_{T2} are obtained.

3. Measurement Results

3.1. Band-Gap Reference Circuit

Figure 6 shows variations of a band-gap reference voltage (V_{BGR}) for temperature and power supply V_{cc}. The temperature is varied from -40 to 100°C and the power supply is varied from 1 to 1.75V. The non-zero temperature coefficient of the reference voltage is achieved by summing the negative temperature coefficient and the positive temperature coefficient. As shown in Fig. 6, the V_{BGR} variation at 1V showed only 0.089V from 0 to 100°C and only 0.014V from -40 to 0°C. The V_{BGR} variation at 1.75V showed similar difference from -40 to 100°C. The V_{BGR} variation at 30°C also showed only 0.023V from 1 to 1.75V. These results verify that designed BGR circuit provides no noticeable effect on circuit performance for variations of temperature and power supply.

3.2. Test Amplifier

Figure 7 shows input impedances of BIST test amplifier for ($D_3D_2D_1$) = (001). These results are used to obtain magnitude of input impedance of the LNA. Since the test amplifier for (D_3,D_2,D_1) = (0,0,1) is designed with magnitude of Re($Z_{in(TA)}$) >> Im($Z_{in(TA)}$) at the frequency range of 4.5GHz and 6GHz, the phase shift for input impedance of test amplifier can be neglected and the matching is optimized. Modeling for input impedance of test amplifier is obtained using conventional Equations, and simulation is obtained using S-parameter results. Using probe station and vector network analyzer, the S-parameter measurement is performed on wafer. As shown in this figure, the measurement had very close results with modeling as well as simulation at 4.5-6GHz.

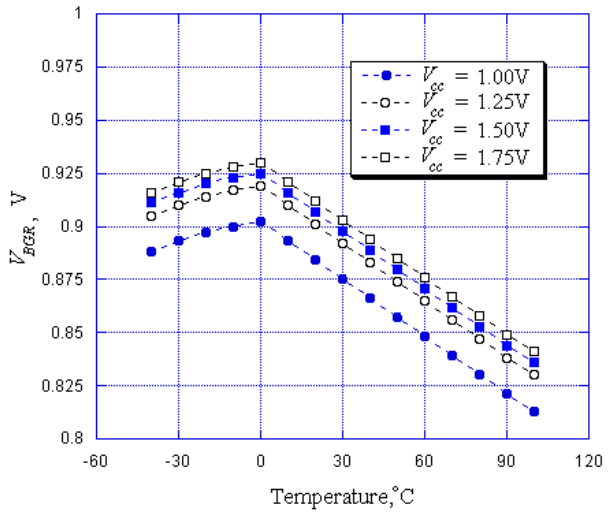

Figure 6. Band-gap Reference Voltage for Temperature and V_{cc}

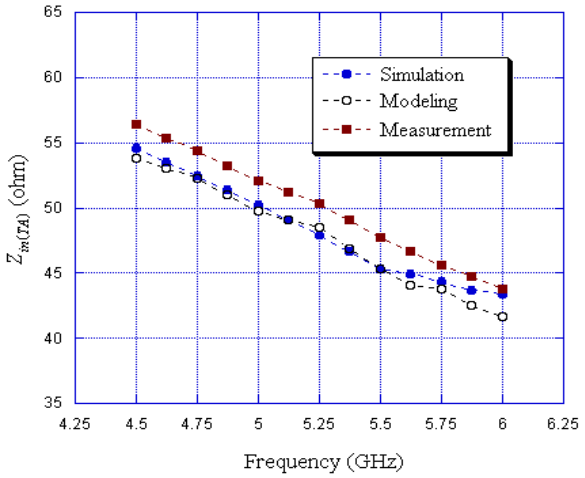

Figure 7. Input Impedances of the Test Amplifier for ($D_3D_2D_1$) = (001)

The gain of the test amplifier under several operating conditions is shown in Figure 8. These results are also used to infer the magnitude of the input impedance of the RF circuits. These real measurement values using S-Parameter are converted to obtain the voltage gain of the test amplifier. As shown in Figure 8, the measurement results were very similar to those predict with modeling as well as simulation at 4-6GHz. However, the measurement result showed the maximum gain at lower frequency than the modeling and the simulation. This frequency shift may be a result of parasitic effects at high frequency. The measurement result also showed an error of approximately 10% at 5.75-6GHz.

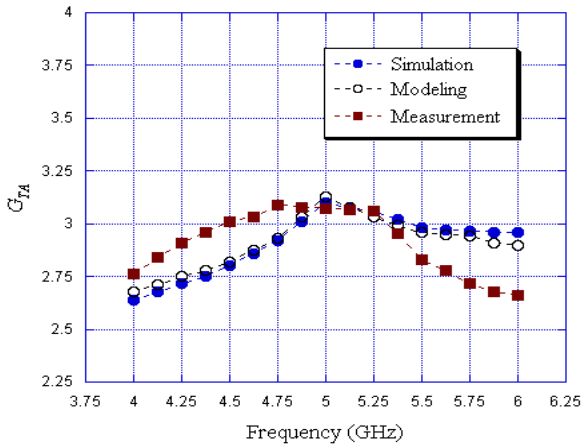

Figure 8. Gains of the Test Amplifier for ($D_3D_2D_1$) = (001)

3.3. Peak and Phase Detectors

Figure 9 shows comparison of the peak detector (PD1) transfer characteristic as determined by simulation and measurement at 5.25GHz. The x-axis and y-axis represent input and output voltages of the PD1, respectively. Measurement showed no detectable frequency dependence in the circuit performance up to the measurement limit of 5.25GHz set by the experimental arrangement. The simulation result and measurement were all very close with values given by Equation as shown in Figure 8. The largest fractional errors occurred, as expected, at low signal and large signal levels. For input voltage of V_{L1} = 150mV, simulation gave output voltage of V_{T1} = 25mV whereas measurement gave output voltage of V_{T1} = 45mV. For large input voltage of V_{L1} = 800mV, simulation gave output voltage of V_{T1} = 625mV whereas measurement gave output voltage of V_{T1} = 595mV.

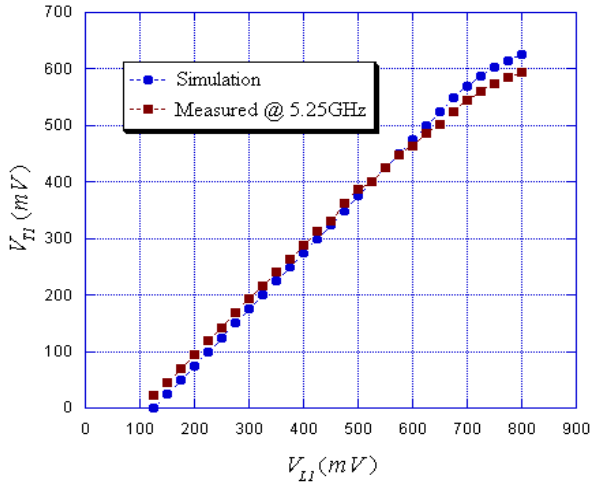

Figure 9. Comparison of the Peak Detector (PD1) Transfer Characteristic

The comparison of the peak detector (PD2) transfer characteristic as determined by simulation and measurement at 5.25GHz is shown in Figure 10. The measurements also showed no detectable frequency dependence in the circuit performance up to the measurement limit of 5.25GHz set by the experimental arrangement. The largest fractional

errors occurred, as expected, at low signal and large signal levels. For an input voltage of V_1 = 20mV, the simulation had an output voltage of V_{T2} = 10mV whereas the measurement had an output voltage of V_{T2} = 25mV. For a large input voltage of V_1 = 300mV, the simulation showed an output voltage of V_{T2} = 290mV whereas the measurement showed an output voltage of V_{T2} = 279mV. However, these results provided no noticeable effect on circuit performance.

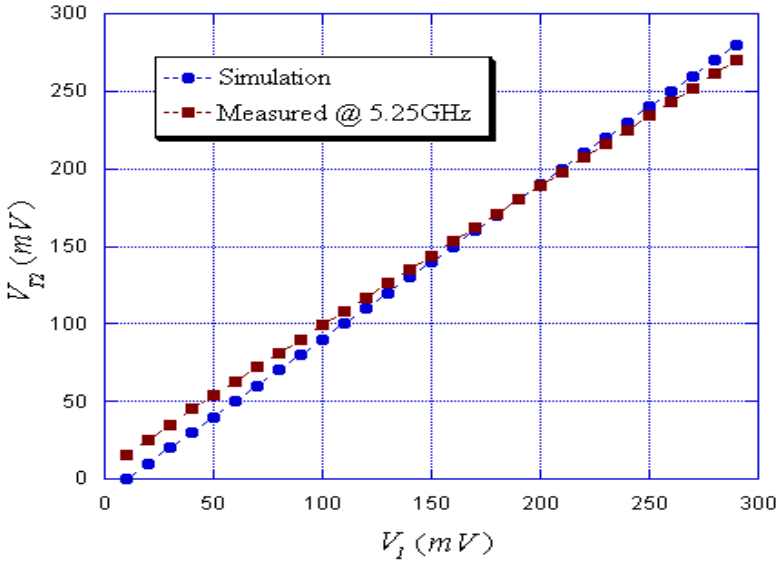

Figure 5.18. Comparison of the Peak Detector (PD2) Transfer Characteristic

3.4. RF BIST Circuit

The $V_{T1(ref)}$, $V_{T2(ref)}$, and $\Delta\theta_{T(ref)}$ measured at output of the BIST circuit are shown in Table1 1. The results show average values from 10 times experiments, and PVT variations of within less than ±2% for defect-free values are accepted. These values are measured after 50 nanoseconds settling time of the PD1, PD2, and PHD to ensure steady-state value. These results are used to obtain input impedances, voltage gains and noise figures of the RF circuits as shown in Table 1. As can be expected from simulation results, since the $V_{T1(ref)}$ is proportional to voltage gain, the $V_{T1(ref)}$ has the highest value at the operating frequency of 5GHz. The $\Delta\theta_{T(ref)}$ showed small difference at 5.25GHz. This value means perfect matching status at this frequency. When the frequency is increased, the $V_{T2(ref)}$ is also increased. As shown in Table 1, the measurement showed similar difference compared to the simulation. However, the measurement result showed the maximum values at a lower frequency than the simulation. This frequency shift may be a result of parasitic effects at high frequency.

To verify the performance of our proposed BIST, the two-stage LNA (Low Noise Amplifier) as a typical circuit of RF ICs was designed. It is designed for a 5-GHz IEEE802.11a wireless LAN application. It is powered by a 1-V supply. The circuit is referred to [1].

Table 1. $V_{T1(ref)}$, $V_{T2(ref)}$ and $\Delta\theta_{T(ref)}$ Measured by the RF BIST Circuit

Frequency [GHz]	$V_{T1(ref)}$ [mV]		$V_{T2(ref)}$ [mV]		$\Delta\theta_{T(ref)}$ [°]	
	Simulation	Measurement	Simulation	Measurement	Simulation	Measurement
4.50	400	343.8	166.20	205.3	-24	-20
4.75	421	335.7	160.30	218.2	-16	-11
5.00	448	304.8	171.40	213.4	-8	-2
5.25	445	274.9	180.00	205.4	0	2
5.50	432	253.0	189.00	182.3	8	4
5.75	418	232.0	191.05	168.1	16	10
6.00	406	219.1	192.02	160.2	24	16

Table 2 shows partial list of V_{T1} and V_{T2} values for several cases presented in 5.25GHz LNA. These results are measured at 5.25GHz using proposed BIST. In Table 2, we considered faults in transistor M_1 (M_{01}) and inductor L_1 (L_{01}). These results are used to obtain important specifications of the low noise amplifiers such as voltage gains, noise figures and magnitudes of input impedances. As shown in Tables 2, fault-free values were significantly different from faulty values, respectively. This result verifies that the proposed BIST can detect various defects from RF circuits.

Table 2. The Results of RF BIST Outputs for 5.25GHz LNA

Test Voltage / Faults	V_{T1} [mV]	V_{T2} [mV]
Fault-free	445.0	180.0
Q_1 Base Open	127.3	209.6
Q_1 B-E Short	127.3	220.0
Q_1 E-C Short	155.2	144.6
L_b + 30%	389.3	194.8
L_b + 40%	383.5	192.0
L_b +50%	375.8	189.8

4. Conclusions

In this paper, we proposed a programmable RF BIST (Built-In Self-Test) circuit. We proved that our programmable RF BIST circuit can help to sort out good and bad RFIC chips in the wafer level as well as providing all of the functional testing. The new programmable RF BIST circuit provided successful testing of LNA chips. To adjust calibration, the BIST was self-programmed. The RF low noise amplifiers provided with complete testing by utilizing a novel BIST architecture. We hope that this new capability will provide industry with a low-cost technique to test RFIC chips.

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