Digital Controlled Oscillator Design with Novel 3 Transistors XOR Gate

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Abstract

The Digital controlled oscillator (DCO) is the core element of all digital phase locked loop (ADPLL) system. Here, we propose DCO structures with digital control, reduced hardware and low power consumption. Different DCOs are based on ring based topology having 3, 4 & 5 control bits. Number of control bits can be increased as per the requirement of output frequency range. DCOs using XOR as an inverter having NMOS and PMOS transistors in pull up and pull down switching networks are presented. Three bit DCO with NMOS control network shows frequency variations of [3.1763 - 3.5290] GHz with power consumption variations of [266.8491 - 293.6420] µW. Three bit DCO with PMOS network shows frequency variation of [1.9918 - 1.4313] GHz with power consumption variation of [46.1176 - 22.8450] µW. Four bit DCO with NMOS & PMOS control networks shows frequency variations of [3.2219 - 3.6114] GHz & [2.1328 - 1.4627] GHz respectively. Power consumption variations of [266.8491 - 294.9430] µW & [53.5188 - 22.8454] µW have been obtained for 4-bit DCO having NMOS & PMOS switch networks respectively. Finally the five bit DCO with NMOS & PMOS network shows output frequency range of [3.3050 - 3.5557] & [2.2579 - 1.4934] GHz. Power consumption of [266.8491 - 295.5983] µW & [61.3773 - 22.8453] µW have been reported with NMOS & PMOS network for 5-bit controlled DCO. Comparisons with earlier reported circuits have been made and reported design shows improvement over previous circuits.

Keywords: *Digital control oscillator (DCO), delay cell, power consumption, voltage controlled oscillator (VCO), XOR gate*

1. Introduction

Due to ever increasing growth of wireless communication systems, the need for low power and cost effective devices is growing exponentially. The Phase locked loops (PLL) are the fundamental circuit elements of data transmission systems and have extensive applications in data modulation, demodulation and mobile communication. Voltage control oscillators (VCO) are the critical and necessary building blocks of these PLL systems. Fully digital PLL known as all digital phase locked loop (ADPLL) [1]-[4] have been developed to over come the disadvantage of analog techniques. Analog PLL have the disadvantages of large noise and sensitivity toward process parameters. Digitally controlled oscillators (DCOs) are the replacement of analog voltage control oscillators (VCOs) in digital PLL systems [5]-[7]. These ADPLL systems have fast frequency locking, full digital control and good stability [1].

With the scaling of technology towards the deep submicron CMOS process, fully digital control oscillators have become highly attractive circuit components. Different designs for digital controlled oscillators have been reported over varied operating frequency range. In path delay oscillator the logic gates are utilized to form a ring structure [6], [8], [9]. The second category of DCO is schmitt trigger current driven oscillators [4], [5], [7], having large number of MOS transistors. Current starved ring oscillators consumes large area and with more hardware complexity are also reported [1], [3].

Delay element is a vital component of oscillator circuit and its precision and power consumption directly contributes to the overall performance of DCO system. A variety of digitally controlled delay elements (DCDE) have been reported in literature [10]-[13]. Two parameters modulate the output frequency of ring oscillator structure. One is propagation delay time of each delay stage and second is total number of delay stages in close ring structure. In DCO structures the oscillating frequency is determined by digital input vector applied to DCDE. Controls switch network of NMOS/PMOS transistors are placed at the sources/drain of NMOS/PMOS transistor of inverter delay cell. Depending upon the condition of input vector, the equivalent resistance of switch network changes and delay of particular stage changes which further modulates the output frequency[1],[14].

In recent years power consumption and output frequency range have become significant performance criteria [14]-[17] in DCO system design. Increasing demand of handheld devices like cellular phones, notebooks, personal communication devices have aggressively enhanced the attention for power efficiency. In battery operated communication systems power consumption has also become more significant factor due to exponential increase in data rates. Power consumption in very large scale integration (VLSI) systems includes dynamic, static power and leakage power. Dynamic power consumption results from switching of load capacitance between two different voltages and is dependent on frequency of operation. Static power is contributed by direct short circuits current component between supply (V_{dd}) & ground (V_{ss}) and it is dependent on leakage currents components. Controlled oscillator is the major components of PLL system and also accountable for most of the power consumption of PLL system. The operating frequency can be increased with more capacitance loading which further adversely affects the total power consumption of oscillator [18], [19]. At circuit level power efficiency can be improved with an optimized design. Optimization are possible in different ways like reduction of switching activity, capacitance and by reducing the short circuit currents etc. This paper proposes novel DCO circuits with XOR gate based inverter delay cell used in ring topology. Here, switch network of transistors are added with inverter based delay cell to control the oscillator frequency. Proposed DCO circuits avoid the analog tuning voltage control and provide the design flexibility with higher power efficiency.

This paper is organized as follows: Section II describes the working of proposed delay cell. Three, four and five bit controlled DCO circuits have been presented in this section. Simulation results and discussion have been described in section III. Section IV concludes the work.

2. System Description

Digitally controlled delay elements (DCDE) are the heart on any DCO structure. The designs of DCO in this paper are based on digitally controlled inverter delay elements connected in ring topology. Three transistor XOR gate working as inverter has been utilized as delay element. One input terminal of XOR gate is connected to V_{dd} and input signal is applied to second terminal and this circuit works as an inverter. Due to elimination of direct path from supply (V_{dd}) and ground (V_{ss}) in XOR based inverter the power consumption is

reduced. Binary weighted MOS transistors as shown in figure 1(a) & (b) have been used in switch networks and delay of each stage has been controlled by binary bits applied to these transistors. With changing bit patterns different transistors are selected with unequal width and resistance of transistor network changes accordingly which further modulates the delay of circuit. Changing delay produces different frequency components as controlled by digital input word.

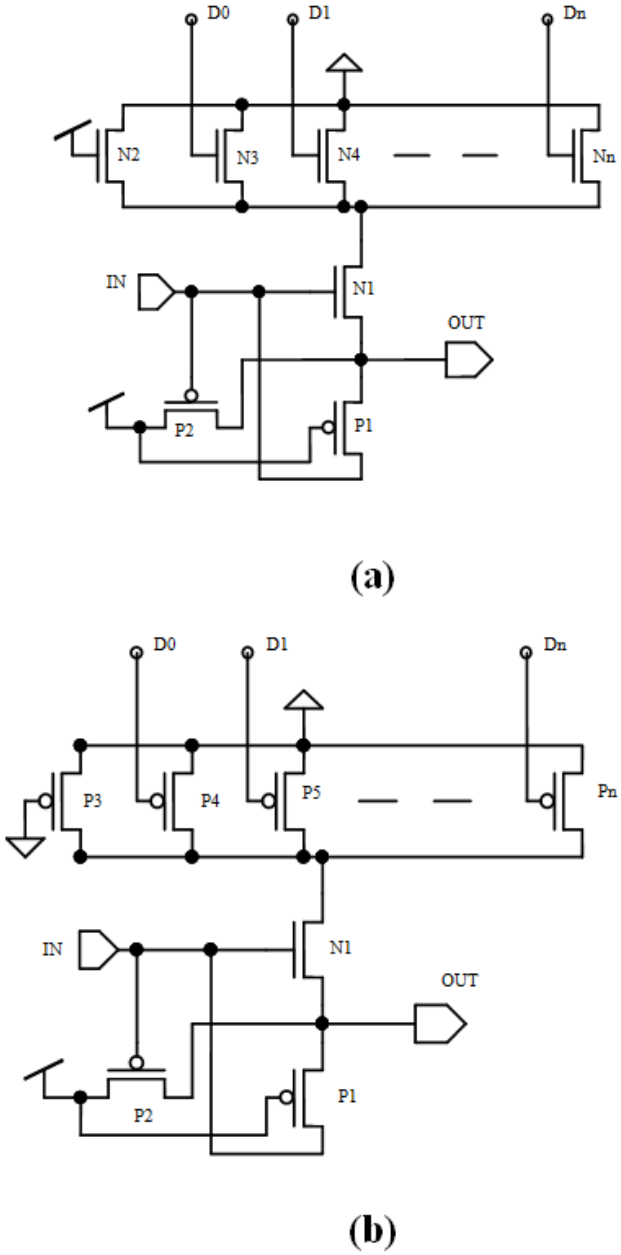


Figure 1. Delay Cell with (a) NMOS (b) PMOS Switch Network

Two different delay cells have been proposed using NMOS & PMOS switching networks as shown in figure 1. Number of bits can be increased or decreased as per the need of

frequency tuning. Gate length of all transistors has been taken as 0.18µm. In XOR based inverter section, width of P1 and P2 has been taken as 2.0µm whereas width of N1 has been taken as 0.25µm. Width of NMOS and PMOS transistors of switching network are binary weighted and have been shown in table 1.

Table 1. Width of PMOS and NMOS Transistors in Delay Cell

PMOS transistors	Width(µm)	NMOS transistors	Width(µm)
P3	1.0	N2	0.5
P4	2.0	N3	1.0
P5	4.0	N4	2.0
P6	8.0	N5	4.0
P7	16.0	N6	8.0
-	-	-	-
-	-	-	-
Pn	2^{n-3}x1	Nn	2^{n-2}x0.5

First DCO structure (DCO-I) with three delay cells having 3-bit control has been shown in figure 2. Switch networks having four NMOS transistors are connected with source terminal of transistor N1 of each delay cell. Four NMOS transistors [N2-N5] are binary weighted with first transistor having V_{dd} supply at gate terminal to provide path for current conduction. Three control bits [D0-D2] are applied to three binary weighted NMOS transistors [N3-N5].

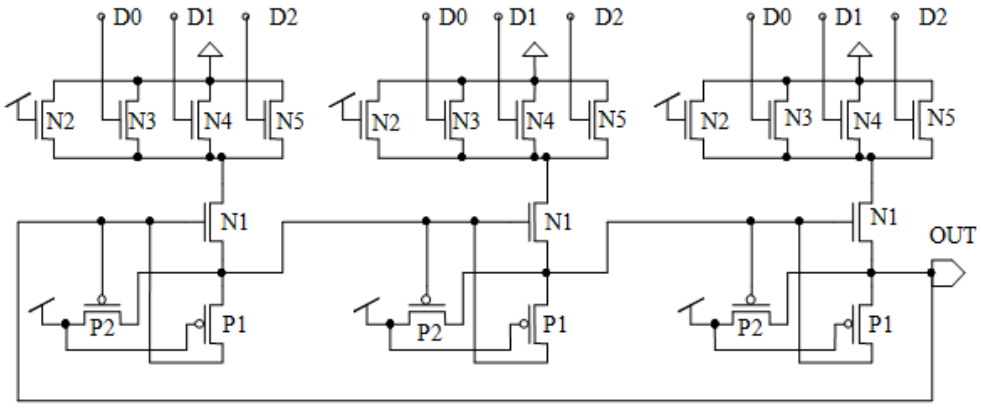


Figure 2. Three Bit DCO with NMOS Switching Networks

Second DCO structure (DCO-II) has been implemented with PMOS switch networks connected as shown in figure 3. Gate of first PMOS transistor P3 of switch network in each delay cell is grounded to provide the path for current conduction. Three control bits [D0-D2] are applied to remaining three binary weighted PMOS transistors [P4-P6]. Transistors with different width are selected with application of control bits which modulated the output frequency.

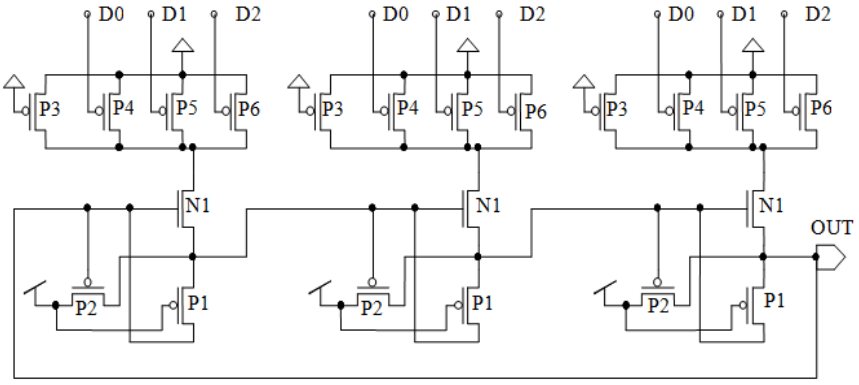
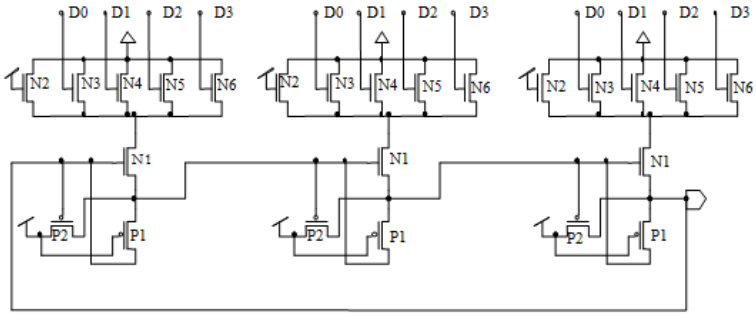
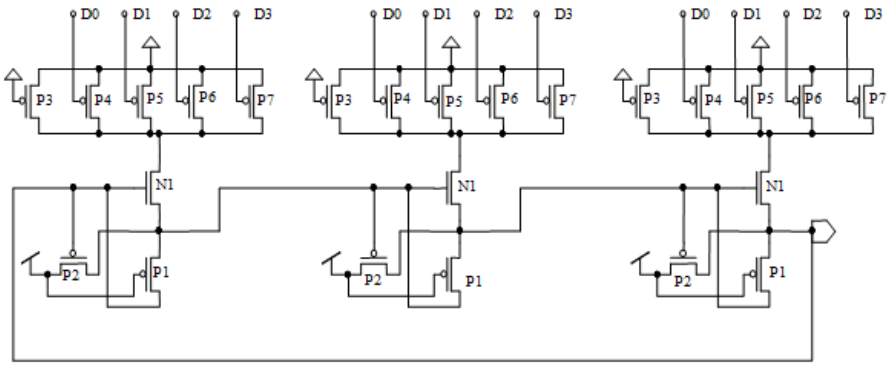


Figure 3. Three Bit DCO with PMOS Switching Networks

Four & five bit control DCO structures also have been implemented with same methodology as presented for three bit DCO structures. Figure 4(a) shows 4-bit DCO with NMOS switching network. Input vector having four bits [D0-D3] has been applied to binary weighted transistors [N3- N6]. DCO design having 4-bit control with PMOS switch network has been shown in figure 4(b). Control bits [D0-D3] have been applied to transistors [P4-P7] in PMOS network. Figure 5(a) shows 5-bit DCO circuit with NMOS switching network. Transistor N2 is always in ON condition with gate at V_{dd} whereas control bits [D0-D4] have been applied to remaining binary weighted NMOS transistors [N3 -N7]. Figure 5(b) shows the 5-bit controlled DCO with PMOS switching network.



(a)



(b)

Figure 4. Four Bit DCO with (a) NMOS (b) PMOS Switching Networks

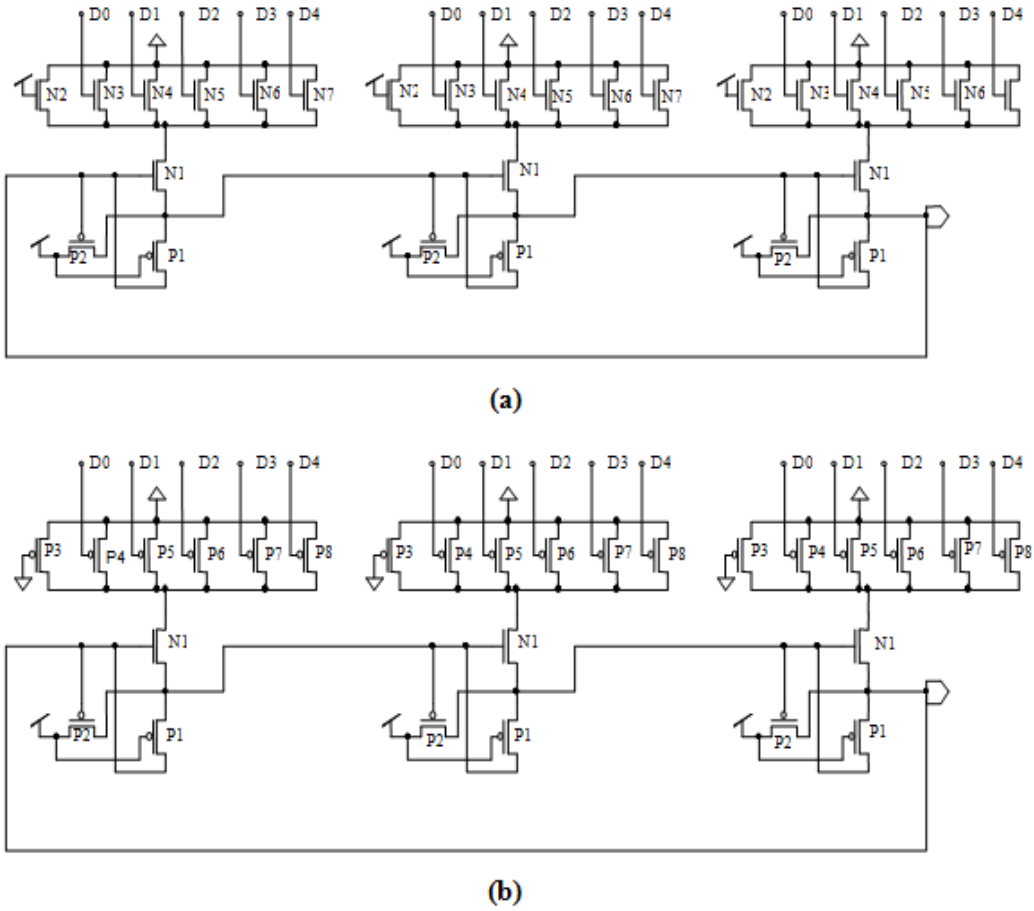


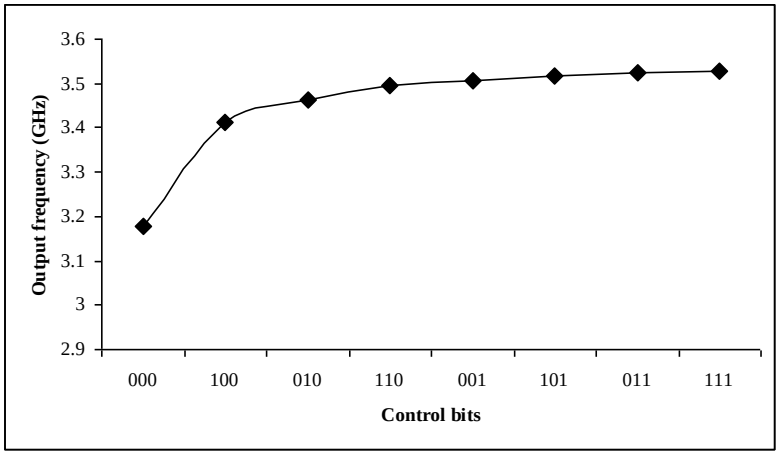
Figure 5. Five Bit DCO with (a) NMOS (b) PMOS Switching Network

3. Results and Discussions

The results have been obtained using SPICE based on TSMC 0.18μm process technology with supply voltage of 1.8V. Table 2 shows the results of 3-bit controlled DCO with NMOS and PMOS switching networks. Power consumption and output frequency has been obtained with different control bits [000 - 111]. Figure 6(a) shows the variation of frequency with NMOS controlled network. Power consumption variation for 3-bit DCO having NMOS switching network has been shown in figure 6(b). In 3-bit NMOS switch network DCO the resistance decreases with varying bit pattern from 000 to 111 and the delay of circuit also reduces. With decrease in delay the output frequency increases with subsequent rise in power consumption as shown in table 2. In PMOS based DCO circuit the resistance of switch network increases with changing bit pattern from 000 to 111 and output frequency decreases due to rise in delay as shown in figure 7(a). Power consumption decreases due to reduced current between supply (V_{dd}) and ground (V_{ss}) as shown in figure 7(b). Output waveform results with input vector [111] have been shown in figure 8(a) & (b) for 3-bit DCO structures.

Table 2. Frequency and Power Consumption Variations for 3-bit DCO

Control bits	NMOS network		PMOS network	
	Power consumption (μW)	Frequency (GHz)	Power consumption (μW)	Frequency (GHz)
000	266.8491	3.1763	46.1176	1.9918
100	284.9757	3.4136	44.4791	1.9662
010	288.7529	3.4624	42.9445	1.9508
110	290.9761	3.4945	40.7278	1.9121
001	291.6941	3.5047	38.9851	1.8852
101	292.6410	3.5169	35.6296	1.8259
011	293.1648	3.5240	31.6637	1.7212
111	293.6420	3.5290	22.8450	1.4313



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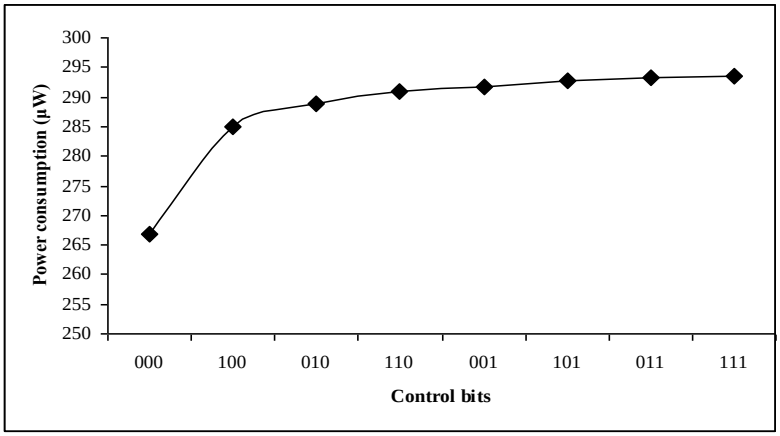
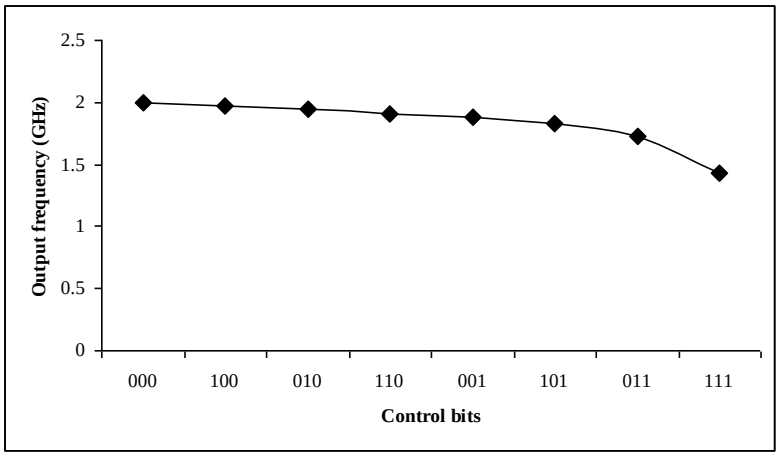


(b)

Figure 6. (a) Output Frequency (b) Power Consumption of 3-bit DCO with NMOS Switch Networks



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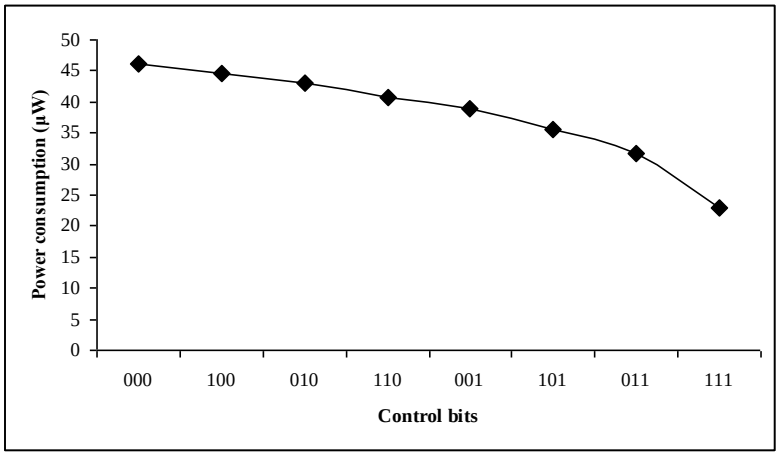

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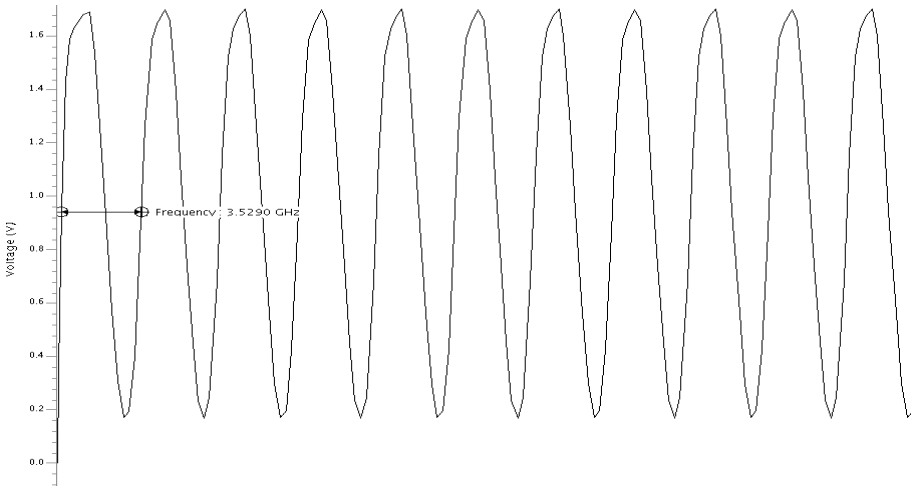
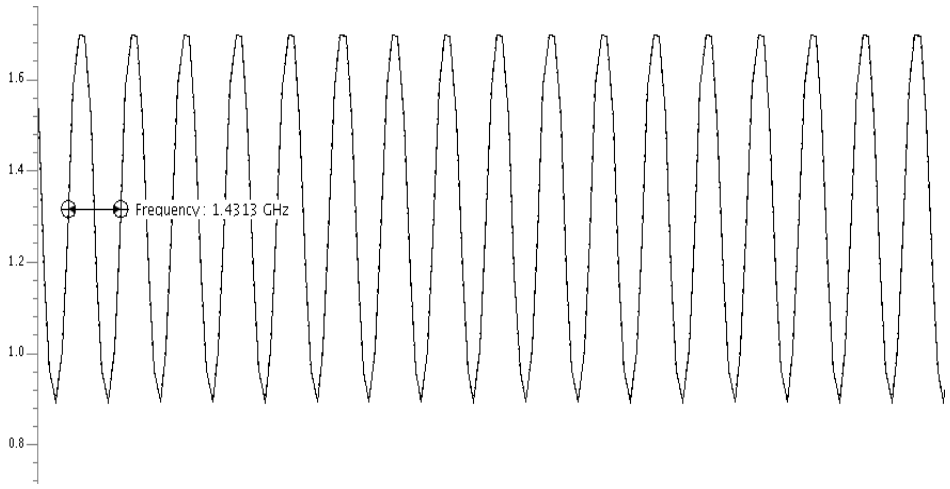
Figure 7. (a) Output Frequency (b) Power Consumption of 3-bit DCO with PMOS Switch Networks



(a)



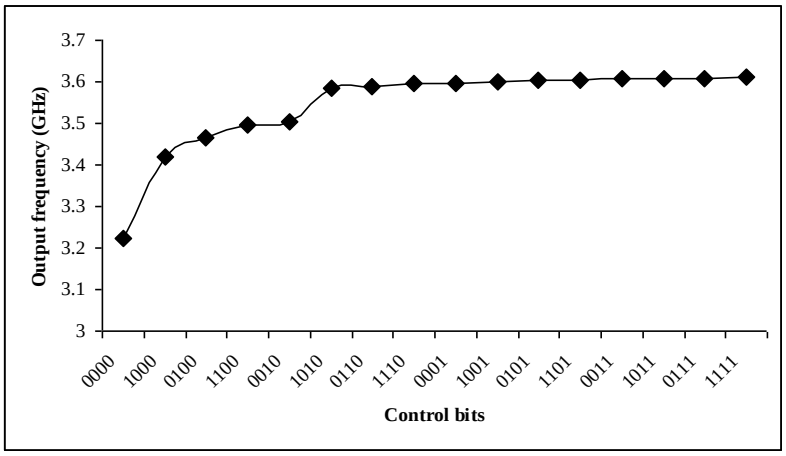
(b)

Figure 8. Output Waveforms of 3-bit DCO with Control Bits [111] for (a) NMOS (b) PMOS

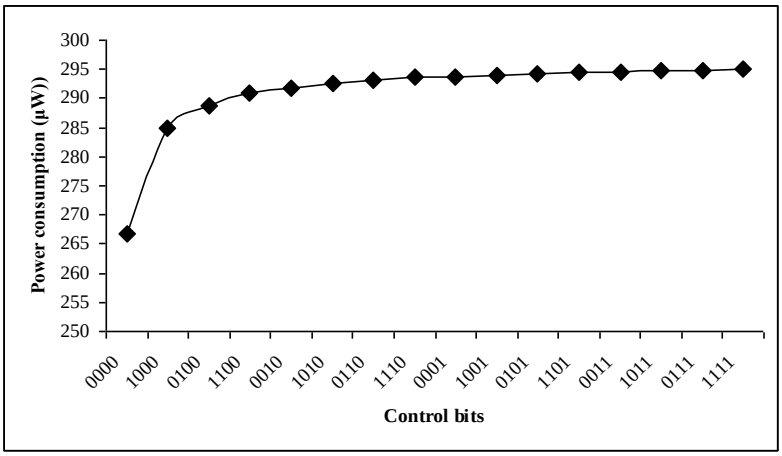
Table 3 shows the results of 4-bit control DCO with NMOS and PMOS switching network. Power consumption and output frequency results have been obtained for varying control bits [0000 - 1111]. Figure 9(a) shows variation of frequency for NMOS switch based circuit with changing control bits. Power consumption variation for 4-bit DCO with NMOS switch networks has been shown in figure 9(b). Output frequency and power consumption increase in NMOS switch based DCO circuit as resistance is reduced with changing bit pattern. In PMOS switch based DCO opposite behavior is observed as shown in figure 10(a) & (b). Output waveform results for input vector [1000] have been shown in figure 11(a) & (b) for 4-bit DCO structures.

Table 3. Frequency and Power Consumption Variations for 4-bit DCO

Control bits	NMOS network		PMOS network	
	Power consumption (µW)	Frequency (GHz)	Power consumption (µW)	Frequency (GHz)
0000	266.8491	3.2219	53.5188	2.1328
1000	284.9757	3.4192	52.6638	2.1228
0100	288.7529	3.4663	51.928	2.1146
1100	290.9761	3.4980	50.9513	2.1035
0010	291.6941	3.5055	50.2910	2.0964
1010	292.6410	3.5828	49.1654	2.0836
0110	293.1648	3.5889	48.1698	2.0780
1110	293.6420	3.5946	46.8134	2.0585
0001	293.6158	3.5943	46.1175	2.0584
1001	293.9763	3.5989	44.4791	2.0279
0101	294.2050	3.6023	42.9445	2.0072
1101	294.4352	3.6051	40.7278	1.9714
0011	294.5373	3.6064	38.9851	1.9355
1011	294.7056	3.6086	35.6294	1.8683
0111	294.8204	3.6092	31.6638	1.7662
1111	294.9430	3.6114	22.8454	1.4627

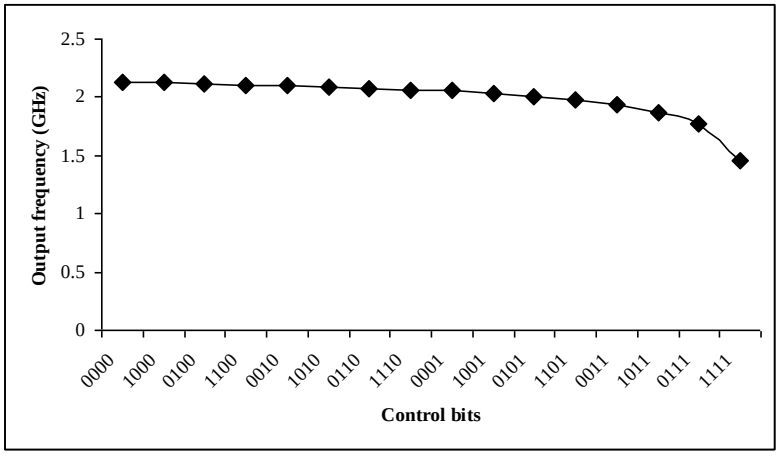


(a)



(b)

Figure 9. (a) Output Frequency (b) Power Consumption of 4-bit DCOs with NMOS Networks



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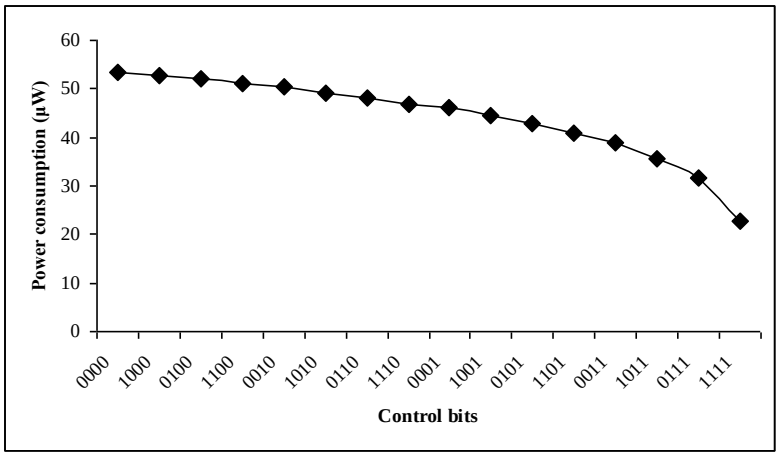

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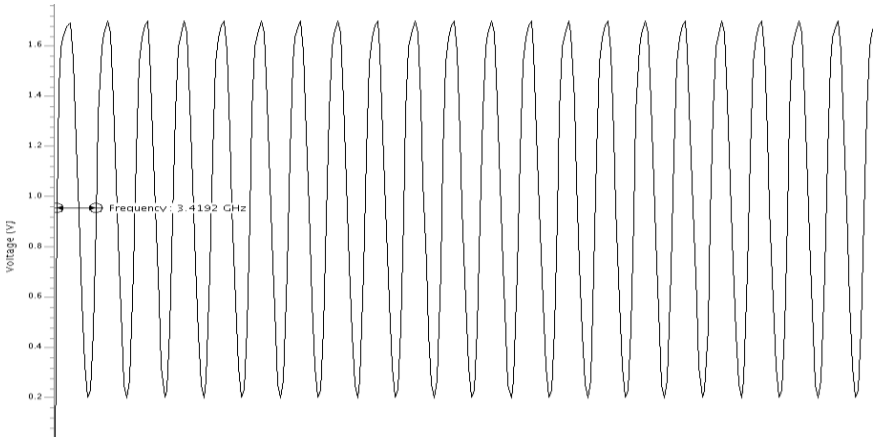
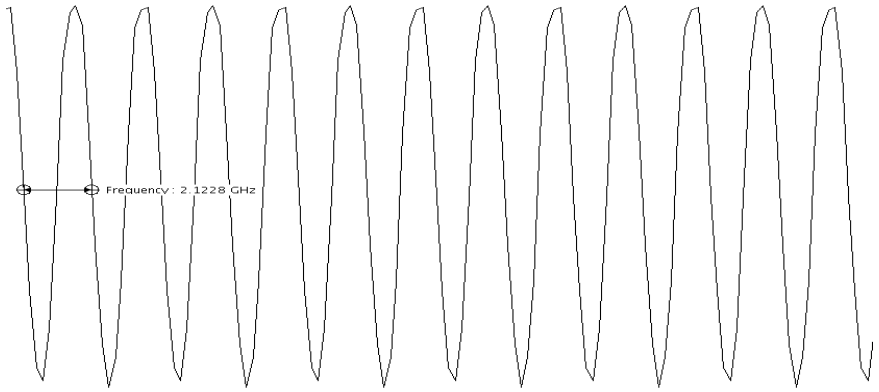
Figure 10. (a) Output Frequency (b) Power Consumption of 4-bit DCOs with PMOS Networks



(a)



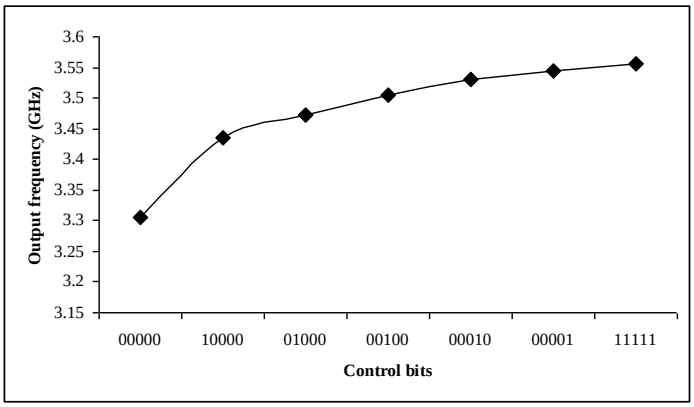
(b)

Figure 11. Output Waveforms of 4-bit DCO with Control Bits [1000] for (a) NMOS (b) PMOS

Table 4. Frequency and power consumption variations for 5 bit DCO

Control bits	NMOS network		PMOS network	
	Power consumption (μW)	Frequency (GHz)	Power consumption (μW)	Frequency (GHz)
00000	266.8491	3.3050	61.3773	2.2579
10000	284.9757	3.4342	60.9225	2.2537
01000	288.7529	3.4724	60.5468	2.2432
00100	291.6941	3.5057	59.7520	2.2349
00010	293.6158	3.5302	57.9938	2.2154
00001	294.7326	3.5441	53.5188	2.1593
11111	295.5983	3.5557	22.8453	1.4934

Table 4 shows the results of 5-bit control DCOs with NMOS and PMOS switching networks for selected input patterns. Figure 12(a) shows variation of frequency for NMOS switch based circuit with changing control bits. Power consumption variations for 5-bit DCOs with NMOS switch network has been shown in figure 12(b). Output frequency and power consumption goes up in NMOS switch based DCO circuit as resistance is decreased with varying bit pattern. In PMOS switch based DCO reverse behavior is observed as shown in figure 13(a) & (b). Output waveform results for input vector [10000] have been shown in figure 14(a) & (b) for 5-bit DCO structures.



(a)

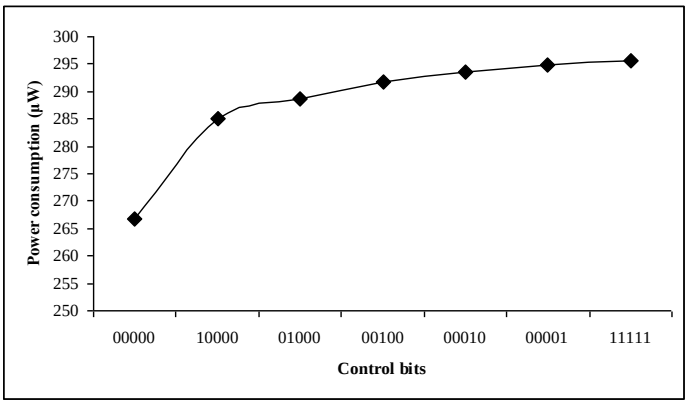


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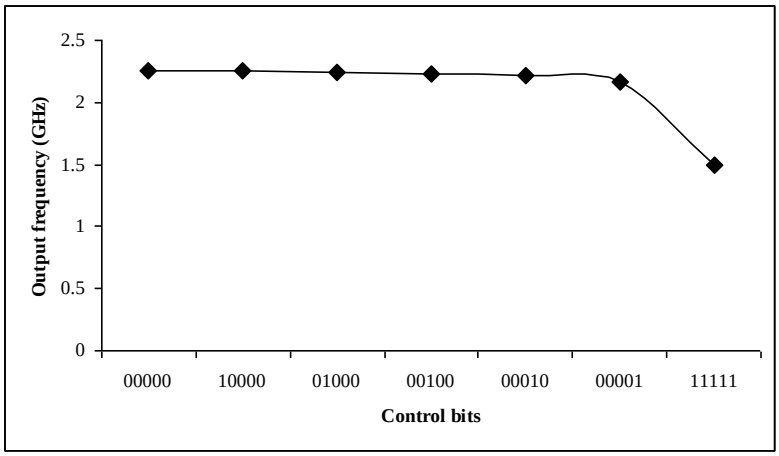
Figure 12. (a) Output Frequency (b) Power Consumption of 5-bit DCOs with NMOS Networks



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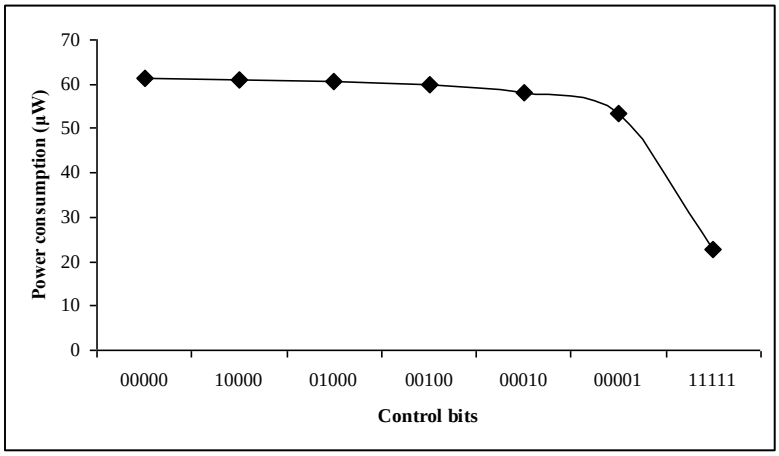
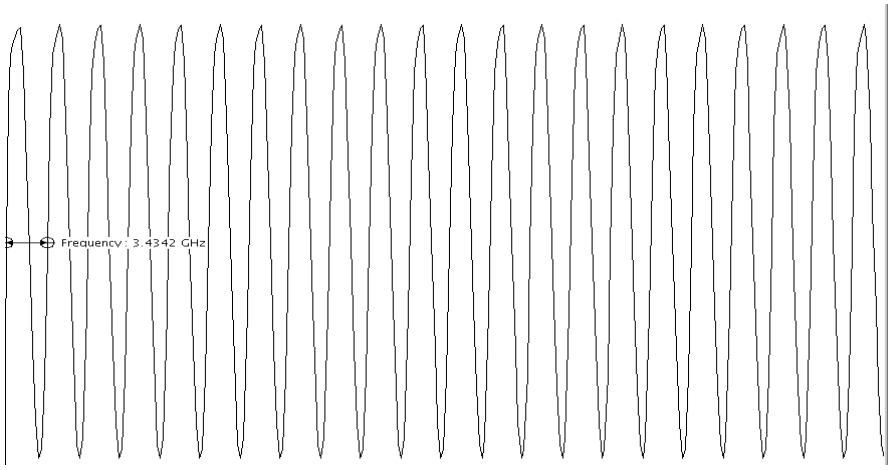


(b)

Figure 13. (a) Output Frequency (b) Power Consumption of 5-bit DCOs with PMOS Networks



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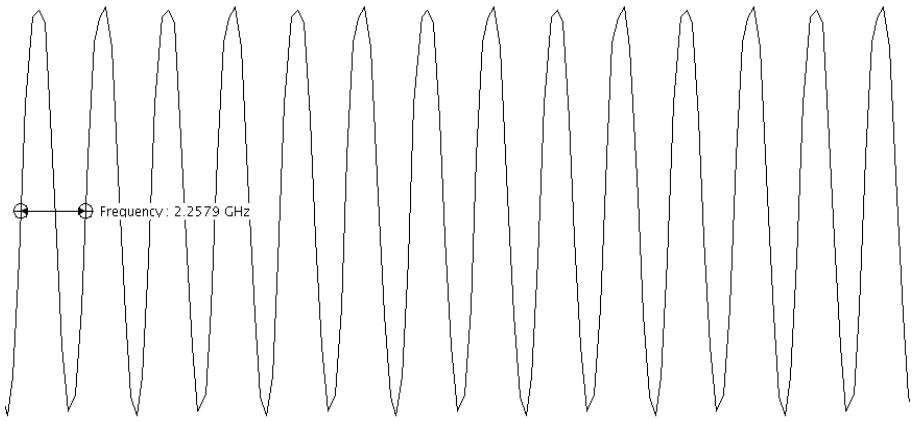

(b)

Figure 14. Output Waveforms of 5-bit DCO with Control Bits [10000] for (a) NMOS (b) PMOS

Comparisons with earlier reported circuits in terms of power consumption and frequency range have been shown in table 5. Proposed circuit's shows considerable power saving with adequate output frequency range.

Table 5. Comparison of DCOs

DCO structure	Power Consumption	Output frequency	Technology
[9]	63.4 mW	333-1472 MHz	0.35µm
[13]	-	1.350 - 4.550 GHz	0.18µm
[4]	2.3 mW	570 - 850 MHz	32nm
[8]	5.4 mW	87 – 250 MHz	0.18µm
[17]	25 mW	1.2 GHz	0.6µm
[5]	2.2 mW	570 - 800 MHz	32nm
[12]	-	0.750 - 1.6 GHz	0.5µm
Present work [3-bit NMOS]	266.8491 - 293.6420 µW	3.1763 - 3.5290 GHz	0.18µm
Present work [3-bit PMOS]	46.1176 - 22.8450 µW	1.9918 - 1.4313 GHz	0.18µm
Present work [4-bit NMOS]	266.8491 - 294.9430 µW	3.2219 - 3.6114 GHz	0.18µm
Present work [4-bit PMOS]	53.5188 - 22.8454 µW	2.1328 - 1.4627 GHz	0.18µm
Present work [5-bit NMOS]	266.8491 - 295.5983 µW	3.3050 - 3.5557 GHz	0.18µm
Present work [5-bit PMOS]	61.3773 - 22.8453 µW	2.2579 - 1.4934 GHz	0.18µm

4. Conclusions

The new structures for digital controlled oscillators (DCOs) with XOR gate based delay cell having full digital control are reported in this paper. Three, four and five bit controlled DCO have been implemented with proposed delay cells. Resistance of switch network has been varied by digital control bits and delay of circuit has been modulated. Power consumption is reduced due to optimized XOR gate in which direct path between V_{dd} and ground has been eliminated. Three bit DCO with NMOS network gives output frequency [3.1763 - 3.5290] GHz with power consumption of [266.8491 - 293.6420] µW. Three bit DCOs with PMOS network shows output frequency of [1.9918 - 1.4313] GHz with power consumption of [46.1176 - 22.8450] µW. Four bit DCO with NMOS network gives output

frequency [3.2219 - 3.6114] GHz with power consumption of [266.8491 - 294.9430] μW. Four bit DCO with PMOS network shows output frequency [2.1328 - 1.4627] GHz with power consumption of [53.5188 - 22.8454] μW. Finally the 5-bit controlled DCO give the frequency range of [3.3050 - 3.5557] & [2.2579 - 1.4934] GHz with NMOS and PMOS switch networks respectively. Power consumption variation ranges of [266.8491 - 295.5983] & [61.3773 - 22.8453] have been obtained for 5-bit DCO with NMOS & PMOS network respectively. Comparison with earlier reported circuits have been made and reported circuits shows wide output frequency range with lower power consumption.

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