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Optimization of Control Block of 3-bit PWM using Adiabatic Dynamic CMOS Logic for OLED Illumination System Based on Internet of Things Service

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Abstract

The environment development for deep sleep has been studied using analysis results of the big data about vital signs and parameters in the bedroom. The organic light emitting diode (OLED) illuminations of the bedroom are dimming using analysis results of the big data. Therefore, a low-power and compact design of dimming part is required for OLED illumination system. In this paper, the optimized control block of the clock cut-off circuit was designed using De Morgan's laws with adiabatic dynamic CMOS logic (ADCL) digital 3-bit pulse width modulation (PWM). The designed clock cut-off circuit pauses the D-flipflops (D-ffs) after cutting off the clock at both 0 % and 100 % pulse width of PWM output for dimming. As a result, 10 transistors of the miniaturized control block were reduced and layout area of the optimized control block is 2,198.0μm^2 using Rohm 0.18μm standard CMOS model .The operation of control block of clock cut-off circuit with ADCL 3-bit digital PWM is confirmed by post-simulation of hspice.

Keywords: *clock cut-off circuit, optimization, adiabatic dynamic CMOS logic (ADCL), digital PWM, OLED illuminations system, internet of things (IoT) service*

1. Introduction

Recently, personal health check and care have attracted significant attention and are increasing using wearable device, ubiquitous device and internet of things (IoT) service [1]. Moreover, environment development for deep sleep has been studied using analysis results of the big data about vital signs and parameters in the bedroom ; breath rate, heart rate, temperature, humidity, brightness of illumination etc. The organic light emitting diodes (OLEDs) which are the closest to natural light have been widely used for illumination of the bedroom and are dimming using analysis results of the big data as shown in Fig. 1[2]. An institution of Yamagata university, Smart MIRAI House, was built to demonstrate the research results for the living environment of the near future and to verify correlation between big data analysis and deep sleep as shown Fig 2.

Presently, the OLED illumination system consists of a power part, dimming circuit part and OLED part, as shown in Fig. 1[3-4]. Although power consumption of the dimming circuit part is the lowest, size and power consumption of the digital circuit, including the dimming circuit part will increase for high-performance OLED illumination systems in the future. Therefore, a low-power and compact design of the dimming circuit part is

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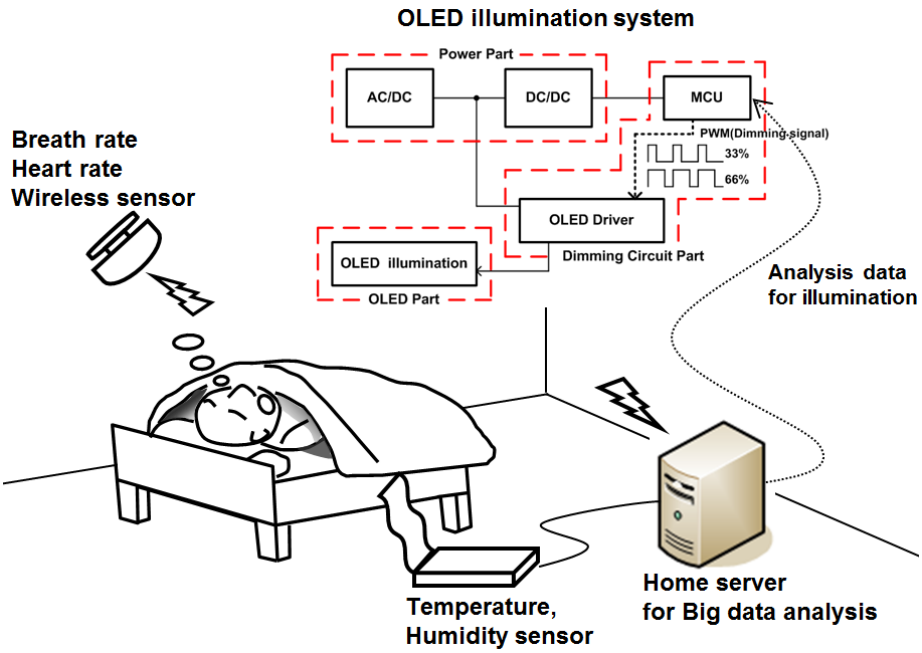


Figure 1. OLED Illumination System using Big Data Analysis

required for low-power OLED illumination systems. The pulse width modulation (PWM) is normally used for the dimming circuit [5-7].

Figure 2. Experiment Environment at Smart MIRAI House

The adiabatic dynamic CMOS logic (ADCL) was studied to reduce the power loss in a conventional CMOS logic for the low-power design of a logic circuit [8-16]. Power loss occurs by a sudden change in voltage from high to low and from low to high in CMOS logic with a direct current (DC) power supply. On the other hand, this power loss is reduced by slowly increasing and decreasing the power supply voltage in ADCL with the alternate current (AC) that is synchronized with for a change to high or low.

The OLED dimming circuit part was designed using the ADCL in Ref. [15]. On the other hand, the architecture has not been optimized. Furthermore, the power consumption is increased by the unnecessary operation of the ADCL D-flipflops (D-ffs) in ADCL digital 3-bit PWM at both dimming 0 % and 100 % of the PWM output. In this paper, the clock cut-off circuit, which controls the wake-up and sleep mode of the ADCL D-ffs, is proposed. The Optimized control block of the clock cut-off circuit is designed using De Morgan's laws with adiabatic dynamic CMOS logic digital 3-bit PWM for OLED dimming system.

The remainder of this paper is organized as follows. Section 2 describes the adiabatic charging, and standard operation of adiabatic logic. A low-power ADCL digital 3-bit PWM was designed and optimized for an OLED illumination system. And layout of the miniaturized control block was designed using Rohm 0.18µm standard CMOS model in section 3. Section 4 reports the post-simulation results of designed circuits using Rohm 0.18µm standard CMOS model. Finally, section 5 concludes the paper.

2. Adiabatic Logic

2.1. Adiabatic Charging

During a sudden transition between high and low levels of the input voltage, a load capacitor cannot be charged and discharged immediately. Power dissipation occurs by the resistive component of the logic circuit in the conventional CMOS logic because this logic circuit uses a constant voltage; DC power supply. To minimize the power dissipation, adiabatic charging is one of the promising candidates with AC power, which has a slower rising/falling time than charge/discharge time constant [8-11].

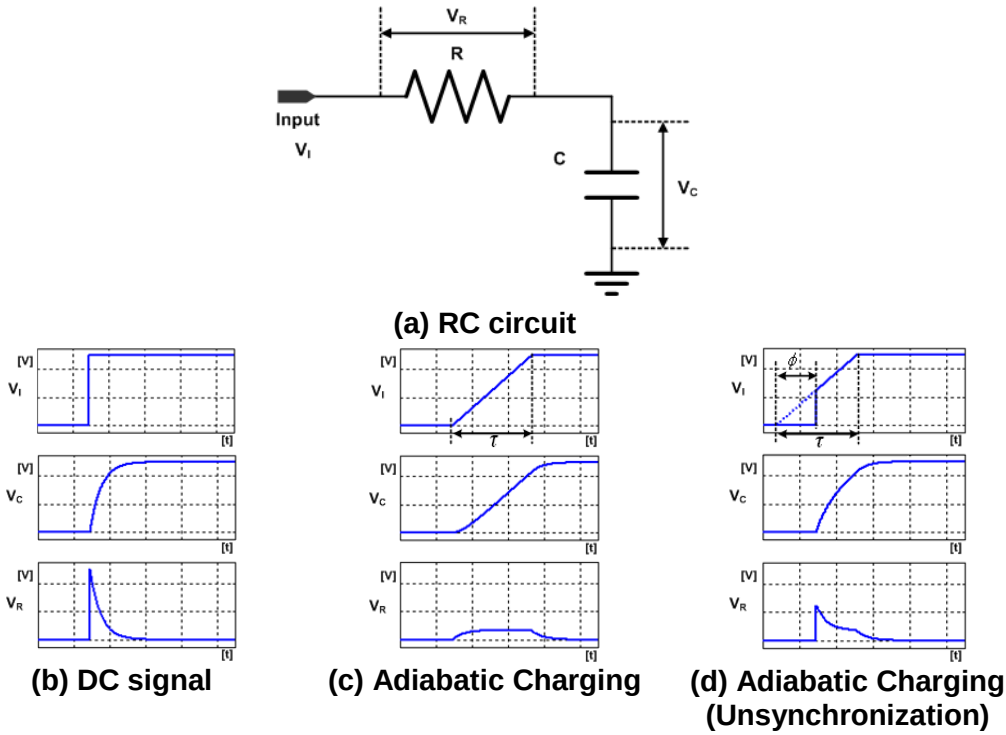


Figure 3. Operation of the RC circuit

Figure 3 shows the operations at a normal RC circuit with a DC signal, adiabatic charging, and unsynchronization. The input signal $v_I(t)$, voltage drop of the resistance

$v_R(t)$ and power dissipation $P_R(t)$ in Fig. 3(a) are expressed in equation (1), (2), and (3), respectively, where τ is the rising time of input, ϕ is unsynchronized period and $u(t)$ is the unit step function [11-16].

$$v_I(t) = \frac{V_I}{\tau}(t+\phi)[u(t) - u(t-(\tau-\phi))] + V_I[u(t-(\tau-\phi))] \tag{1}$$

$$v_R(t) = \frac{RCV_I}{\tau}\left[\left(1-e^{-\frac{t}{CR}}\right) - \left(1-e^{-\frac{t-(\tau-\phi)}{CR}}\right)u(t-(\tau-\phi))\right] + \frac{V_I\phi}{\tau}e^{-\frac{t}{CR}} \tag{2}$$

$$P_R(t) = R\left[\frac{CV_I}{\tau}\left[\left(1-e^{-\frac{t}{CR}}\right) - \left(1-e^{-\frac{t-(\tau-\phi)}{CR}}\right)u(t-(\tau-\phi))\right] + \frac{V_I\phi}{\tau R}e^{-\frac{t}{CR}}\right]^2 \tag{3}$$

In the case of the DC signal ($\tau = \phi$) at the input signal, the energy dissipation occurred at the load R until the end of charging at the load C, as shown in Fig. 3(b). In this case, $v_I(t)$, $v_R(t)$, and $P_R(t)$ at Fig. 3(a) are

$$v_I(t) = V_I[u(t)], \tag{4}$$

$$v_R(t) = V_I e^{-\frac{t}{CR}}, \tag{5}$$

$$P_R(t) = \frac{V_I^2}{R}e^{-\frac{2t}{CR}}. \tag{6}$$

On the other hand, in the case of the AC signal ($\phi = 0$) as the input signal, adiabatic charging and little power dissipation are shown in Fig. 3(c). In this case, $v_I(t)$, $v_R(t)$, and $P_R(t)$ are

$$v_I(t) = \frac{V_I}{\tau}t[u(t) - u(t-\tau)] + V_I[u(t-\tau)], \tag{7}$$

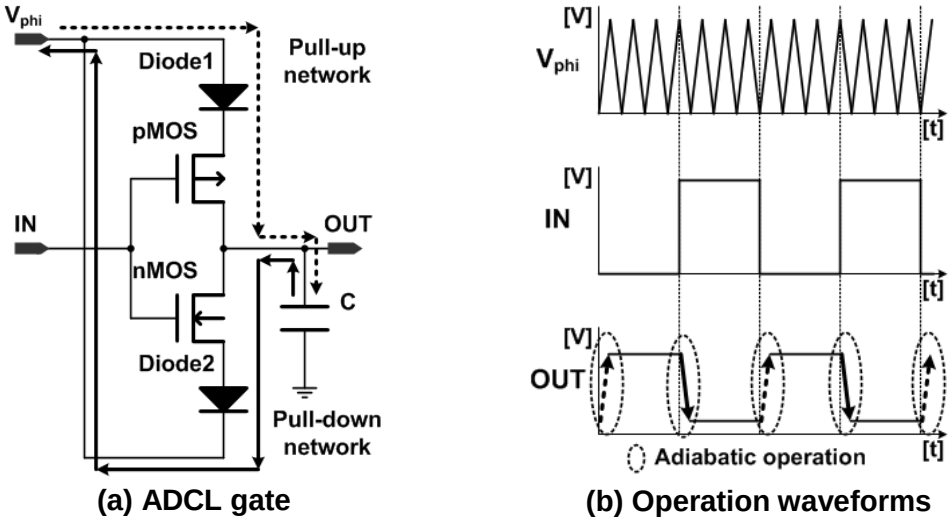
$$v_R(t) = \frac{RCV_I}{\tau}\left[\left(1-e^{-\frac{t}{CR}}\right) - \left(1-e^{-\frac{t-\tau}{CR}}\right)u(t-\tau)\right], \tag{8}$$

$$P_R(t) = R\left[\frac{CV_I}{\tau}\left[\left(1-e^{-\frac{t}{CR}}\right) - \left(1-e^{-\frac{t-\tau}{CR}}\right)u(t-\tau)\right]\right]^2. \tag{9}$$

The region of adiabatic charging decreased with increasing ϕ of the AC signal, as shown in Fig. 3(d). In this case, $v_I(t)$, $v_R(t)$, and $P_R(t)$ are expressed as equation (1), (2), and (3) respectively [15].

2.2. Adiabatic Dynamic CMOS Logic (ADCL)

The ADCL gate consists of the CMOS logic, AC power and two diodes for the adiabatic charging as it is applied to the CMOS logic. Figure 4 shows an ADCL inverter gate. In this circuit, because the output voltage of the ADCL gate is synchronized with the power supply, V_{phi}, the operating speed of the ADCL circuits is determined by the frequency of V_{phi}. Figure 4(a) and (b) show the principle of the ADCL inverter [12-16].



(a) ADCL gate **(b) Operation waveforms**

Figure 4. Principles of ADCL Inverter

Principle (I) : Pull-up network

In Figure 4(a), pMOS and nMOS are on and off, respectively. In this case, the supply current path is generated and the load capacitor C is charged adiabatically by V_{phi}. The high level is then kept with diode1.

Principle (II) : Pull-down network

Under this condition, pMOS and nMOS are off and on, respectively. In this case, the current path is generated, as shown in Fig. 4(a) and the charge in C is discharged adiabatically into V_{phi}.

Consequently, the ADCL inverter works in the adiabatic mode, as shown in Fig 4(b). On the other hand, if the difference between V_{phi} and the voltage across C is large, adiabatic operation will not be established and power will be largely dissipated. The ADCL operates the adiabatic charging whenever logic level of the output is changed from high level to low and vice versa. Furthermore, the charge can be reused because the charge reverts to the power source at the discharge of load C.

3. Optimization of Control Block of Clock Cut-off Circuit

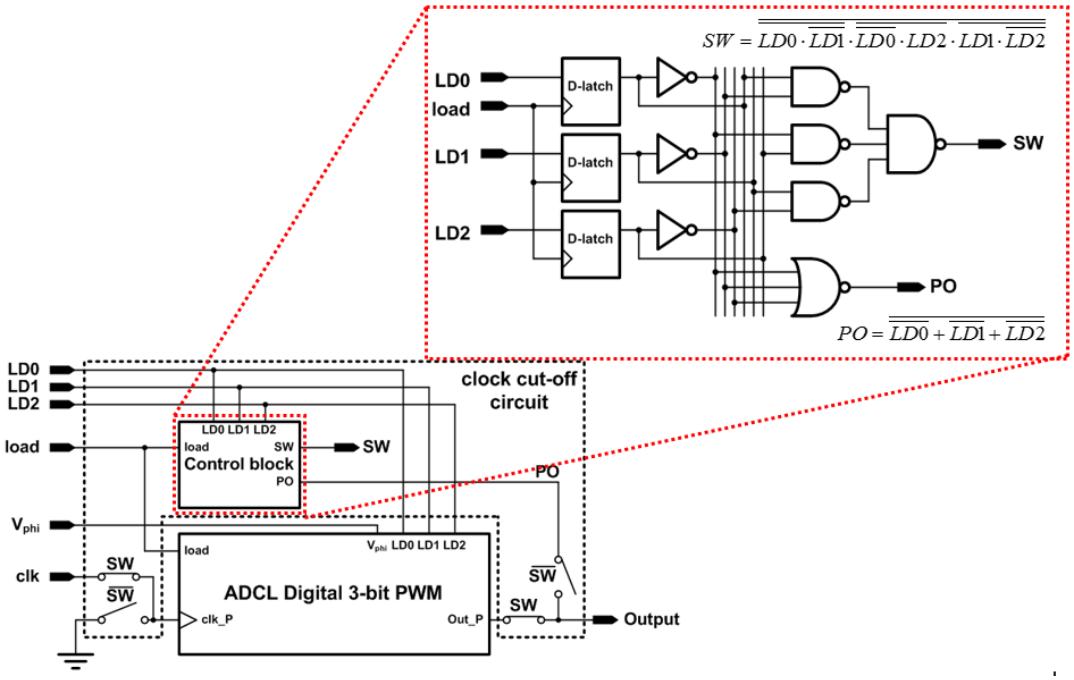


Figure 5. Miniaturized Control Block of the Clock Cut-off Circuit

The PWM is normally used for the dimming circuit. The ADCL digital 3-bit PWM is designed using ADCL gates. When input bits (LD0, LD1, LD2) are LLH, LHH, the output pulse width of PWM is about 33.3 %, 66.6 % and characteristics of ADCL, the adiabatic charging/discharge are confirmed respectively. The power consumption of ADCL digital PWM is lower than it of CMOS digital PWM through adiabatic charging/discharging operation. However, unnecessary operation at both dimming 0 % and 100 % of ADCL digital PWM output results in power consumption. The designed clock cut-off circuit pauses the D-ffs after cutting off the clock at both input-bit LLL (0 %) and HHH (100 %), and performs normal operation of the D-ffs at other case.

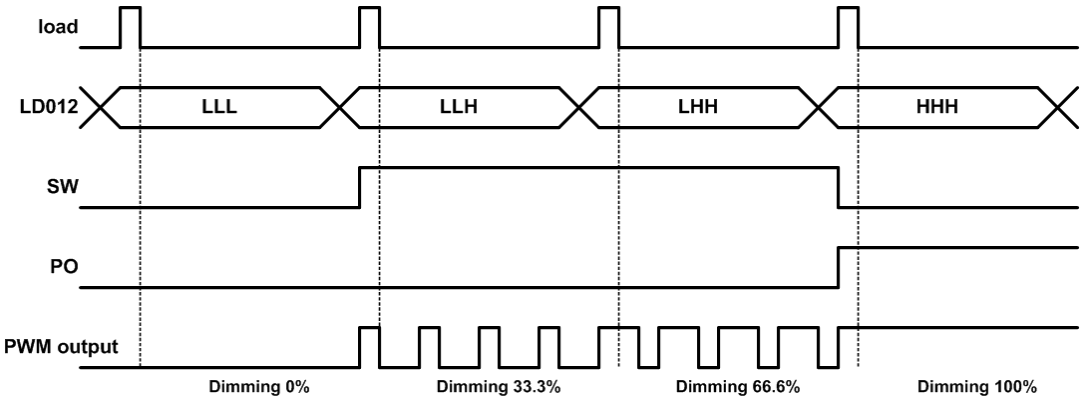


Figure 6. Timing Chart of the Digital 3-bit PWM

Figure 5 shows the optimized control block of the clock cut-off circuit using De Morgan's laws with ADCL digital 3-bit PWM. Figure 6 shows the timing chart and table 1 lists the truth table of the proposed clock cut-off circuit with ADCL digital 3-bit PWM. The PWM is reset, if the load is at a high level. The LD0, LD1, and LD2 can control the output pulse width. For example the output pulse width will be 33.3 % if LD0 = L, LD1 = L and LD2 = H (LLH), and the output pulse width will be 66.6% if LD0 = L, LD1 = H and LD2 = H (LHH). This output pulse width of the PWM can control the dimming of OLED. The up-level D-latch was used to output the logic level of the SW and PO by the input-bit if the load is reset but to remain at the logic level of the pre-state if the load is set.

Table 1. Truth Table of Proposed Clock Cut-off Circuit

load	LD0	LD1	LD2	SW	PO	clk_P	Output
H	L	L	L	L	L	L	L (PO)
H	L	L	H	H	L	clk	Out_P
H	L	H	H	H	L	clk	Out_P
H	H	H	H	L	H	L	H (PO)
L	Don't care	Don't care	Don't care	X_{n-1}	X_{n-1}	X_{n-1}	X_{n-1}

In reference [15], Boolean algebras, SW and PO of control block are

$$SW = LD0 \cdot \overline{LD1} + \overline{LD0} \cdot LD2 + LD1 \cdot \overline{LD2}, \quad (10)$$

$$PO = LD0 \cdot LD1 \cdot LD2 . \quad (11)$$

In this paper, SW, PO of control block are optimized using De Morgan's laws as follows ;

$$SW = \overline{\overline{LD0 \cdot \overline{LD1}} \cdot \overline{\overline{LD0} \cdot LD2} \cdot \overline{LD1 \cdot \overline{LD2}}}, \quad (12)$$

$$PO = \overline{\overline{LD0} + \overline{LD1} + \overline{LD2}} . \quad (13)$$

Table 2 lists the elements. Compared to the control block of Ref. [15], 10 transistors were reduced.

Table 2. Comparison of the Elements

Ref. [15]			This paper		
Logic gate		Tr.(ea)	Logic gate		Tr.(ea)
D-latch	3ea	54	D-latch	3ea	54
Inv.	3ea	6	Inv.	3ea	6
AND3	1ea	8	NOR3	1ea	6
AND	3ea	18	NAND	3ea	12
OR3	1ea	8	NAND3	1ea	6
Total		94	Total		84

Figure 7 shows layout of the optimized control block using Rohm 0.18μm standard CMOS model. Layout area of the optimized control block is 2,198.0um^2, which decreased by 9.0 % compared to that of the control block of Ref. [15].

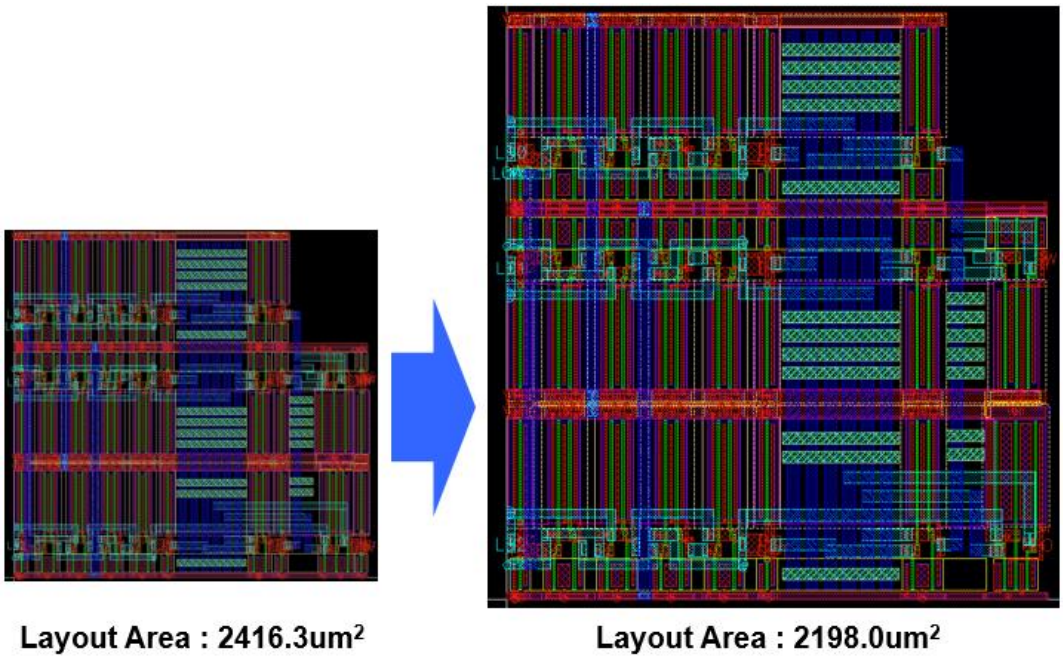


Figure 7. Layout of Optimized Control Block

4. Simulation Results

The optimized clock cut-off circuit was simulated using hspice with Rohm 0.18µm standard CMOS model. Figure 8 shows the simulation results. The post-simulation confirmed that the clk_P is low level at both input-bits LLL and HHH because the SW is low level, and cutting off the clock. Moreover, the Output is a low level at input-bit LLL and a high level at input-bit HHH. Simulation results match the truth table of the proposed clock cut-off circuit.

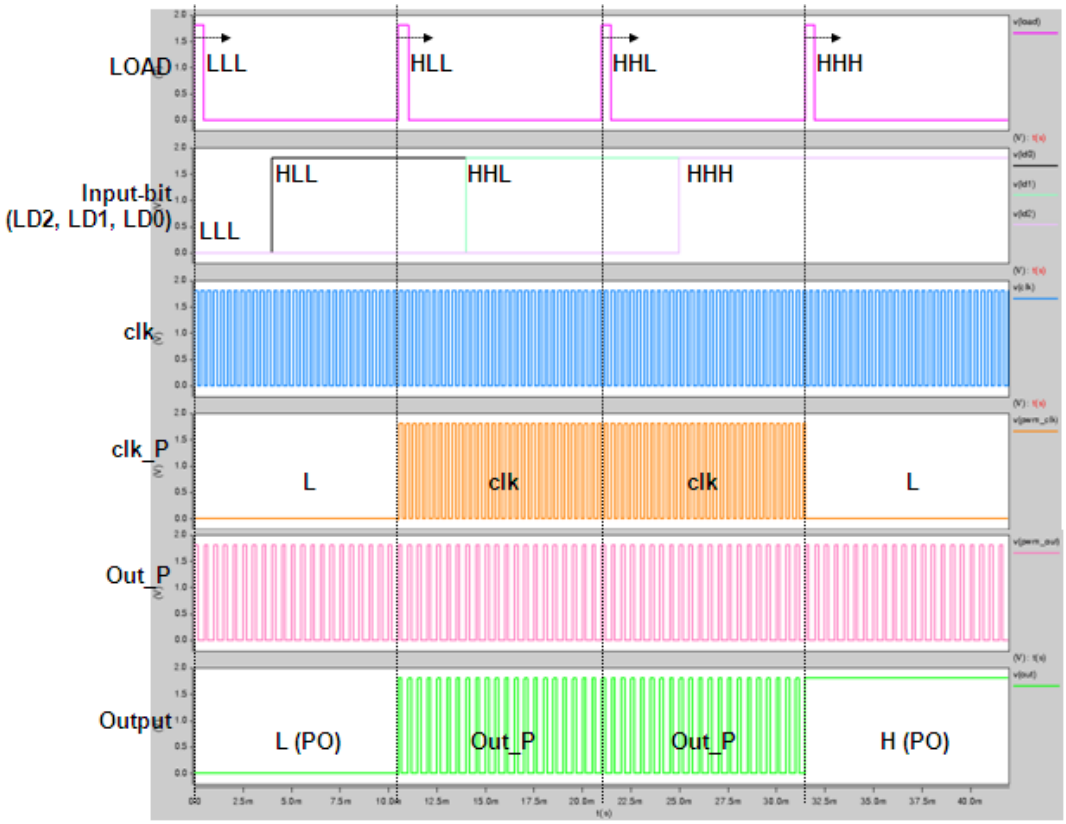


Figure 8. Post-simulation Results of the Clock Cut-off Circuit

In order to confirm operation of total ADCL PWM with the proposed clock cut-off circuit, it and the ADCL 3-bit PWM are simulated using a Rohm 0.18µm standard CMOS model and hspice post-simulation. The DC power, AC power and clock were 1.8 V, 33 kHz sine wave, 3 kHz square wave respectively. Figure 9 shows the simulation results. The simulation confirmed that the input clock of the ADCL D-ffs is cut off because the SW is high at both input-bits LLL and HHH. And the pulse width of the PWM output becomes 100 % because the PO is a high level at input-bit HHH. Moreover, adiabatic charge/discharge are confirmed other case, as shown Fig. 9①②.

5. Conclusion

In this paper, the optimized control block of the clock cut-off circuit was designed using De Morgan's laws with ADCL digital 3-bit PWM. Layout area of miniaturized control block was 9.0 % lower than that of the control block of Ref. [15], because 10 transistors were reduced using a Rohm 0.18µm standard CMOS model. The operation of control block is confirmed by computer post-simulation. The designed clock cut-off

circuit pauses the D-ffs after cutting off the clock at both 0 % and 100 % pulse width of PWM output.

This shows the potential of the optimized ADCL digital PWM in future low-power OLED dimming systems. Moreover, at the Smart MIRAI House, the research results for the living environment of the near future are demonstrated and correlation between big data analysis and deep sleep are verified.

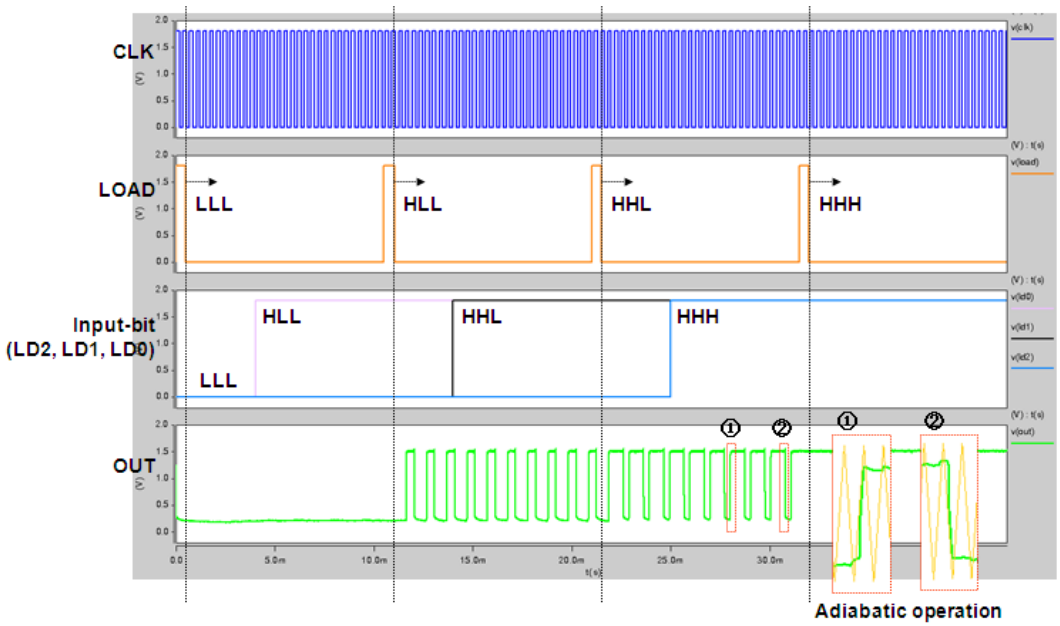


Figure 9. Post-simulation Results of ADCL 3-bit PWM with the Clock Cut-off Circuit

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Michio Yokoyama was born in Yamagata, Japan, on March 1st, 1967. He received his B.E. degree in electrical engineering from Yamagata University in 1989, and his M.E. degree in electrical and communication engineering and Ph.D degree in electronic engineering from Tohoku University in 1991 and 1994, respectively. From 1994 to 2001, he joined the Research Institute of Electrical Communication (RIEC), Tohoku University, Sendai, Japan, where he was engaged in research on the design and development of RF-CMOS devices, such as power amplifier modules for digital cellular phone systems. Since 2001, he has joined Yamagata University, Yonezawa, Japan, and was engaged in the development of RF-CMOS circuits and RF system packages. He is a member of JIEP, IMAPS, JSAP, IEICE, and IEEJ.