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A New Quadratic Boost Converter with Voltage Multiplier Cell: an Analysis and Assessment

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Abstract

A new topology of high gain DC-DC quadratic boost converter with voltage multiplier cell (VMC) is introduced in this paper. The proposed VMC technique is derived from the traditional quadratic boost converter, which has an advantage with high voltage gain and stress across the semiconductor devices are lower than the output voltage. To validate efficacy of the proposed method simulation has been performed in Mat lab Simulink software to compare the voltage gain of proposed method with others five modified boost converters. The input voltage of proposed converter and other topologies are same 10VDC but the output voltage of proposed converter is much higher than others converters which are discussed in this paper.

Keywords: *Quadratic boost converter, Voltage multiplier cell, high voltage gain, voltage stress*

1. Introduction

Usually renewable energy technologies RETs, particularly solar photovoltaic PV system demand high step up voltage conversion. Because of solar PV fluctuated output voltage under non-uniform solar conditions DC-DC boost converter has attracted the intention of research in recent year [1-4]. Therefore, different types of DC-DC converter are being used to attain the required and stable output voltage. To mitigate the aforesaid disadvantage of conventional boost converter, so far many solutions are proposed and successfully implemented to get the high voltage step up ratio, such as forward or fly back converter is discussed in [5]. The disadvantage of this type of converter is transformers which increase the losses, cost and size [6]. In [7] conventional quadratic boost converter is proposed which use only one switch for voltage conversion ratio, the voltage gain of conventional quadratic boost converter is not much high and they present voltage and current overstress when the conversion ratio is high. In [8] tapping Boost converter with coupled many inductors in presented to achieve the high step up voltage by adjusting turn ration. The disadvantage of this type of converter is difficult to couple inductors and leakage inductance occurred, the problems overshoot the large voltages [9].

The non-insulated converter has an advantage over insulated converters, the cost of non-insulated converter is lower than insulated converter and efficiency is high. The disadvantage of non-insulated converter is the input current and output voltage is high, at this situation the switches need to be sized according to input current and output voltage for high voltage gain. The sizing of switching is expensive that's why at some point insulated converter are better option [10]. In [13-15] cascaded converter for PV and fuel cell is presented, but the disadvantage of cascaded converter is its high cost and also compromise on efficiency.

A new topology of quadratic boost converter with voltage multiplier cell (VMC) is introduced in this article; the advantage of the proposed topology over the conventional quadratic boost converter and other modified converters which are presented in this paper has high voltage gain, and the voltage stress across the switches is lower than output

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voltage. According to conventional quadratic boost converter the voltage stress across the switch S is equal to $V_{S\text{-}stress}=V_0$ and the voltage stress of proposed the converter is $V_{S\text{-}stress}=V_{C2}$ which are lower than output voltage, similarly stress across the diode D_3 in conventional quadratic boost converter is $V_{D3}= -V_0$ and stress across the diode in the proposed topology is$V_{D3}= -V_{C2}$.The proposed (VMC) topology shows an enhancement of the high voltage gain over the some topologies presented in [1-11-12-14-16] with same duty ratio at D=0.6.

2. Traditional Boost Converter

The traditional boost converter circuit diagram is depicted in Figure-1, which is mostly used for step up voltage in conventional applications [11]. The main disadvantage of this type of converter is for high step up conversion need high duty ratio, which causes the difficulties for switching frequency because of limitation of OFF time of semiconductor switch.

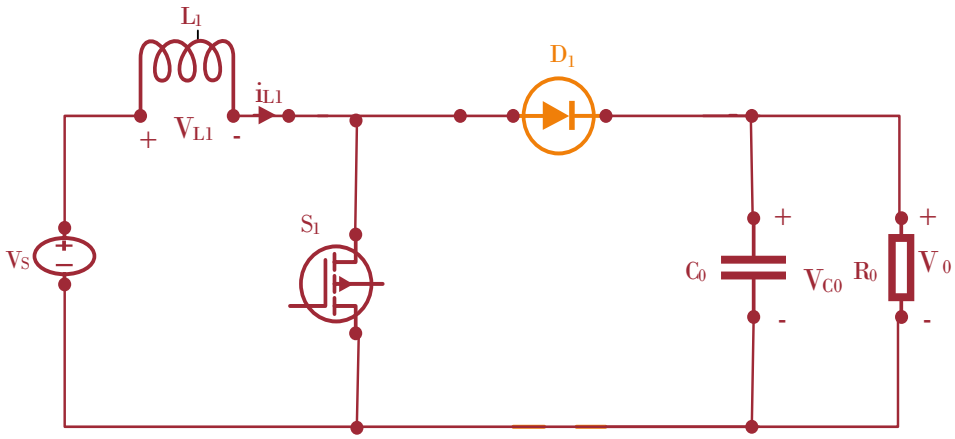

Figure 1. Traditional Boost Converter

Voltage gain of traditional Boost converter is obtained by (1):

$$M = \frac{V_0}{V_s} = \frac{1}{2(1-D)^2}$$

3. A Boost Converter with Voltage Extension Cell

In Figure-2 boost converter with extension cell module is depicted. It contains two additional switches (Sa-S1), diode (Da) and capacitor (C1). This converter is derived from traditional boost converter; the advantage of this converter over traditional boost converter has high voltage gain [1].

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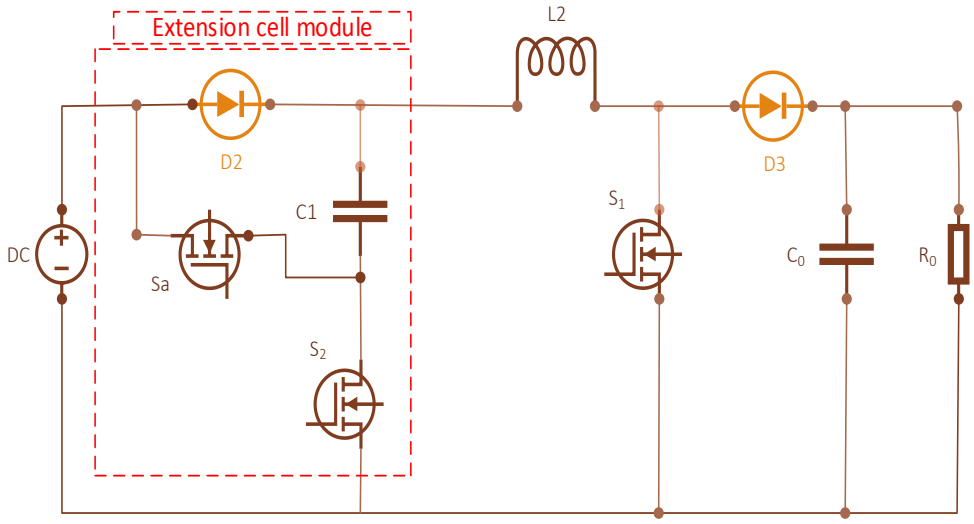

Figure 2. Boost Converter with Extension Cell Module

The operation of this converter work with fixed switching frequency 100 kHz and the switching period is T_s. The semiconductor switches S_a,S_1 and S_2 turn ON and OFF with two PWM signals. S_2 and S_1 are operated at one PWM signal and the S_a is operated by 2nd PWM signal, which is the inverse of 1st PWM.

The voltage gain of this converter is,

$$M = \frac{V_0}{V_s} = \frac{2 - D}{1 - D}$$

4. Boost Converter with Voltage-Lift Cell

Boost converter with voltage-lift-cell is shown in Figure 3; the advantage of voltage lift cell over traditional boost converter is high voltage gain with decreased stress across the switch. As compared with traditional boost converter, two additional capacitor and two diodes are employed in the voltage-lift cell as depicted in Figure 3.

The operation of boost converter with voltage lift cell work in continuous conduction mode (CCM), in 1st state when switch S is ON at this time input voltage source delivered supply voltage to inductor L_1 at the same time capacitor C_2 and C_1 are in charging mode with supply voltage. When switch S is in OFF mode inductor L delivered the stored energy to capacitor C_1 and the other capacitor C_2 in this stage is in discharging mode to load respectively.

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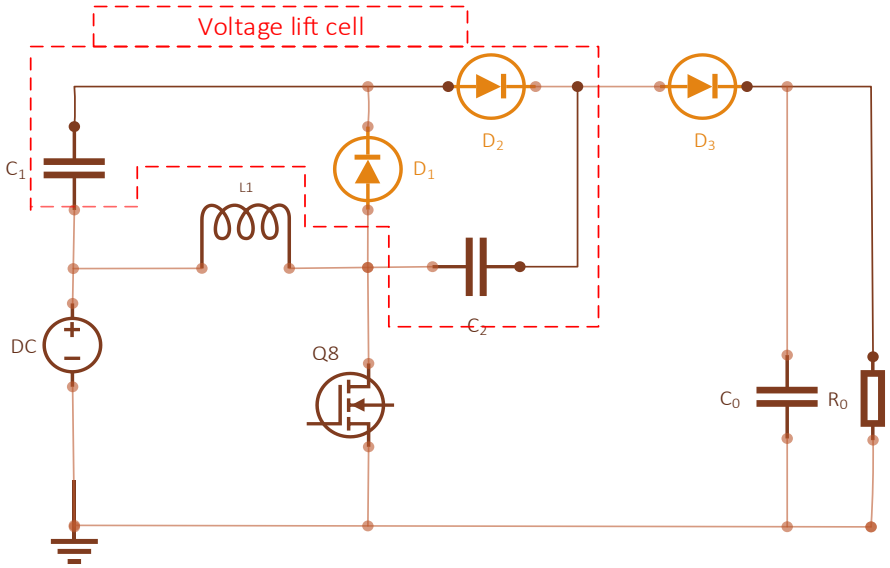

Figure 3. Boost Converter with Voltage Lift Cell

The voltage gain is

$$M = \frac{V_0}{V_s} = \frac{2}{1 - D}$$

Voltage gain of this converter is higher than the traditional boost converter and have advantage reduces losses over semiconductor devices which increase the life time of converter [12].

5. Traditional Quadratic Boost Converter

Traditional quadratic boost converter circuit is depicted in Figure 4. Its consist 1 switch S, 2 inductors L_1,L_2 ,3 diodes D_1,D_2,D_0 and two capacitors C_1,C_0 respectively. This quadratic boost converter can enhance the high voltage gain work with only 1 switch S [14]. The voltages stress on switch S is equal to output voltage. This converter can produce over voltage and current overstress when voltage gain is high.

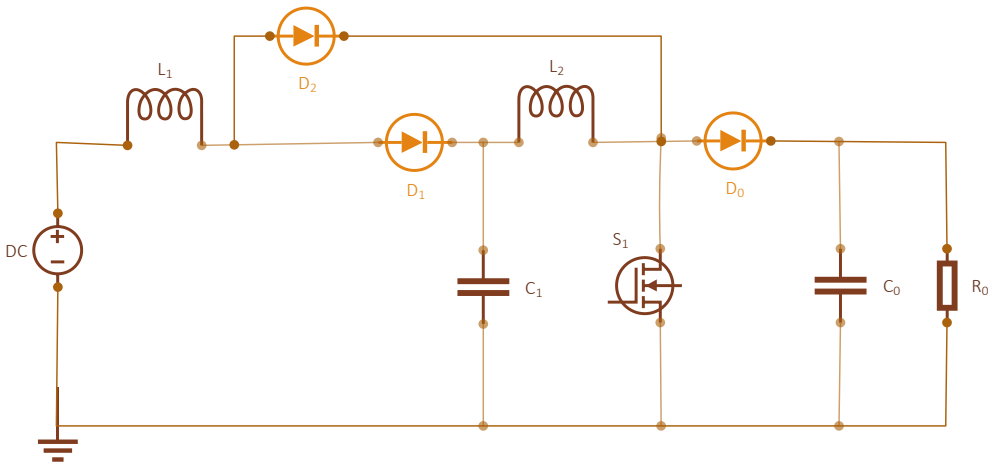

Figure-4 Traditional Quadratic Boost Converter

The voltage gain is

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$$M = \frac{V_0}{V_s} = \frac{1}{(1-D)^2}$$

The main disadvantage of traditional quadratic boost converter is step-up switching structure, which is not suitable because there is no energy storing elements.

6. Three-level Quadratic Boost Converter

Three level quadratic boost converter derived from traditional quadratic boost which depicted in figure-5. The advantage of this converter is two switches and two output capacitors which decree the voltage stress across the switches and result output voltage is balanced. The current conducted by switches in this converter is some of currents of both inductors.

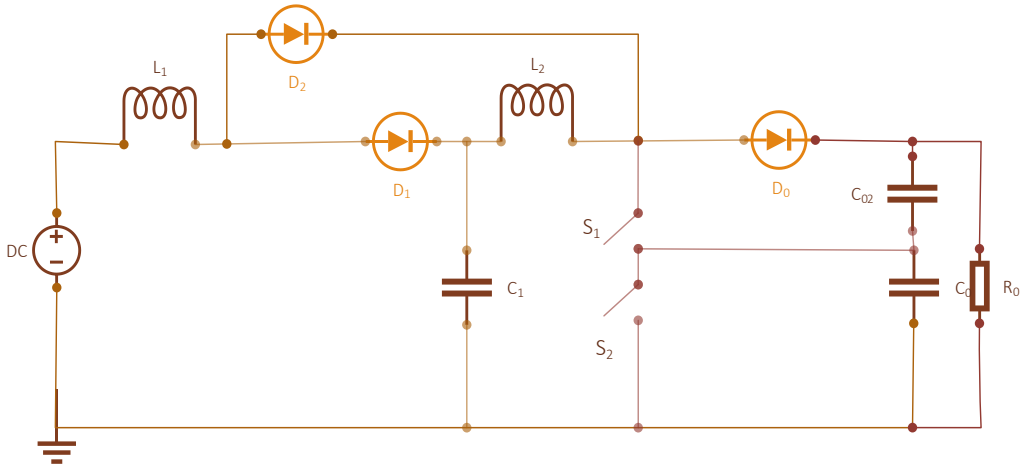

Figure 5. Modified Quadratic Boost Converter

The main disadvantage of this topology is its transfer function which increases the complexity, control and cost [13]. The voltage gain of this converter is half of conventional quadratic boost converter.

The voltage gain equation given below;

$$M = \frac{V_0}{V_s} = \frac{1}{2(1-D)^2}$$

7. Proposed Topology

The proposed quadratic boost converter with voltage multiplier (VMC) cell is shown in figure-6. This topology is derived from quadratic boost converter, which consist two additional diodes (D_3-D_4), capacitors (C_2-C_3) and inductor L_3 which called Voltage multiplier cell (VMC). The main advantage of the proposed topology is its high voltage gain and losses across the semiconductor devices are lower than the output voltage as presented in literature.

7.1. Working Principle of the Proposed Converter

The proposed topology has two switching state in 1 PWM signal as shown in Figure 7(a&b). The steady state waveform shows below in Figure 8.

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7.2. State-I:

When switch S is ON as depicted in Figure 7(a). In this state D_2, D_3, D_4 remain OFF, and diode D_1 is in ON state. DC input voltage source V_s provides energy to inductor L_1 and at same time capacitor C_1 deliver stored energy to inductor L_2. During this stage capacitor C_1 and C_2 works in series, the resultant output voltage is sum of both capacitors $Vc_2+V_{c3}=2_{vc}$, capacitor's stored energy delivered to L_3, and the output capacitor during this time is in charging mode. In 1st stage all the inductors current i_{L1}, i_{L2} and i_{L3} linearly increase.

7.3. State-II:

When switch S and diode D_1 is OFF as shown in Figure 7(b), in this stage inductor L_1 deliver stored energy to capacitor C_1, and the inductor L_2 deliver stored energy to capacitor C_1 and C_2 and load while inductor L_3 delivered stored energy to output. In this state inductors current i_{L1}, i_{L2} and i_{L3} linearly decrease. At this time all capacitors are in discharging mode to load.

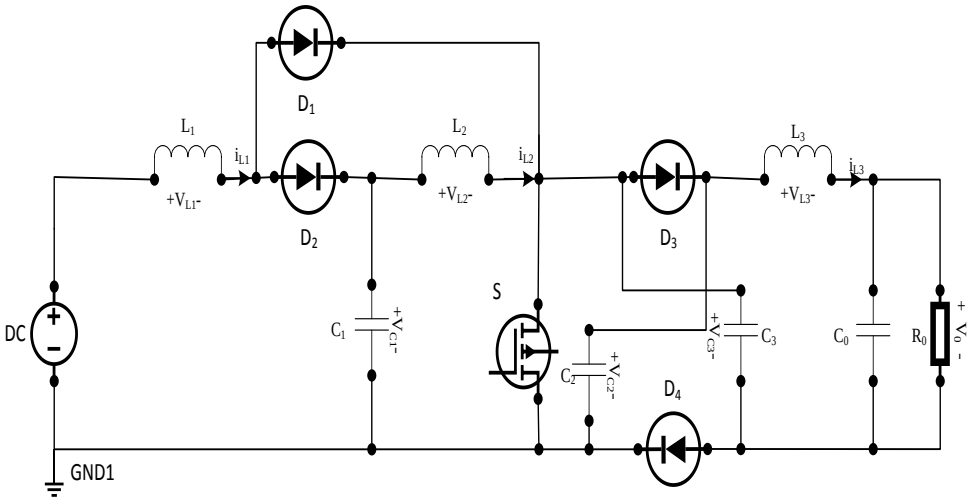
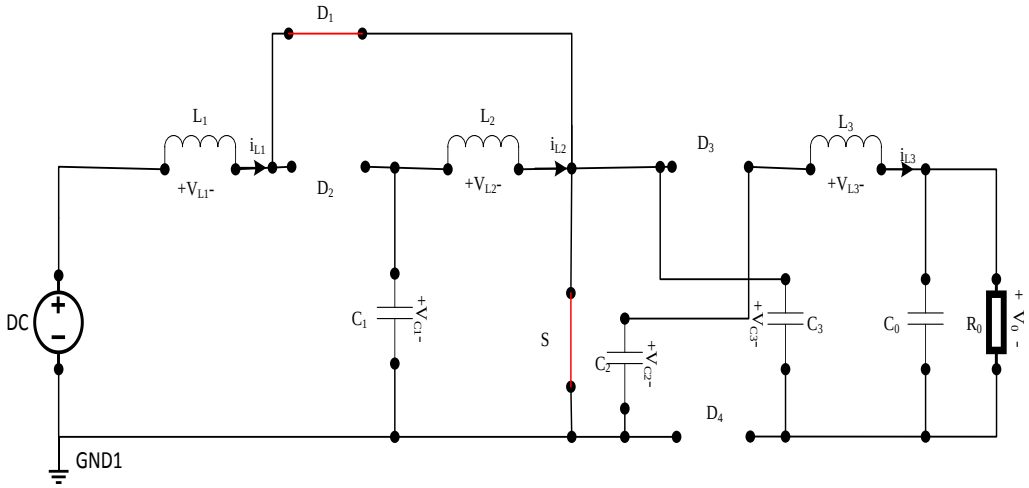


Figure 6. Proposed Converter



(a)

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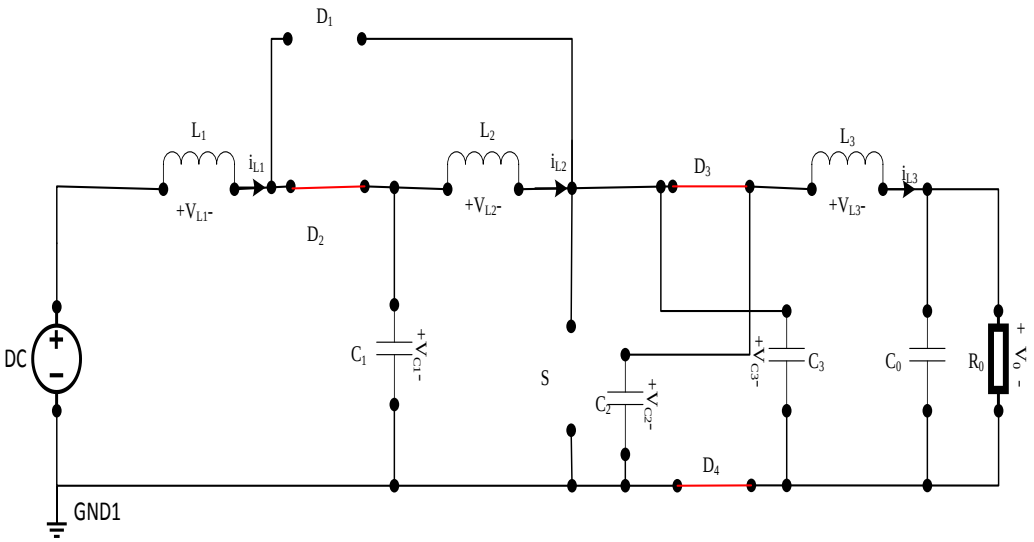

(b)

Figure 7. Switching State of Proposed Converter

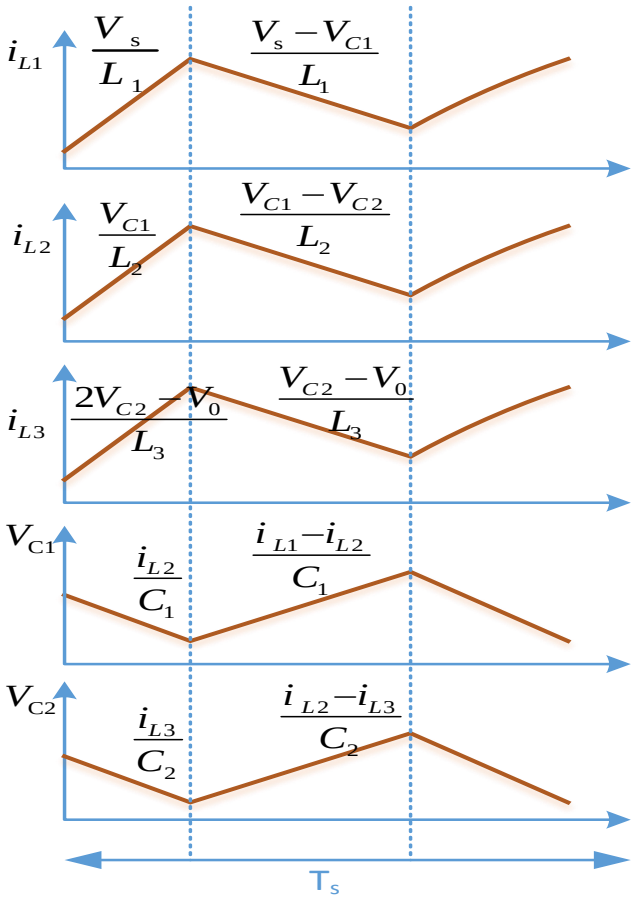

Figure 8. Steady State Waveforms

7.4. Steady State Analysis of the Proposed Converter

As it can be observed in Figure 7(a), when the switch S is ON during that stage diode D_1, D_3 and D_4 are in off mode. The state equation shows in below.

$$\left\{\begin{array}{l} V_{L1} = V_S \\ V_{L2} = V_{C1} \\ V_{L3} = 2vc - V_0 \end{array}\right\} \quad (1)$$

At stage-II we can see figure 7(b), at this stage when switch S and diode D_2 are in OFF mode. The state equation derived below.

$$\left\{\begin{array}{l} V_{L1} = V_S - V_{C1} \\ V_{L2} = V_{C1} - V_{C2} \\ V_{L3} = V_{C2} - V_0 \end{array}\right\} \quad (2)$$

7.5. DC Conversion Ratio

Using the principle of inductor volt second balance at inductor L_1 we get:

$$DV_s + (1-D)(V_s - V_{c1}) \quad (3)$$

After solving the equation (3) we get,

$$V_s = V_{C1}(1-D) \quad (4)$$

$$V_{C1} = \frac{V_S}{(1-D)} \quad (5)$$

Again using inductor volt balance at inductor L_2

$$DV_{C1} + (1-D)(V_{c1} - V_{c2}) \quad (6)$$

After solving this equation (6) we get,

$$V_{c2} = \frac{V_{C1}}{(1-D)} \quad (7)$$

After put the V_{c1} Value we get,

$$V_{c2} = \frac{V_S}{(1-D)^2} \quad (8)$$

Using inductor volt balance at inductor L_3,

$$D(2V_C - V_0) + (1-D)(V_{c2} - V_0) \quad (9)$$

After solving the equation (9) we get,

$$V_0 = V_{C2}(1+D) \quad (10)$$

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Static gain of proposed topology is,

$$M = \frac{V_0}{V_S} = \frac{1 + D}{(1 - D)^2} \tag{11}$$

7.6. Voltage Stress Across the Semiconductor Devices

In state-I the voltage stress across the semiconductor diodes is as below,

$$V_{D1-stress} = \frac{(1 - D)V_0}{1 + D} \tag{12}$$

$$V_{D3\text{-}stress} = -V_{c2} \tag{13}$$

Similarly in state-II the voltage stress of semiconductor devices are,

$$V_{s-stress} = V_{C2} \tag{14}$$

$$V_{D2\text{-}sress} = \frac{D_{V0}}{1 + D} \tag{15}$$

7.7. Simulation Results and Discussion

To validate the performance of the proposed converter and others converter which are presented to compare with the proposed topology simulation are done in MATLAB/ Simulink software according to the parameters given in Table 1. The proposed topology results shows in Figure 9. For comparison other converters output voltages shown in Figure 10.

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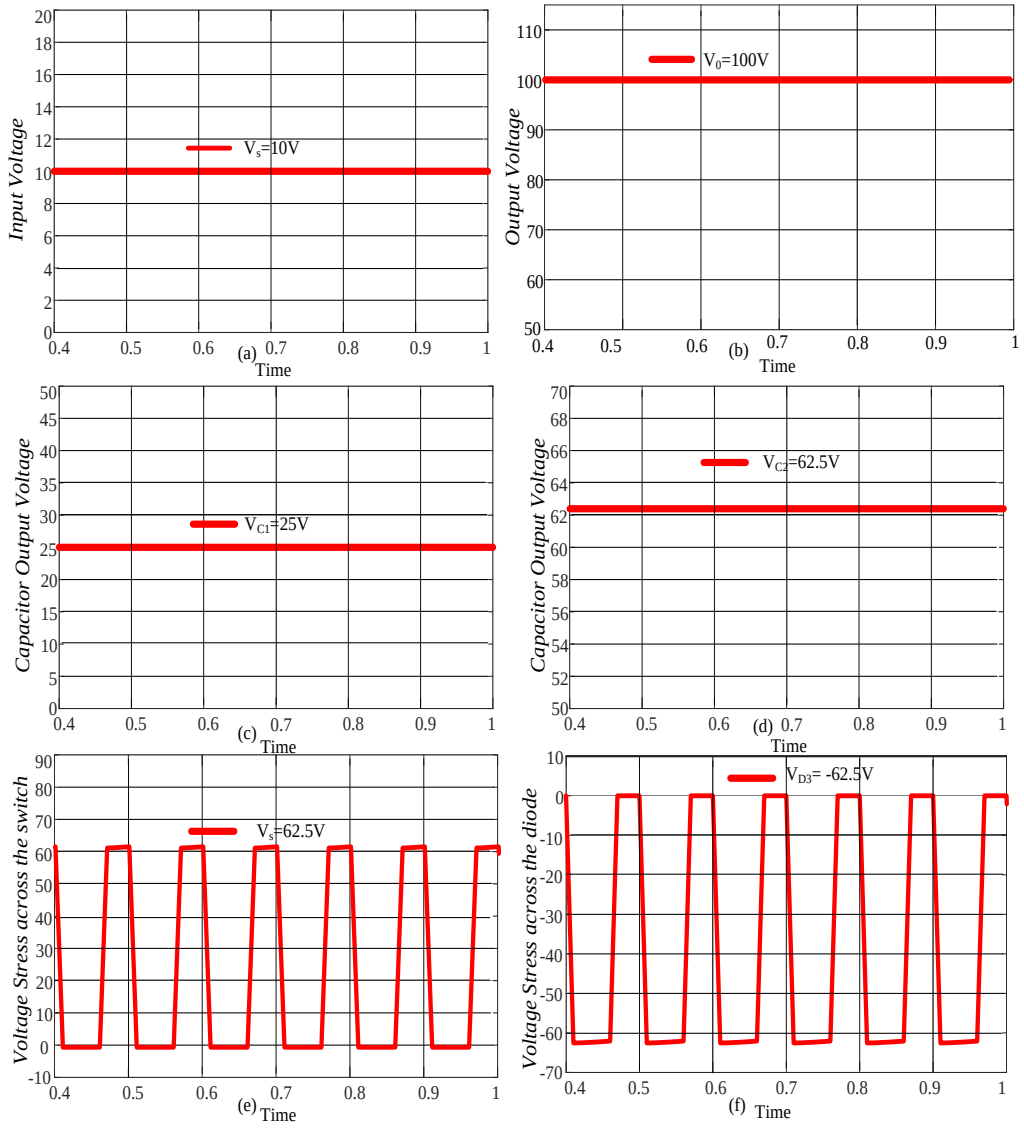

Figure 9. Simulation Results of Proposed Converter. (a) Input Voltage (V_S), (b) Output Voltage (V_0), (c & d) Capacitors Voltage (V_{c1}, V_{c2}), (e) Voltages Stress, (V_{s1}) and (f) Voltage Stress V_{D3} of Diode D_3

Table 1. Component List of the Proposed Topology

Name of parameter	Symbol	Value
Input Voltage	V_S	10V
Output Voltage	V_O	100V
Load Resistance	R_L	100Ω
Frequency	F_S	100kHz
Filter inductor/phase	L	200uH
Capacitors	C	10uF
Output capacitor	C_o	10uF
Duty ratio	D	0.6

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Table 2. Voltage Gain Comparison

	Topology Name	V_s	V_0	Voltage gain
1	Proposed topology	$10V_{DC}$	100V	10%
2	Conventional quadratic boost converter	$10V_{DC}$	62.5V	6.25%
3	Boost converter with voltage lift cell	$10V_{DC}$	50V	5%
4	Boost converter with extension cell	$10V_{DC}$	35V	3.5%
5	Three level quadratic boost converter	$10V_{DC}$	31.5	3.15%
6	Traditional boost converter	$10V_{DC}$	25V	2.5%

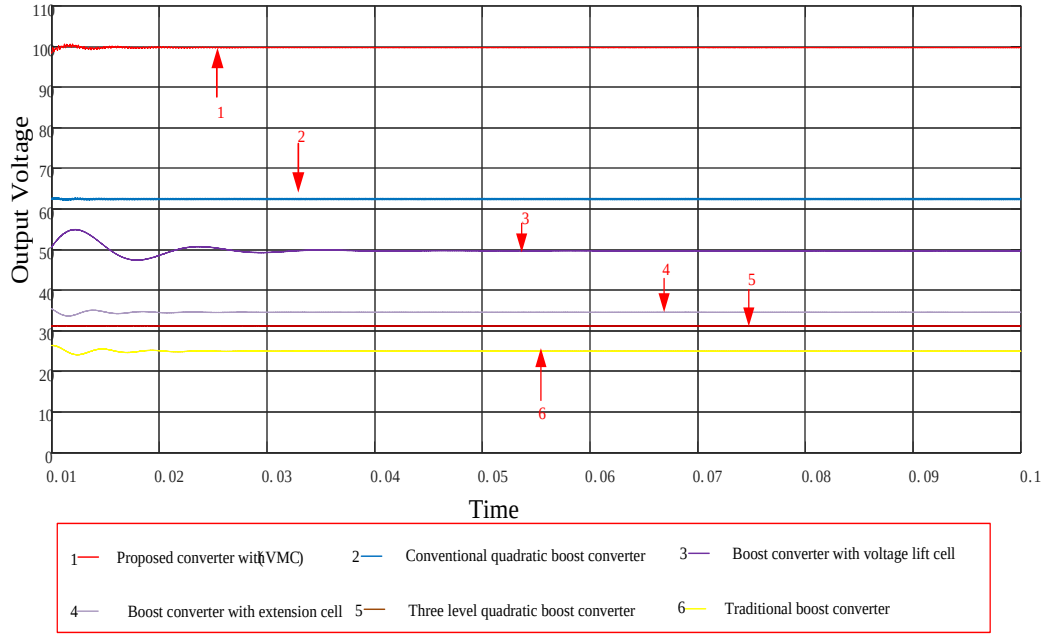

Figure 10. Comparison Simulation Results

Figure 10 is output voltages of proposed converter and other modified converters which are explained in Table 2. In Figure 9 authenticate the results and efficacy of the proposed quadratic boost converter with voltage multiplier cell (VMC) simulation results attain in Mat-lab Simulink software according to Table 1. Figure 9 (a) shows the waveforms of input voltage where we can see clearly the input voltage is 10V and in figure-9 (b) output voltage is nearly 100V which is very near according to voltage gain equation (11). It is prove that the proposed converter can achieve high voltage gain conversion ratio at the low input voltage 10V and output voltage is 100V. Figure-9(c) is waveforms of voltage stress $V_{s\text{-}stress}$ across the MOSFET switch S its clearly shows that the stress of switch is lower than the output voltage. In Figure-9(d) shows the waveforms of the voltage stress across the diode D_3, it's also clear from figure that the voltage stress of diode D_3 is also less than the output voltage when compare to conventional quadratic boost converter. Traditional quadratic boost converter has stresses across the switch and diode is equal to output voltage according to equations $V_{S\text{-}stress}=V_0$ and $V_{D3}= -V_0$. Figure 9(e, f) shows the waveforms of the capacitor output voltages across the capacitors C_1 and C_2. The output voltage of V_{C1} is 25V and the voltage across the capacitor C_2 is 62.5V which are same according to theoretical equations (5) and (7).

In Figure 10 simulation results carried out at same input voltage 10VDC is given to all the other 5 topologies and including the proposed topology with voltage multiplier cell. In figure-10 output voltages are given, where it can be observe that output voltage of the proposed topology is higher at 100VDC as compare to others output results. In figure-10 we can clearly see that if we use same parameters according to table-1 the proposed

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quadratic boost converter with voltage multiplier cell (VMC) is higher than other modified converters. The output voltages of proposed converter is 100V and the output voltage of traditional boost converter is 25V, traditional quadratic boost converter is 62.5V, boost converter with voltage lift cell is 50V, modified quadratic boost converter is 31.5V and boost converter with extension module is 35V.From simulation results it is clear that the proposed topology quadratic boost converter with voltage multiplier cell (VMC) has advantage over other converters which are presented in literature. This converter is very suitable where we need low input to high output voltages such as photovoltaic (PV) and other application *etc*.

8. Conclusion

A new topology of quadratic boost converter with voltage multiplier cell (VMC) is introduced in this paper. The operation principle of proposed converter and others converter discuss in details. The basic advantage of voltage multiplier cell over the traditional quadratic boost converter and others which discussed in literature has high voltage gain and stress across the switches is lower than the output voltage, which makes appropriate for application where we need the high step up conversion ratio. Furthermore to validate the proposed converter simulation results given in this paper with compression of others converter. Simulation results shows that the proposed converter has much higher voltage gain under the same duty ratio $D = 0.6$. The proposed quadratic boost converter with voltage multiplier cell (VMC) is very useful where we need low input to high output voltage such as photovoltaic (PV) and fuel cell (FC) *etc*.

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