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A Technique for Reducing Power Consumption in IC by Test Vector Ordering

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Abstract

This paper considers the issue of high power dissipation in test mode, and puts forward a novel technique based on the reordering of test vectors. This approach considers both the circuit structure and test set. The proposed approach uses a weight to quantify the relationship between the switching of each input and the internal switching activity, then reorder test set based on these weights. Results of experiments show reductions of the switching activity ranging from 17.06% to 69.22% during external test application.

Keywords*: power consumption ；Test vector ordering ；weighted hamming distance*

1. Introduction

With the development of the deep submicron and even ultra-deep sub-micron technology, the complexity of integrated circuits increases while area decreases, the frequency increases and power consumption become an important design parameter. Various low-power technologies are used in integrated circuit design, testing is an essential step in IC production, power consumption in test mode can reach twice the normal operating mode. When the tested circuit is during the testing, the power consumption is too large may cause damage to the chip, reduce the test reliability and the use of time or cause another other issues. Reducing the test consumption became an important goal in test design.

Test consumption can be divided into static and dynamic power consumption, test vectors sorting primarily affects dynamic power consumption. Dynamic power is caused by the state transitions of each gate in the circuit, the test vector sequence determines the dynamic power consumption when the test vector has been determined, and test vectors without optimization may make test consumption too large. Now there are two main methods to sort the test vectors, literature[1] proposes the method of Hamming distance reordering, which shows that the turnover number of the circuit internal state and input vectors of Hamming distance are directly proportional ， the smaller the Hamming distance is , the smaller the turnover number of the circuit internal state becomes, so it is obviously not comprehensive to use the Hamming distance between test vectors to optimize the test vector sequence to make test set minimum Hamming distance without the consideration of the internal structure of the circuit ; Literature [2] counts circuit internal status of all nodes when the circuit plus test vectors, then sorted the vectors according to these states, so that the turnover number of the circuit internal will be minimum, this method is effective in smaller circuits , but now circuits become more and more complicated, the number of internal nodes (n_{total}) is very large, for n test vectors, n * (n-1) times logic simulation[3] is necessary for circuits, and the time in calculating the distance between two vectors is n_{total} /n times as long as which in the Hamming distance, all of those causing the test time is too long.

This paper presents a new method to optimize sorting, which can optimize test vector ordering fast and effectively, it also can reduce the test consumption. The method

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determine the influence coefficient for each input according to the relationship between the internal circuit and the input port, which is used to decide the degree when the port changes influence the circuit activity, the coefficient is also used to correct the Hamming distance and get the weighted Hamming distance, so as to optimize test vector ordering. This sorting method comprises the following steps: first to determine the measured circuit test set, then get influence coefficient of each input according to the structure of the circuit and test set, calculation of the weighted Hamming distance, last using the greedy algorithm to optimize the sorting of test set.

In this paper, the various circuits of ISCA85、ISCA89 were experimented by the methods in literature [2] and this paper respectively, compare the time consuming and power with optimization between two methods, the result turns out that the method in this paper has an obvious advantage over which in literature [2], the optimization results express apparently and the time consuming is same.

2. Consumption Model

Now the power consumption of CMOS circuit mainly come from the consumption consumed by charging and discharging of the logic gate state changes in circuits, when the test vectors V_1 become V_2, the circuit power consumption P [4] is:

$$P = 0.5 \cdot (V_{dd}{}^2 / T) \cdot \sum_{i=1}^{N} \{[f_i(V_1) \oplus f_i(V_2)] \cdot fanout(i)\} = K \cdot P_0 \quad (1)$$

$$K = 0.5 \times (V_{dd}{}^2 / T)$$

$$P_0 = \sum_{i=1}^{N} \{[f_i(V_1) \oplus f_i(V_2)] \times fanout(i)\}$$

And V_{dd} represents for circuit supply voltage, T is the circuit's clock period, N represents for the number of gates in the circuit, i is one of the doors, $f_i(V_1)$, $f_i(V_2)$ respectively represent for Boolean value of gate i when V_1 and V_2 input, *fanout(i)* represents for the fan-out of gate i, where $0.5(V_{dd}{}^2/T)$ is constant and it has nothing to do with the input vector, it can be seen that the power P is proportional to P_0,and P_0 is the accumulated value of product when Boolean function value XOR all gates of circuit then multiplied by the number of fan-out of this gate when V_1 and V_2 are the input. Vector sorting with Optimization must be found to reduce P, thus the state of the gate in the circuit changes as little as possible.

3. Determining the Influence Coefficient

Take C17 circuit in ISCAS85 for example to illustrate the relationship between the input and the consumption.

3.1. Relationship Between the Circuit Structure and Circuit State Changes

Figure 1 represents the circuit structure of C17 with five inputs and six NAND gates, among them six gate status are related to input c, this means c input changes will cause changes mostly in the six gate status, on the contrary, a and e are related to only two gates, the changing of a and e can lead to two gate status changes at most. From the above we know that the circuit structure is related to power relations closer.

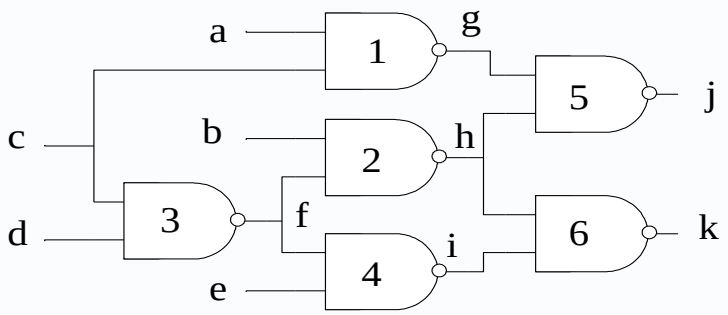

Figure 1. Circuit Configure of C17

3.2The Relationship between Tests Set and Circuit Status Changes.

We choose the No.1 NAND gate in C17 circuit to consider, if focused on the determined test set, the value of c is 0 in the two test vectors, then changing of a does not affect the state of g, on the contrary the value of C is 1, then a changes will affect the state of the G. It is showed that the changing of gate status is relevant to the value of input in test set. In summary, the change of circuit status and the structure of circuit and characteristics of the test sets are closely related, these relationships can be summed up the relationship between circuit activity and the input, using the influence coefficient to express size when the variation of the each input effect on activity, sorting test vector according to the coefficient and then began the quantitative analysis.

3.3. Determine the Influence Coefficient Which Input Impact on the Circuit Status Change

Consider a measured circuit with M original input s and n gates inside, gate G presents progression in the circuit, T is the fault test set, the V_i is the test vectors in the test set.

Definition: the influence coefficient which the number i original input impact on the status change of gate j is

$$W_{ij} = W_{ix} \times P(y = key) + W_{iy} \times P(x = key) \tag{2}$$

In the equation, x and y are the direct inputs of gate j, W_{ix} is the influence coefficient when original input i impact on the input x, $P(\ \ y=key)$ is the probability when y take the key value during the test procedure. FOR AND gate, key value is 1(because when the input of AND of gate is 1, another change in the input will lead to changes in the gate state); Similarly, the key value is 0 for OR gate; for NAND gate or the buffer gate, it only has one direct input, assuming that the input is x, then $W_{ij}=W_{ix}$.The multiple input gate is combined by the two input gate in the circuit and calculate the influence coefficient. The influence coefficient when original input impact on the gate which g=1 is equal to which another input of this gate take key value.

Definition: the influence coefficient when the number *i* original input effect on the whole circuit state changes is

$$W_i = \sum_{j=1}^{n} [\, fanout(j) \times W_{ij} \,] \tag{3}$$

The circuit as shown in Figure 2 as an example, test set T are {（10100）, （01000）, （01110）, （01010）, （00111）, （00100）}, the influence coefficient

which input b impact on circuit status change is composed of the influence coefficient by b on gate 2, 6, 7, 9, 10 status:

The influence coefficient W_{b2} of b on 2 is 1;

The influence coefficient W_{b6} of b on 6 is $W_{b2}\times p(h=1)$;

The influence coefficient W_{b7} of b on 7 is $W_{b2}\times p(j=0)$;

The influence coefficient W_{b9} of b on 9 is $W_{b6}\times p(i=1)$;

The influence coefficient W_{b10} of b on 10 is $W_{b7}\times p(k=0)$;

Among that $p(h=1)$、$p(j=0)$、$p(i=1)$、$p(k=0)$ is the probability when h、j、i、k take their own gate value respectively, the influence coefficient W_b of b impact on circuit status changes is:$2\times W_{b2}+1\times W_{b6}+2\times W_{b7}+1\times W_{b9}+1\times W_{b10}=5$,then calculate the influence coefficient which each original input changes influence on circuit state respectively[4].

4. Optimizing the Test sSet Order

Last chapter we assign influence coefficient to each of the original input, this value includes influence degree of the original input change impact on the whole circuit state variation, we use this value to correct the Hamming distance and make it become the weighted Hamming distance, then use ordering method which is similar with Hamming distance to optimize the ordering of test set. The specific steps are as follows:

Take the circuit in Figure 2 and the test set T as examples, definite the test vectors in T: V_1、V_2、V_3、V_4、V_5、V_6, the individual bits in the test vector corresponding to each original input. The Hamming distance between two vectors is the number of original input of different values, for example the Hamming distance between V_1 and V_2 is 3；First the Weighted Hamming distance take bitwise exclusive-OR of two vectors, and then multiply it with bitwise by the influence degree of the original input, and then summed, for example the Weighted Hamming distance between V_1 and V_2 is $W_a+W_b+W_c$. The method of sorting test set is similar to the Hamming distance sorting method, both of them using the Greedy algorithm.

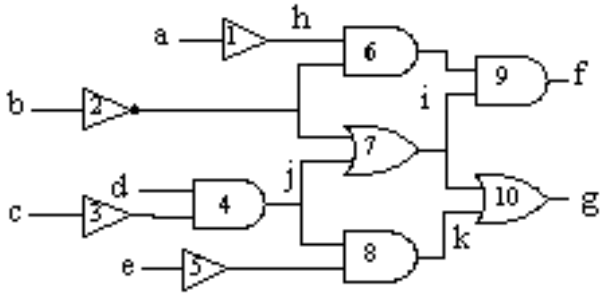

Figure 2. Circuit Under Test

The method of sorting test set is similar to the Hamming distance soring method, both of them using the Greedy algorithm, Figure 3 shows a flow chart[5] of sorting methods.

As shown in the flowchart, randomly select a vector as the first test vector after sorting, and then select the vector whose Weighted Hamming distance between itself and last vector is minimum as next vector. Adding backtracking in algorithm, if the two vectors weighted Hamming distance is greater than the half of maximum weighted Hamming distance, take the current ordered i vector as the first test vector, and then re-start sorting. The Weighted Hamming distance of test set is smaller than which in The original

stochastic ranking test set after sorting, reducing the status change of circuit in test procedure, thereby reducing the test power[6] [7].

The circuit in Figure 4 is S1488 and the internal weighted jumping variables are the flowing:

$$P_0 = \sum_{i=1}^{N} \{[f_i(V_1) \oplus f_i(V_2)] \times fanout(i)\} \quad (4)$$

We can see from the first chapter that the smaller the P_0 , the smaller the power consumption in test procedure; the figure shows that the smaller the weighted Hamming distance ,the smaller the weighted hop variable in measured circuit internal, so the power consumption is smaller. So that we can use the Hamming distance optimizing test set to reduce the test power consumption.

5. Experimental Results

This method is applied to part of the ISCAS85and ISCAS89 circuit[8], uses the full-scan test design and MINTEST test set[9] whose optimization procedure uses MATLAB software[10], optimized with the greedy algorithm. Each circuit activity evaluation standard uses the measured circuit internal weighted transitions.

Table 1 is the comparison of circuit activity of the original order of each circuit, this method and Hamming distance in the test procedure. The second column is the number of test vector in the MINTEST test set, the third column is the internal weighted jump variables in measured circuit when the original test set is tested, the followed two column is the comparison of this method and the Hamming distance method, optimized range is the result of original activity minus optimized activity which divided by original activity, it is shown that this method has an obvious advantage over the Hamming distance method on the optimization of activity. The average optimization of this method is 48.07% and maximum optimization is 69.22%, the average optimization of Hamming distance is 28.58%, on the other hand ,time spent in this method is similar with which spent in the Hamming distance method.

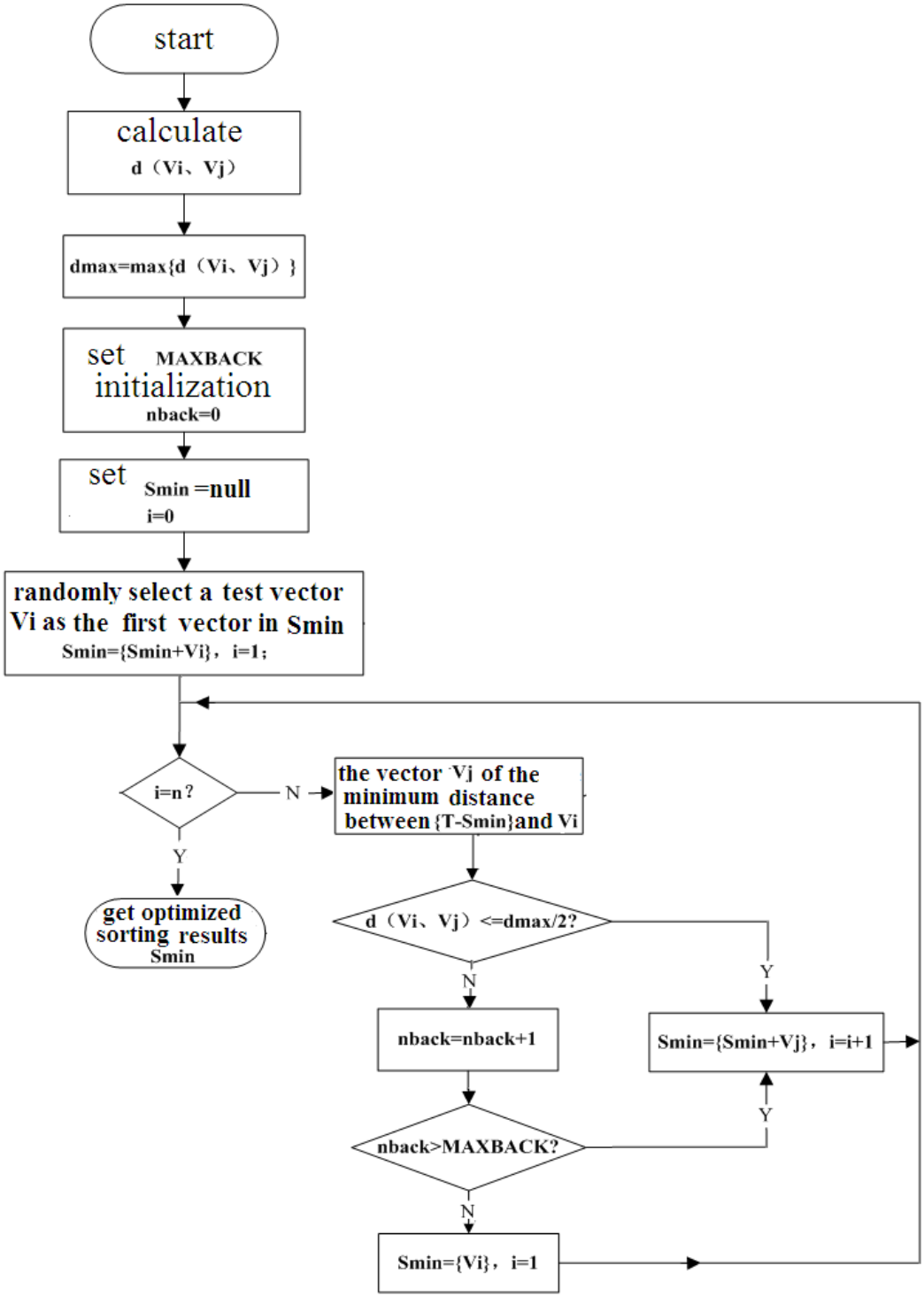

Figure 3. Process of Weighted Hamming Distance Algorithm

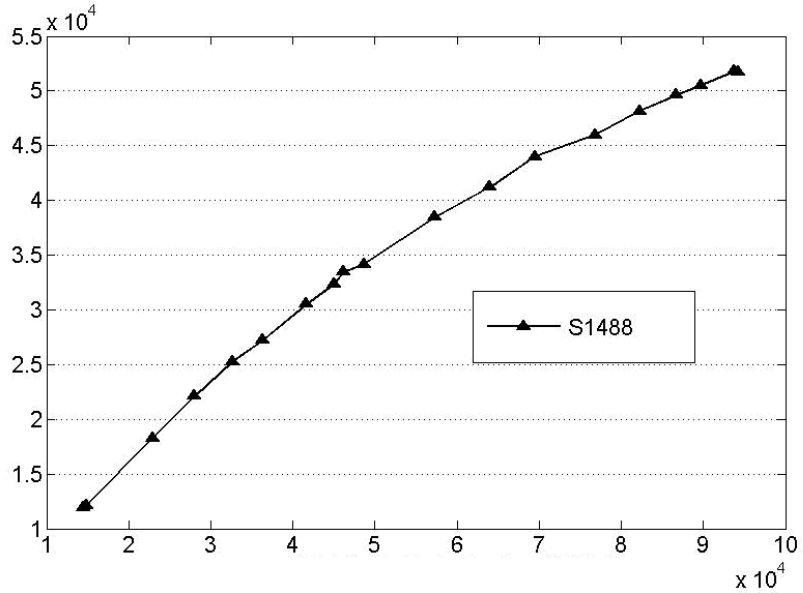

Figure 4. Relationship Between Weighted Hamming Distance and Weighted Transition of Circuit

6. Conclusion

This paper proposes a new ordering method of test vector after in-depth study of the power source of digital integrated circuit in testing process and original test of low power design. The method takes into consideration the internal structure of circuit and the information of test set, proposes the relationship between the changing of input and the changing of internal status of circuit, which is used to reordering the test set, then get the optimized test set. The ordered test set makes the state turnover number of circuit less during the test; reduce the power consumption of circuit efficiently. The method has not change the test set itself so it has no impact on the fault coverage.

Table 1. Experiment Result

circuit	Number of test vector	Weighted jump of random order	Hamming distance method.			method in the paper		
			Weighted jump	Optimization proportion	Time(s)	Weighted jump	Optimization proportion	Time(s)
c1908	106	50918	41581	18.34%	0.172	36586	28.15%	0.256
c7552	73	162620	146836	9.71%	0.872	134871	17.06%	1.21
s420	23	1622	1225	24.48%	0.0885	1066	34.28%	0.1723
s510	54	5953	4156	30.19%	0.1323	2333	60.81%	0.235
s820	93	14079	9010	36.00%	0.242	5258	62.65%	0.377
s832	94	14630	9608	34.33%	0.2124	5344	63.47%	0.358

s1238	121	29589	21042	28.89%	0.3111	15113	48.92%	0.465
s1488	101	39658	21125	46.73%	0.223	12207	69.22%	0.351

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