Design of Switching System Based on FC-AE-1553 Bus

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Abstract

As 1553B bus system is also widely used in modern avionics system, so in the new bus system development, not only the quality improvement on the performance is needed, but also should be required to be compatible with the original avionics equipment complying with 1553Bbus protocol, maximum reducing avionics system upgrade difficulty. Based on this consideration, the American National Standards Committee has developed the upper mapping of FC protocol—FC-AE-1553 agreement. FC-AE-155 agreement takes full advantages of the fibre channel and also gives full consideration to the requirement of being compatible with the original 1553B equipment, so the system upgrade can be easily realized. Conduct the fibre bus study based on FC-AE-1553, raise the hardware and software design methods and complete the control system demonstration verification based on fibre-optic bus. At the same time, conduct the bridging technology of FC-AE-1553 and MIL-STD-1553B, construct two types of demonstration verification system for bus bridging, breaking the hardware and software technology of FC-AE-1553 and MIL-STD-1553B bridging and establish the hybrid structure of the high and low speed bus, to meet the needs of the actual model, which plays a very important significance for the further development of China's aerospace business.

Keywords: Bus; Fibre; FC-AE-1553; Control system

1. Introduction

MIL-STD-1553 is the military data bus standard developed by the US Department of Defense, which is characterized by the linear network structure, redundancy, high electrical safety, good environmental adaptability and guaranteed rea-time performance, and has been applied in various aspects such as plane, vessels and vehicles, etc. Foreign use of 1553B bus has nearly two decades of history, in domestic, the application of 1553B bus has also been developed to study and imitation from being fully imported, and it has been successfully applied to the aircraft such as "J-8".

But with the appearance of the more and more highly integrated digital avionics system, the new avionics equipment are constantly applied to the modern aircraft, and the constraints of the data transfer rate to the avionics system becomes increasingly evident. Therefore the current avionics bus systems need great improvement in transmission speed. The fixed transmission speed 1Mb/s of 1553B bus has severely restricted the high-speed transmission of the data. Furthermore, the overall quality, network performance and anti-interference ability of 1553B bus system cannot meet the upgrade requires of modern avionics systems.

In order to meet the various needs of the development of modern avionics system developing a higher-performance bus system is an urgent task. The gradual rise of fibre channel technology just meets the various needs of the new bus system. Fibre channel (abbreviated as FC) is a computer communication protocol designed to adapt to the requirements of high-performance data transmission, with the advantages of high bandwidth, low latency, distance insensitiveness, flexible topology and supporting various upper-layer protocols. Fibre channel technology has been used in avionics system, and has become the preferred solution for the system interconnection of the next generation of aviation electronics system.

2. Study of Bus Architecture Based on FC-AE-1553

Construct the bus architecture base on FC-AE-1553, establish bus redundancy and switching mechanism, develop the reliable communication mode between devices and complete the following items:

2.1. FC-AE-1553 Communication Protocol Research

Determine the FC-AE-1553 network architecture suitable to the control system through the research on FC-AE-1553 communication protocol and control network form , to adapt to the use demand of the new research models,

2.2. FC-AE-1553 Communication Rahway Research

It is not necessary for RDMA to enable the sub-address lookup for the realization of quick move of the large blocks of data. The large image transmission and alignment problems in terminal guidance can be effective solved through the study of FC-AE-1553 RDMA. Bridge with 1553B and other mature buses to achieve a smooth transition of the models from low speed bus to high speed bus. When the system still has MIL-STD-1553B bus and MIL-STD-1553Bdevices, the original devices can be connected to FC network though the bridges from MIL-STD-1553B to FC-AE-1553, not only retaining the original hardware and software, but also achieving a moth upgrade f the system.

3. Analysis if Fibre Channel Protocol

3.1. Fibre Channel Protocol Overview

The T11 working group of the American International Committee for Information Technology Standards (INCITC) developed a high-speed serial communication protocol in 1998: fibre channel protocol, which combines the fast and reliable channel technology with the flexible and scalable network technology. FC protocol uses the channel technology to control signal transmission and uses control strategy based on channel shared conflict resolution mechanisms on the arbitration or exchange and the flow rate control strategy based on credit. FC transfer rate in commercial areas has gradually improved to 8Gbit/s from the initial 1Gbit/s, and it towards to 16Gbit/s. So far, the FC protocol has been able to support many upper-layer protocols and instruction set, such as IP, ATM and MIL-STD-1553 and HIPPI, IPL, SCSI and other instruction set. It can support various physical media, such as fibre optic and copper. FC can achieve the communication mode of full-duplex, half-duplex and simplex. The basic features of the FC protocol are: high bandwidth, high reliability, low delay, flexible topology and openness.

3.2. Fibre Channel Data Unit

Fibre channel frames and signaling protocol define 3 kinds of protocol data unit frame, sequence and exchange and the hierarchical relationship between them is shown in Figure 1.

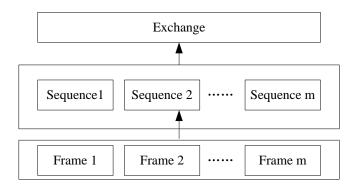


Figure 1. Hierarchical Relationship of the Protocol Data Unit

The frames follow a common frame format and FC frame format is shown in Figure2.

4bytes frame start	24bytes frame header	2112bytes Data area		4bytes CRC	4bytes End of
		64bytes Optical title	2048bytes Purely gruous	CRCtest	frame

Figure 2. FC Frame Format

Every frame includes the start delimiter, the fixed header with the size of 24bytes, various operational service head, and the flexible-length effective load from 0 to 2112 bytes, a frame standard cyclic redundancy check and a closing delimiter. The sequence is one or more relative frames transmitted from one N port to another N port. The sequence is a one-way transmission. Exchange consists of one ore more non-concurrent sequences. Exchange can be unidirectional or bidirectional.

3.3. Fibre Channel Service Type

Fibre channel defines 6 types of services. The use type is largely dependent on the category of the transmitted data. The main difference between the serve categories is to use the different types of flow control. If the communication is between two N-Port or one N-Port needs to be registered to the switched network, then the type 1 public service support. In the process of switched network registration and N-Port registration, the information is exchanged. The specific contents of the 6 types of services are as follows:

3.3.1. Service of Type 1: dedicated connection. The dedicated connection established by the service of type 1 needs to be maintained and ensured with the switches. The frame is transmitted to the destination N port in the same order with the sending order of source N port by the switch.

3.3.2. Service of Type 2: reuse connection. The service of type 2 is the non-connection service. after receiving data frame; the link control frame needs to be sent for confirmation. In a given sequence, the transmitter will continuously transmit the data frame of the type 2, but the switch cannot ensure to transmitted in order.

3.3.3. Service of Type 3: datagram. The service of type 3 is the non-connection service; just supporting the unimpeded transfer and it will not send any link control

frame for confirmation after receiving the valid data frame. In a given sequence, the transmitter will continuously transmit the data frame of the type 3, but the switch cannot ensure to transmitted in order.

3.3.4. Service of Type 4: part bandwidth. Use switch manage part bandwidth allocation protocol. The use of the service of type 4 inside the switch, sending frame with the two virtual circuit transmissions between the N ports with communication. In a given sequence, the transmitter will continuously transmit the data frame of the type 4, and the frame is transmitted to the destination N port in the same order with the sending order of source N port by the switch.

3.3.5. Service of Type 5: the service of type 5 is used for synchronization and instant service, but so far, it has not been fully defined and may be discarded.

3.3.6. Service of Type 6: multicast connection. The service of type 6 allows the establishment of the dedicated connection of one and more N port. Once the dedicated connections are established, they must be maintained and guaranteed by the switch. The data flow of type 6 can only be from source N port to destination N port. All of the destination N port will send the appropriate link response frame to the multicast server, which will collect there link response frame and return to a separate link to the source N port, and the frame is transmitted to the destination N port in the same order with the the sending order of source N port by the switch.

3.4. Fibre Channeled Protocol Hierarchical Structure

Similar to the OSI seven-layer model structure and TCP/IP four-layer model structure, FC protocol has five-layer model structure. FC-0 interface and media layer is used to define the characteristics of physical link: FC-1transmission protocol layer, defining the coding/decoding scheme, the byte synchronization and ordered set; FC-2link control layer, defining rules and mechanisms of block data transmission; FC-3 common service layer; FC-4 protocol mapping layer, defining the method of mapping the upper layer protocol to the lower layer protocol. Figure 3 shows a more intuitive structure of FC.

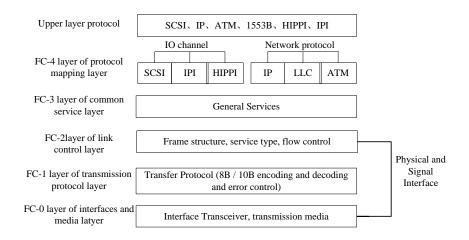


Figure 3. FC Hierarchical Structure

4. High and Low Speed Hybrid Bus Architecture Base on FC-AE-1553

In the design of the high and low sped hybrid bus architecture base on FC-AE-1553, according to the function, features data transmission of the various parts of the avionics system, the hybrid point-to-point topology of switching network should be used.

Due to the current FC-AE basically application in the aviation field, with relatively sound theory and practice, the avionics system bus architecture based on FC-AE-1553 is established taking the avionics system of the current aircraft as the model. As the core of the avionics system, the integrated core processor interior models complete the data and signal processing of many sensors, producing a variety of command and task data and realizing the release of the video and image signals. There are a lot of read-time and key data exchanges between the models, with high requirements for the reliability and timeliness. In the JAST plan, the photoelectric sensor and signal processing module has the highest requirements for processing capability, respectively reaching 400MIPS and 8000Mops, to support which, the topology structure inside the integrate core processor is required to provide higher bandwidth. Considering the three topology structures of FC, the switching network is most suitable, not only with reliability and timeliness, but also able to provide the communication of multiple highest bandwidth 4.268Gbps.

In F-35avionics system, ICP internal modules interconnects to each other through switch module. Based on the reference of the existing literature and design, the interconnection of the integrated core processing internal modules of the avionics system uses FC switching network, as shown in Figure 4.

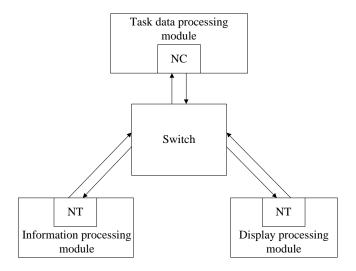


Figure 4. Integrated Core Processor Internal Topology Structure

There are a lot of real-time data transmissions between sensors and signal processing module, as well as monitor and display processing module, with relatively fixed transmission path. They have high requirement for the bandwidth. In the JAST plan, the radar input and output bandwidth is up to 1000Mbps and photoelectric sensor reaches 2000Mbps and electronic warfare sensor, 500Mbps, so the dedicated connection should be established with the bandwidth exclusive point-to-point structure, providing the highest 4.268Gbpsband width for completing the data transfer tasks.

In the F-22 avionics system, the connection between he sensor and CIP uses 400Mbit/s point-to-point fibre optic link. By the literature reference, the point-to-point structure can be used the dedicated connection established between the sensor and signal processor or the connection established between the monitor processor and the cockpit monitor. Through and above analysis and reference to the existing design, in the

design of the avionics system, the interconnection between the sensor and the signal processing module and the monitor and the monitor processing module uses the point-to-point configuration, as shown in Figure 5.

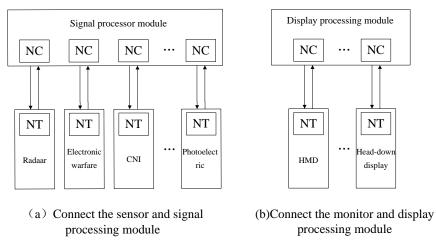


Figure 5. Point-to-Point Topology Structure in Avionics System

The entire avionics system uses point-to[-point and switching network hybrid topology structure, as shown in Figure 6. depending on the difference between the equipment and modules functions in the system, the defines of equipment and module interface functions are conducted. In the integrated core processing internal switch ing network structure, task data processing module, as the core management module, is the initiator and scheduler of the data transfer, with NC interface and other modules have NT interface. In the point-to-point structure, signal processing module and display processing module as the initiator and scheduler of the data transfer has NC interface. And the sensor and monitor passively send or receive data, with NT interface. So in the whole, the signal processing module and display processing module have multi-NC and single NT interfaces, completing their functions respectively in the different network topologies. Protocol bridge, as NT access switching network, sends control and task information to 1553B bus under the management of task data processing module. There may be many protocol bridge, with each bridge corresponding to a 1553B bus.

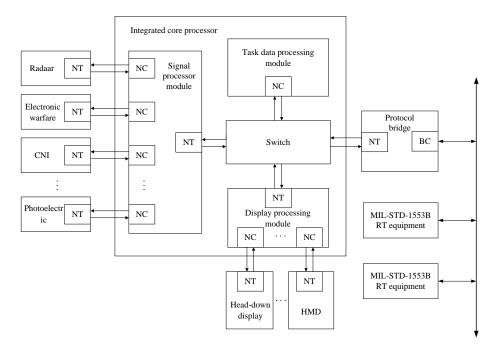
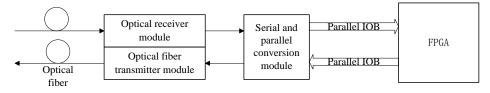


Figure 6. Avionics System Bus Architecture Based on FC-AE-1553

5. Protocol Bridge Interface Circuit Design

5.1. FC-AE-1553 Interface Circuit Design

According to the design requirements and NC/NT module compatibles, the protocol modules also use 1.0625G/band rate fibre. In order to make FPGA identify data signals, the1.0625G/serial data need to be converted to 106.25M/s parallel data. Figure 7 shows a detailed presentation of the design scheme of FC-AE-1553 interface circuit.





This design also uses the multimode optical fibre with the core diameter of 50um, out packaging diameter of 125um, taking the short wave with 850nm wavelength as the optical signal carrier. Optical fibre receiving module also uses FTLF8524P2 of Finisar Company the same with NC/NT modules. The signal after photoelectric conversion is 1.0625G/s serial data and the optical fibre communication uses 8b/10b coding mode, so it is necessary to convert the serial data to 10B parallel data. Because the FPGA used does not contain high-speed transceiver, the serial and parallel conversion chip needs to be added, which should be from Agilent Company (HDMP-1636A).

Serial and parallel conversion chip HDMP-1636A mainly contains TX0~TX9, REFCLK, RX0~RX9, RBC0, RBC1, BYTSYNC, ENBYTSYNC, RX+(-) and TX+(-) of signals, among which, RX+, RX- and TX+, TX- differential signals are the serial signal connected with the photoelectric conversion chip. TX0~TX9 is the 10B parallel data transmitted by FPGA, companied with the associated clock REFCLK, 180 degrees

difference with the data, and the serial and parallel conversion chip will store the data at the rising edge of the associated clock and convert the associated clock multiplier 10 times parallel data into 1.0625G/s serial data. RX0~RX9 is the serial data received by the photoelectric receiver and will be converted to 10B parallel data, which is the data receiving termination. RBC0 and RBC1 obtain two 53.125M clocks with the difference of 180 degrees using REFCLK by the serial and parallel conversion chip PLL binary frequency. RX0~RX9 is valid on the rising edge of RBC0 and RBC1. RBC0 and RBC1c convert 106.25M/s data frequency to 53.125M/s, making the data processing requirements to the hardware performance reduced. Figure 8 shows the data transmission and reception mode of the serial and parallel conversion chip.

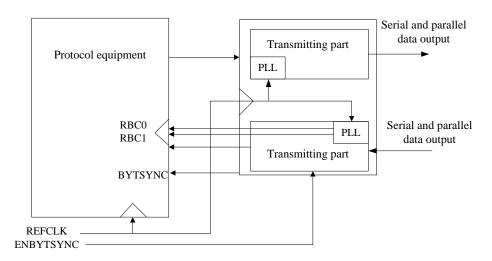


Figure 8. HDMP-1636A Application Diagram

Serial and parallel conversion chip also supports special characters 101111100(K28.5 RD-coding) detecting synchronization function. When the ENBYTSYNC is enabled, whenever detecting 101111100, the middle of RX0~RX9 will be strictly aligned with the rising edge of RBC0/RBC1 and the synchronization enabling BYTSYNC give the high level. The links always have K28.5 RD- coding in the normal communication, ensuring the strict alignment between the data valid points and the associated clock to prevent the appearance of error codes.

6. Conclusion

Construct the bus architecture base on FC-AE-1553, establish bus redundancy and switching mechanism, develop the reliable communication mode between devices and complete the following items:

6.1. FC-AE-1553 Communication Protocol Reach

Determine the FC-AE-1553 network architectrure suitable to the control system through the research on FC-AE-1553 communication protocol and control network form ,to adapt to the use demand of the new research models,

6.2. FC-AE-1553 Communication Rahway Research

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