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Design Goal Based Implementation of Energy Efficient Greek Unicode Reader for Natural Language Processing

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Abstract

Unicode font is used in coding system that assign a unique code to every symbol of scripts irrespective of their platform, and language. The Greek Unicoder receives 16-bit hexadecimal code of alphabet. The device has been designed to convert Greek language into different languages that our people could understand. This Unicode reader code has been implemented on 28nm FPGA platform called Kintex-7 FPGA. In this paper we are using frequency scaling technique and Design goal. In this paper power analysis is our main concern and we have studied about the power analysis at different frequencies keeping the temperature constant at 25 degree Celsius and maintaining the constant air flow.

Keywords: *Design Goal, Greek, Unicode Reader, FPGA, Energy Efficient*

1. Introduction

Greek is an independent branch of the Indo-European family of languages [1]. Unicode assign a code to every character irrespective of their platform, program and language [4]. Research gap was identified and going to fill with design of energy efficient hardware in text analysis [2]. A lot of research has been done in the field of Unicode readers and many researches have presented their work and are still working for better results. Design of Punjabi Unicoder for Gurmukhi scripts on Virtex-6 FPGA had been discussed [3]. Comparison between the two languages that is Arabic and Punjabi has been done [6]. Paper discusses additions to Arabic Script for the representation of Punjabi language [6]. Other researchers have designed Bengali Unicode reader [5], Gurmukhi OCR [7] and Gurmukhi Words Recognition system [8] and Devnagari Unicoder [9] too. In this research work, we have designed a Greek Unicode Reader that will translate Greek Language into other languages and will tell us about the Additional letters, Archaic letters, Coptic letters, Editorial symbols, Letters, subscript, Lowercase, Numeral signs, Punctuation, Spacing accent, Symbol, Variant letters form.

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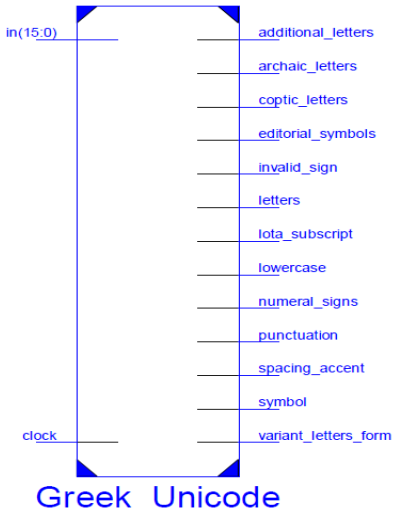

Figure 1. Symbol of Greek Unicode Reader

Unicoder receives16-bit hexadecimal code for symbol in scripts is visible in Figure 1. The output of reader can be one of 13 outputs. Depending on Greek input, output at output port will visible. Greek Unicode takes input as an alphabet and gives corresponding output like Additional_letters, Archaic_letters, Coptic_letters, Editorial_symbols, Letters, Lota_subscript, Lowercase, Numeral_signs, Punctuation, Spacing_accent, Symbol, Variant_letters_form. Ranges of outputs are shown in Table 1.

Table 1. Hexadecimal Range of Greek Unicode

Character Type	Unicode Range
Additional_letters	037F, 03F3
Archaic_letters	0370-0373, 0376-0377, 03D8-03E1, 03FA, 03FB, 03F7, 03F8
Coptic_letters	03E2-03EF
Editorial_symbols	03FD-03FF
Letters	0386, 0388-03CE
Lota_subscript	037A
Lowercase	037B-037D
Numeral_signs	0374-0375
Punctuation	037E,0387
Spacing_accent	0384-0385
Symbol	03FC
Variant_letters_form	03CF-03D7,03F9,03F4-03F6,03F0-03F2

We have taken different set of frequencies mentioned and have done power analysis by varying its design goal. In this paper, we are using frequency scaling technique as energy efficient design. Others techniques are capacitance scaling technique [10], thermal scaling [12], and scalable implementation [11]. In Xilinx software, we have five design goals and they are Area Reduction, Balanced, Minimum Runtime, Power Optimization, and Timing Performance shown in Figure 2. These design goals plays a vital role when we analyses power in our circuit or design [13-19]. In this paper power analysis is our main concern and we have studied about the power analysis in this paper at different frequencies keeping the temperature constant at 25 degree Celsius and maintaining the constant air flow.

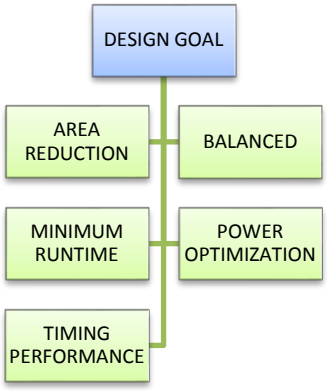

Figure 2. Types of Design Goal

Power is also of two types (i) Static (ii) Dynamic. In this research work we have focus on the dynamic power and it includes Clock Power (CPower), Logic Power (LoPower), Signal Power (SPower), IO Power (IOPower), and Leakage Power (LePower). The sum of all these give us the TPower involved in the designed. Figure 3 shows the components of power. Our main aim is to make it energy efficient that's why the testing has been done at different frequencies and different design goal.

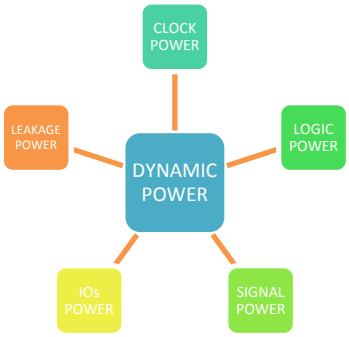

Figure 3. Components of Dynamic Power

2. Power Analysis

A. Power Analysis at 1400 Million Hertz

Table 2. Power Analysis at 1400 Million Hertz

Design goal	CPower	LoPower	SPower	IOPower	LePower	TPower
Area reduction	0.008	0.001	0.002	0.006	0.045	0.062
Balanced	0.008	0.001	0.002	0.061	0.045	0.118
Minimum runtime	0.013	0.001	0.002	0.004	0.045	0.066
Power optimization	0.013	0.001	0.002	0.004	0.045	0.066
Timing performance	0.008	0.001	0.002	0.061	0.045	0.118

There is 38.46% saving in C Power dissipation with area reduction, Balanced and Timing Performance design goal, when compare to power dissipation with minimum run time and Power Optimization design goal. There is 90.16% reduction in IO power dissipation with area reduction design and 93.44% reduction in IO power dissipation with Minimum runtime and Power Optimization goal when compared with Balanced and Timing performance design goal. There is no change in LoPower, SPower and LePower. There is 44.06% saving in TPower dissipation with minimum runtime and power

optimization when compared with balanced and timing performance design goal's power dissipation as visible in Table 2 and Figure 4.

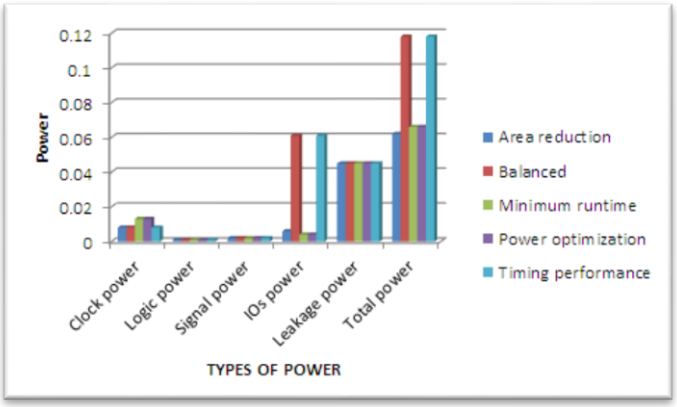

Figure 4. Power Dissipation at 1400 Million Hertz

B. Power Analysis at 1.2Giga Hertz

Table 3. Power Analysis at 1.2Giga Hertz

Design goal	CPower	LoPower	SPower	IOPower	LePower	TPower
Area reduction	0.007	0.001	0.002	0.005	0.045	0.059
Balanced	0.007	0.001	0.002	0.045	0.045	0.100
Minimum runtime	0.007	0.001	0.002	0.045	0.045	0.100
Power optimization	0.011	0.001	0.002	0.004	0.045	0.063
Timing performance	0.007	0.001	0.002	0.045	0.045	0.100

There is 36.36% saving in CPower dissipation with area reduction, balanced, minimum runtime, Timing performance design goal when compared with power dissipation of with balanced, minimum run time, and timing performance design goal. There is 41.50% reduction in IO power dissipation with power optimization design goal in compare to all other different design goal. There is no change in LoPower and LePower. There is 12.5% saving in SPower dissipation with area reduction, power optimization, timing performance and balanced when compared with power dissipation of minimum runtime. There is 20.83% saving in TPower dissipation with power optimization when compared with balanced, minimum runtime and timing performance design goal's power dissipation as visible in Table 3 and Figure 5.

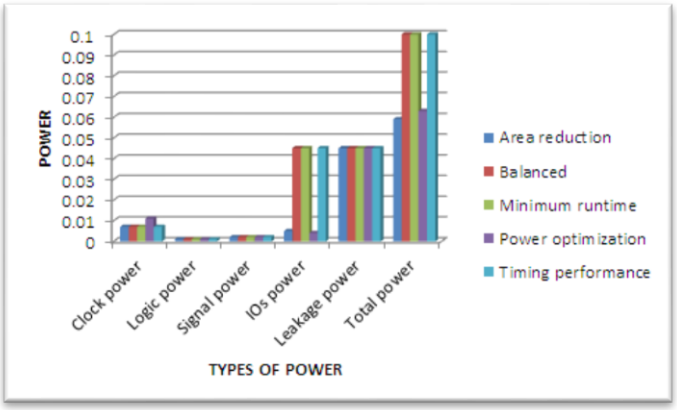

Figure 5. Power Dissipation at 1.2 Giga Hertz

C. Power Analysis at 2100 Million Hertz

Table 4. Power Analysis at 2100 Million Hertz

Design goal	CPower	LoPower	SPower	IOPower	LePower	TPower
Area reduction	0.012	0.001	0.003	0.010	0.045	0.072
Balanced	0.012	0.001	0.004	0.134	0.046	0.197
Minimum runtime	0.012	0.001	0.004	0.134	0.046	0.196
Power optimization	0.020	0.001	0.004	0.006	0.045	0.076
Timing performance	0.012	0.001	0.003	0.134	0.046	0.196

There is 35.29% saving in CPower dissipation with area reduction design goal , 23.52% saving in CPower dissipation with power optimization design goal in compare to power dissipation with balanced, minimum run time, and timing performance design goal. There is 64.74% reduction in IO power dissipation with power optimization design goal in compare to all other different design goal. There is no change in LoPower and LePower. There is 14.28% saving in SPower dissipation with area reduction, power optimization when compared with power dissipation of minimum runtime. There is 7.14% saving in SPower with balanced when compared with minimum runtime. There is 45% saving in TPower dissipation with power optimization when compared with minimum runtime design goal's power dissipation as visible in Table 4 and Figure 6.

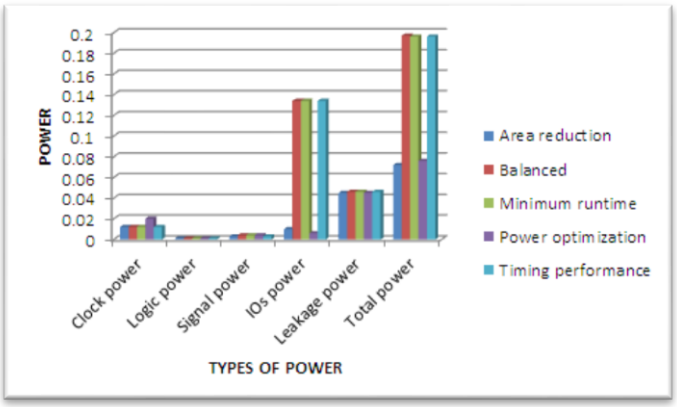

Figure 6. Power Dissipation at 2100 Million Hertz

D. Power Analysis at 1700Million Hertz

Table 5. Power Analysis at 1700Million Hertz

Design goal	CPower	LoPower	SPower	IOPower	LePower	TPower
Area reduction	0.010	0.001	0.003	0.007	0.045	0.066
Balanced	0.010	0.001	0.003	0.089	0.045	0.148
Minimum runtime	0.010	0.001	0.003	0.089	0.045	0.148
Power optimization	0.016	0.001	0.003	0.005	0.045	0.070
Timing performance	0.010	0.001	0.003	0.089	0.045	0.148

There is 50% saving in CPower dissipation with area reduction design goal, 28.57% saving in CPower dissipation with power optimization design goal in compare to power dissipation with balanced, minimum run time, and timing performance design goal. There

is 57.28% reduction in IO power dissipation with power optimization design goal in compare to all other different design goal. There is no change in LoPower and LePower. There is 9.09% saving in SPower dissipation with area reduction, power optimization and timing when compared with power dissipation of minimum runtime and balanced. There is 35.55% saving in TPower dissipation with power optimization when compared with balanced design goal's power dissipation as visible in Table 5 and Figure 7.

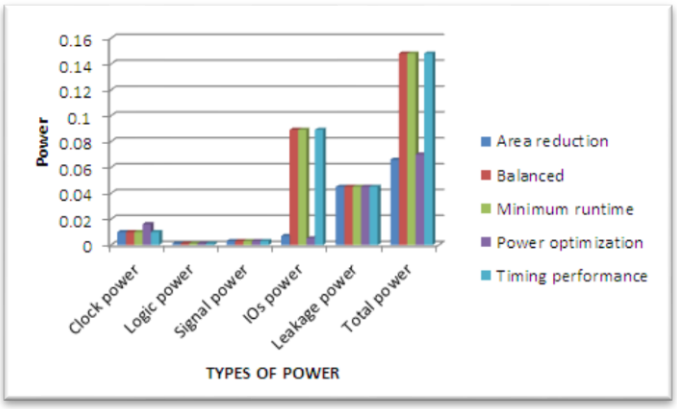

Figure 7. Power Dissipation at 1700 Million Hertz

E. Power Analysis at 1800Million Hertz

Table 6. Power Analysis at 1800 Million Hertz

Design goal	CPower	LoPower	SPower	IOPower	LePower	TPower
Area reduction	0.011	0.001	0.003	0.008	0.045	0.068
Balanced	0.011	0.001	0.003	0.099	0.045	0.159
Minimum runtime	0.011	0.001	0.003	0.099	0.045	0.159
Power optimization	0.017	0.001	0.003	0.005	0.045	0.072
Timing performance	0.011	0.001	0.003	0.099	0.045	0.159

There is 40% saving in CPower dissipation with area reduction design goal,26.66% saving in CPower dissipation with power optimization design goal in compare to power dissipation with balanced, minimum run time, and timing performance design goal. There is 0.8% saving in IO power dissipation with balanced, minimum runtime and timing performance and 59.48 % saving in IO power dissipation with power optimization design goal in compare with area reduction design goal. There is no change in LePower. There is 16.66% saving in SPower dissipation with area reduction, power optimization and 8.33% saving in SPower dissipation with balanced and timing performance when compared with power dissipation of minimum runtime. There is 38.14% saving in TPower dissipation with power optimization when compared with minimum runtime design goal's power dissipation as visible in Table 6 and Figure 8.

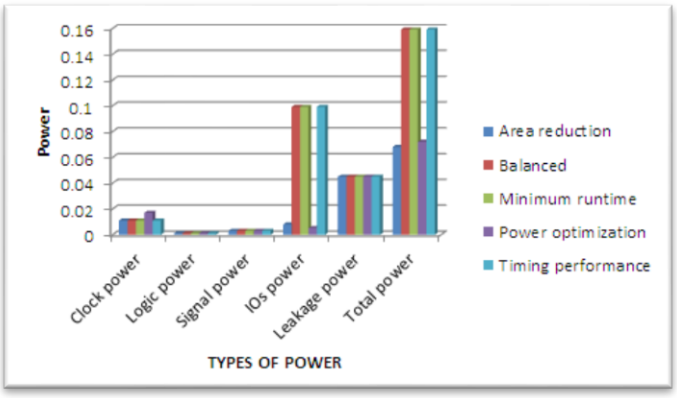

Figure 8. Power Dissipation at 1800 Million Hertz

F. Power Analysis at 2.2 Giga Hertz

Table 7. Power Analysis at 2.2 Giga Hertz

Design goal	CPower	LoPower	SPower	IOPower	LePower	TPower
Area reduction	0.013	0.001	0.004	0.010	0.045	0.073
Balanced	0.013	0.001	0.004	0.146	0.046	0.210
Minimum runtime	0.013	0.001	0.004	0.146	0.046	0.210
Power optimization	0.021	0.001	0.004	0.007	0.045	0.078
Timing performance	0.013	0.001	0.004	0.146	0.046	0.210

There is 38.88% saving in CPower dissipation with area reduction and power optimization design goal in compare to power dissipation with balanced, minimum run time, and timing performance design goal. There is 66.66% saving in IO power dissipation with power optimization and 0.58% saving in IO power dissipation with balanced, minimum runtime and timing performance design goal in compare to area reductiondesign goal. There is no change in LoPower and LePower. There is 20% saving in SPower dissipation with area reduction, power optimization, and 13.33% saving in SPower dissipation with balanced and timing performance when compared with power dissipation of minimum runtime. There is 53.30% saving in TPower dissipation with power optimization when compared with balanced, minimum runtime and timing performance design goal's power dissipation as visible in Table 7 and Figure 9.

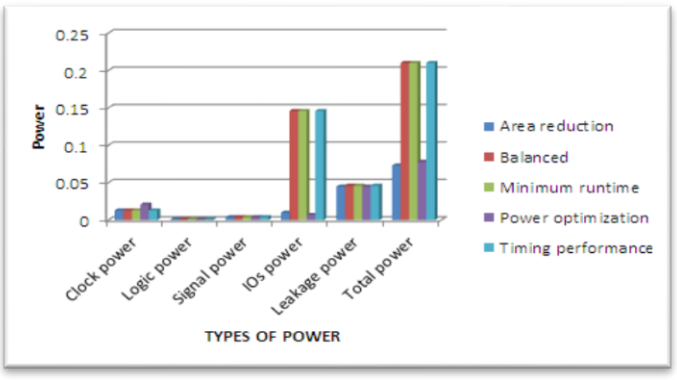

Figure 9. Power Dissipation at 2.2 Giga Hertz

3. Conclusion

There was research gap in natural language processing for energy efficient design. Here, by designing the energy efficient Greek Unicode Reader we have filled this research gap. This Unicode reader code has been implemented on Xilinx ISE Design Suite 14.2 and results were tested on 28nm FPGA platform using Kintex-7 FPGA family. The device has been designed to convert Greek language into different languages that our people could understand. The schematic of Greek Unicode reader takes 16-bit hexadecimal code of alphabet and clock. The output that can be given by this reader can be one of 13 outputs. Our Unicode reader is operating at 25 degree Celsius. The design is based on different design goals like Area Reduction, Balanced, Minimum runtime, Power optimization, Timing performance and is tested at various operating frequencies such as 1400 Million Hertz, 1.2 Giga Hertz, 2100 Million Hertz, 1700 Million Hertz, 1800 Million Hertz, 2.2Giga Hertz.

4. Future Scope

"The best way to predict future is to create it" is a age old saying. Similarly, predicting future of our research is limited to what we can think that is possible in near future with current understanding of system and techniques. Our current knowledge is limited to 28nm FPGA, 1.2-2.2 billion Hertz range. In future, that can be extended beyond 28nm FPGA and 1.2-2.2 GHz frequency ranges. In this work we are limited to Greek Unicode, so we can go for Unicode reader design of the other languages used in this world like Hindi, Chinese, Italian, German, Mandarin and so on.

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