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FPGA Implementation of Image Acquisition for Quadruped Search Robot Monitor

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Abstract

The problem of image acquisition system for quadruped search robot is proposed based on FPGA. The quadruped search robot can be used in smart home monitor. In the design, FPGA ping-pong operation method is used. The OV9650 camera module, EP4CE15 main control chip module and auxiliary module (clock unit and PLL unit) are completed with module method. The software design of the system is completed, including the control module and image acquisition module. According to the problems of co-ordination mechanisms of image acquisition, image storage and image processing, the immunity algorithm is improved to achieve co-ordination mechanisms. The simulation results given by training time of co-ordination mechanisms indicate that the proposed image acquisition system of FPGA is effective.

Keywords: *image acquisition; FPGA design; robot monitor; co-ordination mechanisms*

1. Introduction

With the improvement of living standards, people put forward the higher request to the residential function and residential quality [1]. The connotation of residential quality transforms from the simple construction quality to the comprehensive function quality [2]. So, smart home becomes the development direction of the modern house. Intelligent home is liked with safe, comfortable, flow of information and perfect service by people. Therefore, the research and development of smart home have a very important significance to meet with requirements of the people.

The development of real smart home is intelligent control system solutions for a complete set of intelligent home [3]. It includes state detection, parameter record, state identification and automatic control to the various functional units of the modern family. These processes will be concentrated together [4-6]. It is local control or remote control to achieved the needs of the people.

Significant characteristics of the development of smart home is the gradual integration of automatic control technology and robot technology in recent years [7-9]. Today, for example, automatic cleaning robots is a very good application for smart home. So, there may be the below picture for smart home in the future. The owner left the house to go to the office and want to keep monitoring to every corner of home. There is need to monitor every indoor corner with a mobile robot [10]. This not only prevents outside intrusion and timely alarm, but also avoids the information omission of home water leakage.

Nowadays, the quadruped walking robots has been making great progress. The monitor system of quadruped search robot not only has good image acquisition ability, but also

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has enough acquisition efficiency. Image acquisition method is commonly used by the acquisition card. But this design is not suitable for embedded real-time control system of quadruped search robot. At present, the most outstanding embedded soft-core is in the FPGA (Field-Programmable Gate Array) [11].

Designers and engineers of smart home are usually more interested in the behavior of smart home control system than control complexity. This paper attempts to integrating embedded technology and robot technology into smart home. FPGA acquisition system of the quadruped mobile robot is designed, which is beneficial to the control of various functions unit of smart home.

2. FPGA Image Acquisition System

For the monitor system of robot, the main consideration is the problem of the system operation speed and power consumption. The biggest advantage and characteristic of Nios II is the modular hardware structure, and it has good ability to modify and extend. This system uses Quartus II as the hardware development platform, and uses FPGA chip as the controller, the image sensor, memory, video converter, TFT display interface as FPGA peripherals. It is shown in Figure 1. The programming and control of the FPGA and peripherals is with SOPC technology, and it eventually realize the image real time collection.

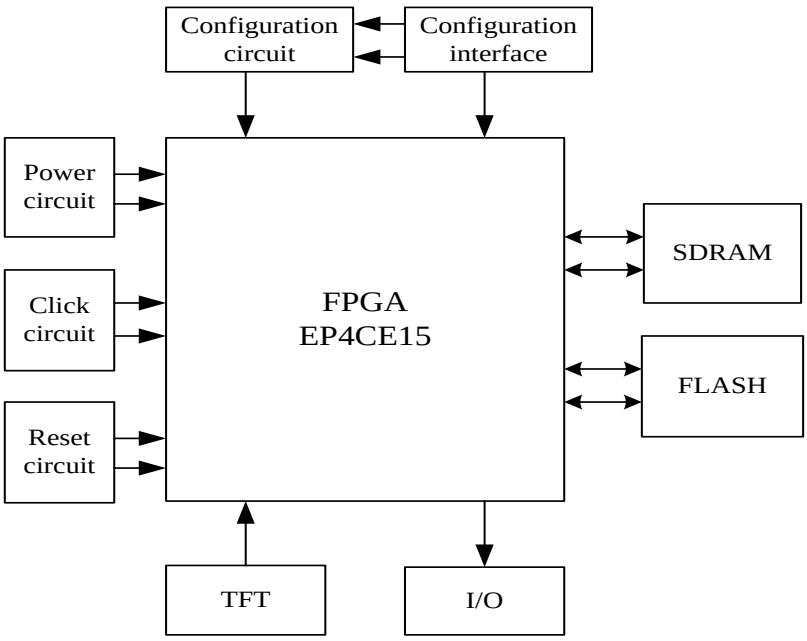


Figure 1. Image Acquisition System Framework

2.1. Ping-pong Operation Design Method Based on FPGA

Serial design method only needs a set of registers and memory in performing arithmetic task and save the hardware resources, but its computation speed is slow compared to the parallel design method. Although the parallel design method occupies hardware resources more than serial design method, but it is suit for this research, which focuses on processing speed. Therefore, parallel design method with ping-pong operation is designed for digital system based on FPGA. The illustration of ping-pong operation is shown in Figure 2.

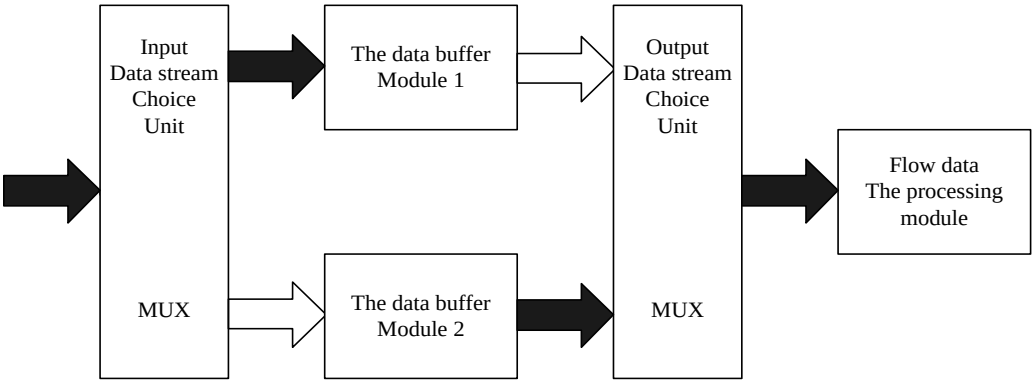


Figure 2. Illustration of Ping-pong Operation

Process: System selects the ping-pong operation unit and lets input data distribution into such two parts separately in the buffer module, and then system performs the buffer module. Input data part of the selection unit 1 is output. At the same time, the data input selection unit puts isochronous data into the buffer module 1. When part output of the data 1 is end, the output module 2 part data of selection single element output through the output unit. At the same time, output module 2 is the data buffer module. According to the process of continuous output, it completes the ping-pong operation.

2.2. The Main Module Design of OV9650

OV9650 is COMS camera with 1300000 pixels of OmniVision Company, and it can clearly to capture image information. The data interface of OV9650 is called SCCB (serial camera control bus), which is consists of two data lines: SIO_C is used for the transmission of the clock signals; SIO_D is used for the transmission of data signals. A secondary transmission of SCCB has 9 bits of data. The top 8 bits of data is useful data. The ninth bit data is not care bits during a write cycle and it is NA bit in a read cycle. The basic unit of data transmission is the SCCB phase, which is a transmission of a data byte. SCCB transmission cycle is shown in Figure 3.

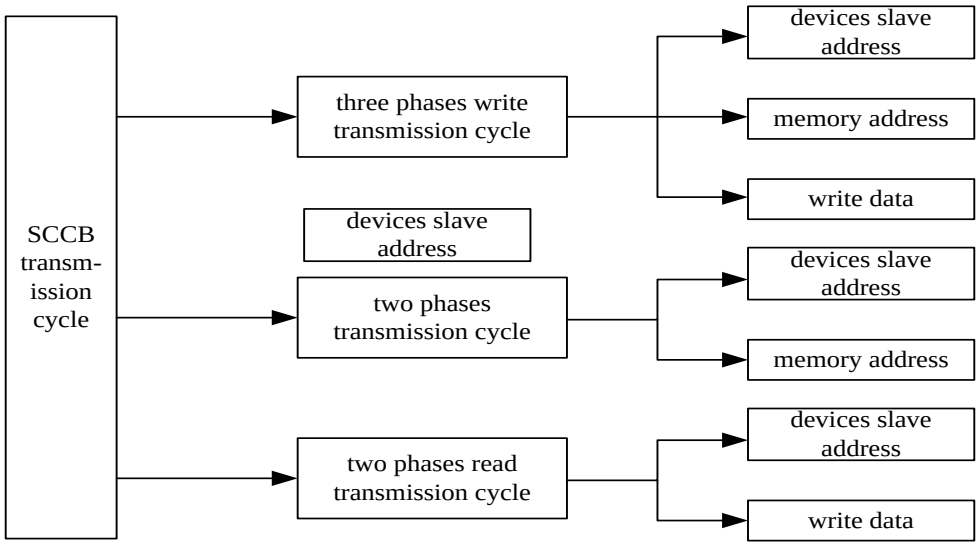


Figure 3. SCCB Transmission Cycle

When data is need to write, three phases write transmission cycle is used. When data is need to read, two phases transmission cycle and two phases read transmission cycle are

orderly used. So SCCB can only read or write a byte. OV9650 has high pixels, and the transmission mode of SCCB is similar with IIC transmission, the application of IIC transmission is instead of its original SCCB transmission. The transmission process is simplified to hardware implementation.

2.3. The Main Control Chip Module

The FPGA main chip is mainly different in logic unit (LE) of several numbers, memory capacity, general PLL number and I/O port number. This study focuses on the memory capacity, logical unit number. Altera's EP4CE15 chip has a number of storage capacity and logical unit larger. The connection of EP4CE15 is shown in Figure 4.

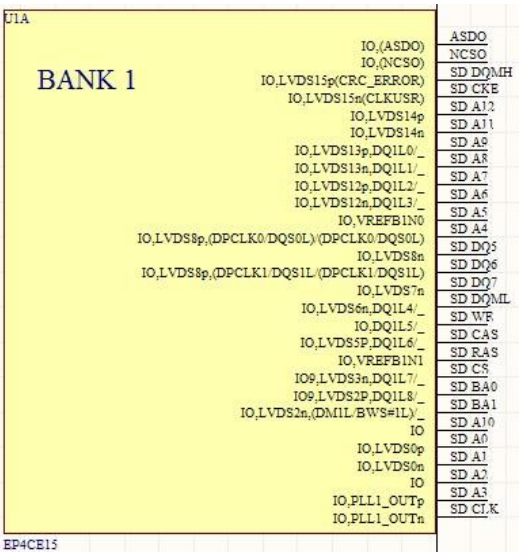


Figure 4. EP4CE15 External Wiring

2.4. FPGA Crystal Oscillator Circuit Design

In the FPGA clock circuit design, clock skew is one of the most serious problems. Clock skew is called time difference that different elements detect the effective clock jump within the system. Method that reduces clock skew is through the PLL module and FPGA proper clock buffer within the frequency division and the frequency multiplier of the input clock. FPGA crystal oscillator circuit and PLL circuit are shown in Figure 5 and Figure 6.

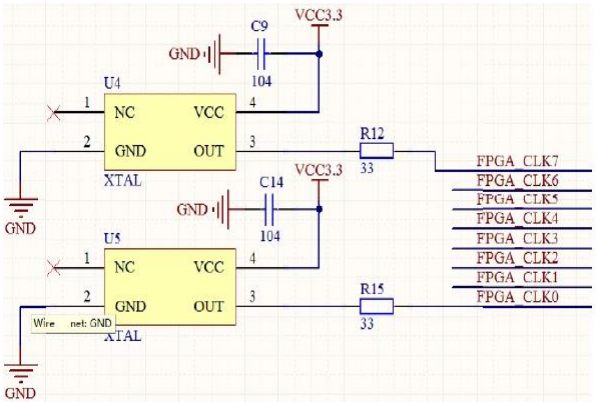


Figure 5. FPGA Crystal Oscillator Circuit

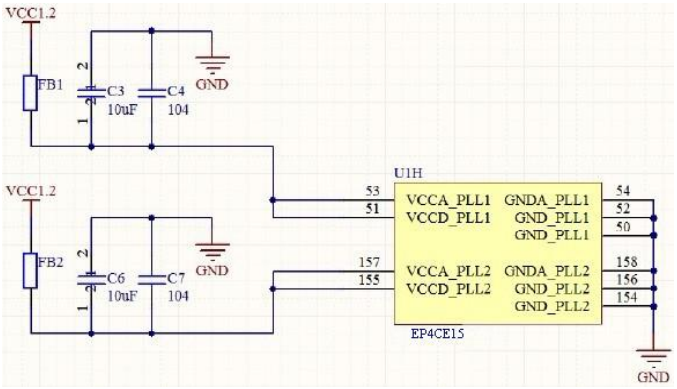
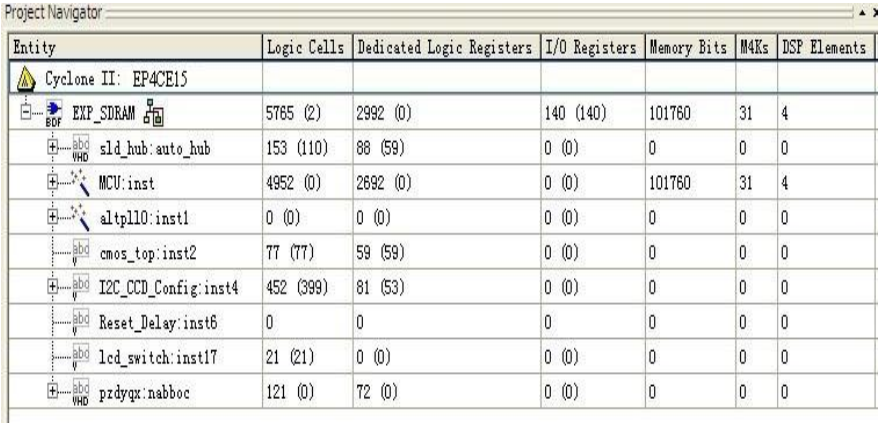


Figure 6. PLL Circuit of FPGA

2.5. Image Acquisition Design

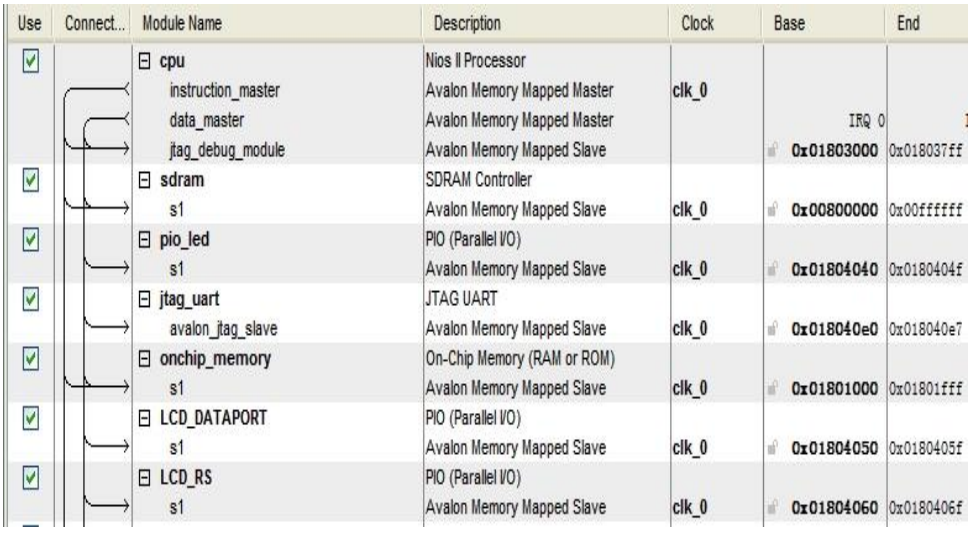
Establishment of Nios II Engineering is shown in Figure 7. The appropriate control core and peripheral circuit are selected, and FPGA pin is bound. The configuration information of engineering II Quartsu is completed, and it generates BDF files. Nios II system configuration is shown in Figure 8.



Project Navigator

Entity	Logic Cells	Dedicated Logic Registers	I/O Registers	Memory Bits	M4Ks	DSP Elements
Cyclone II: EP4CE15						
EXP_SDRAM	5765 (2)	2992 (0)	140 (140)	101760	31	4
sld_hub:auto_hub	153 (110)	88 (59)	0 (0)	0	0	0
MCU:inst	4952 (0)	2692 (0)	0 (0)	101760	31	4
altpll0:inst1	0 (0)	0 (0)	0 (0)	0	0	0
cmos_top:inst2	77 (77)	59 (59)	0 (0)	0	0	0
I2C_CCD_Config:inst4	452 (399)	81 (53)	0 (0)	0	0	0
Reset_Delay:inst6	0	0	0	0	0	0
lcd_switch:inst17	21 (21)	0 (0)	0 (0)	0	0	0
pzdyqx:nabboc	121 (0)	72 (0)	0 (0)	0	0	0

Figure 7. Quartus II Image Acquisition Project Navigator



Use	Connect...	Module Name	Description	Clock	Base	End
☑		cpu	Nios II Processor			
		instruction_master	Avalon Memory Mapped Master	clk_0		
		data_master	Avalon Memory Mapped Master		IRQ 0	
		jtag_debug_module	Avalon Memory Mapped Slave		0x01803000	0x018037ff
☑		sdram	SDRAM Controller			
		s1	Avalon Memory Mapped Slave	clk_0	0x00800000	0x00ffffff
☑		pio_led	PIO (Parallel I/O)			
		s1	Avalon Memory Mapped Slave	clk_0	0x01804040	0x0180404f
☑		jtag_uart	JTAG UART			
		avalon_jtag_slave	Avalon Memory Mapped Slave	clk_0	0x018040e0	0x018040e7
☑		onchip_memory	On-Chip Memory (RAM or ROM)			
		s1	Avalon Memory Mapped Slave	clk_0	0x01801000	0x01801fff
☑		LCD_DATAPORT	PIO (Parallel I/O)			
		s1	Avalon Memory Mapped Slave	clk_0	0x01804050	0x0180405f
☑		LCD_RS	PIO (Parallel I/O)			
		s1	Avalon Memory Mapped Slave	clk_0	0x01804060	0x0180406f

Figure 8. Nios II System Configuration

2.5.1. I2C Image Sensor Configuration Module

Read and write operations of the register is achieved through the I2C bus. The transmission of I2C bus timing is shown in Figure 9. This study uses the FPGA control as the acquisition module of the host machine, and the corresponding register is a slave object. The host machine configures the slave machine through I2C bus to achieve data transmission.

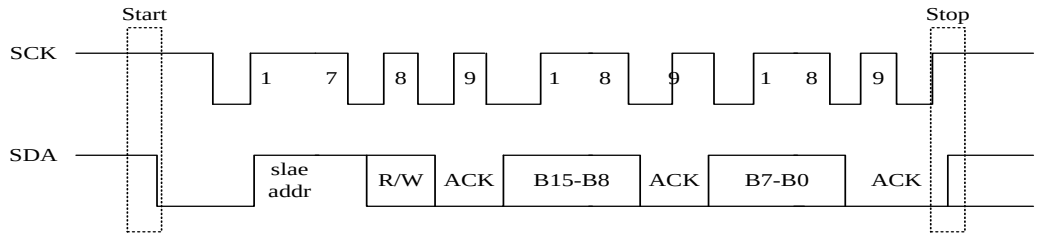


Figure 9. I2C Transfer Timing

Because SOPC Builder does not provide the I2C kernel, the host program is need to write and make the control chip I/O port communication function realization of I2C. The data transfer simulation waveform is shown in Figure 10.

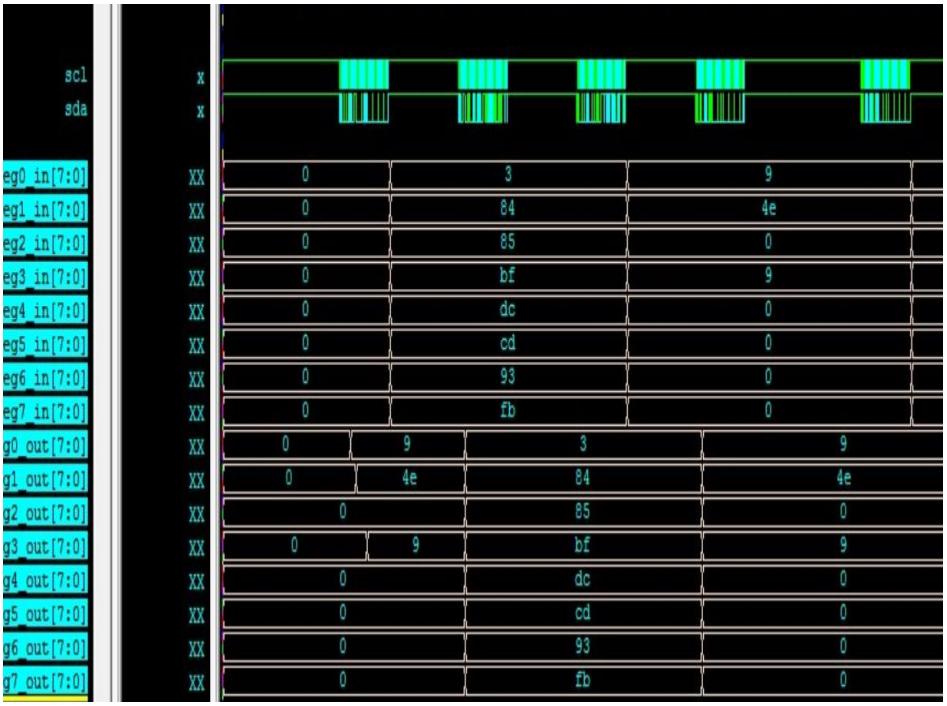


Figure 10. Simulation Waveform Data Transfer

2.5.2. I2C Image Information Extraction Module

FPGA provides the main work clock to register, and the assignment of VS, HREF and PCLE3 signals will register the data output to the main control chip. Acquisition process is determined by VS condition that is high or low for the trigger condition. When the VS signal is at high level, the system gives the address control to start the program. Judging from the high to low for HREF level, the system begins to collect image at the same time. WE signal is set to low level and the system begins to extract image information. When

PCLE signal is high, the new addresses are given and the system goes to extract image information.

3. Co-ordination Mechanisms of Image Acquisition, Image Storage and Image Processing

At the time of data collection, computer send commands to the FPGA module, A/D module began to work, flow of data is continuous. Because of the continuous storage, hard disk should be check by CRC. Once there is the error, a frame of data must be transmitted again. So, the storage structure has a large buffer device. Co-ordination mechanisms of image acquisition, image storage and image processing must be designed.

Immunity algorithm is same as other evolution algorithms, they are all the tactics of assembly searching. But the immunity algorithm has memory functions, there is more extensive application. It discerns the question at first, while estimates a group solution at first for the unknown question, and then it imitates the principle of immunity system for those estimated solutions, repeating the cloning course constantly. According to the fit or unfit of the estimated solutions, immunity algorithm takes it as judgment to upgrade and evolve the present estimated solutions until it solves optimally.

The basic immunity algorithm has the following shortcomings: Firstly, antibody appreciation mainly depends on affinity between antibody and antigen. Secondly, it promotes high affinity antibody and inhibit low affinity antibody often result in the acquired solution falls into local optimally. Thirdly, the memory storehouse is only used when the initialize group generated during the following course.

In order to solve above problem, this paper has designed the improved immunity method. It includes optimizing the immunity election detector and group update tactics based on information entropy. The purpose of optimizing detector is to enable the detector distributes uniformly in the testing space, we must introduce an index to measure the uniformity coefficient of antibody distribution and take it as a measure to judge the effect of optimization. This measure can be used to guide the optimization operation of the antibody. The index of evaluation can be reflected through the uniformity coefficient of detector distributing in the space. In other words, system reflects it indirectly through the overlap quantity between detectors. In the evolutionary process, in order to avoid saving prematurely, we put the group update tactic based on information entropy to reflect the active interaction between antibodies.

The concrete steps of this algorithm are as follows:

1. Antigen discerned. System analyzes and understands the characteristic of question and its solution, it carries on the antibody coding.

2. Initial antibody population generation. Immunization algorithm is randomly initialized population, and chaos is leaded in. Chaotic motion is traversal and random, so it can traverse all the states without repeat according to its law in a certain range. If chaotic is used to generate the initial population, digital values will uniformly distribute in the solution space, and the data redundancy will be eased, the solution will be obtained at beginning of the iteration, so the search speed becomes fast. Here the famous logistic equation is used to generate the initial population.

3. Appraise antibodies. This algorithm regards information entropy as the index of affinity, and then it takes affinity of the antibody as the standard of appraising

antibody. The affinity between the antibody No. w and antibodies No. v is defined as:

$$a_{v,w} = \frac{1}{1 + M(N)} \tag{1}$$

Where $M(N)$ is information entropy between the antibody No. w and antibody No. v. When $M(N)$=0, that means their gene is same. The value of $a_{v,w}$ is between 0 and 1.

Similarly, the affinity between antibody and the antigen is defined as:

$$a_v = \frac{1}{1 + d_v} \tag{2}$$

Where d_v indicates the discrepancy degree between antibody and antigen. The value of a_v is between 0 and 1. When $d_v = 0$, $a_v = 1$, that states antibody and antigen are matching, the antibody is the optimal solution.

In the group evolutionary process, when some antibodies which are not the optimal solutions scale up to a certain degree, they will be easy to trap in the local convergence. Therefore, in order to prevent premature convergence, it is necessary to carry out its limitation. This algorithm poses the group update tactic based on information entropy to curb the antibody which is the larger scale but not the optimal solution.

4. The antibody group updates. The concentration of antibody v can be defined as:

$$c_v = \frac{1}{N}\sum_{w=1}^{N} ac_{v,w} \tag{3}$$

Where $ac_{v,w} = \begin{cases} 1 & \text{ay}_{v,w} \geq \text{Tacl} \\ 0 & other \end{cases}$, T_{acl} is a fixed threshold value.

Arranging the original antibody group as descending order of cv, and taking the previous N individuals to constitute a new antibody group. At the same time, system writes the previous m antibodies into the memory storehouse.

5. Repeat the above mentioned steps, until meet the condition of convergence. If it is satisfied, output the optimal result and finishing the algorithm, or roll down to the next step.

6. Election of immunity. The high concentration and high affinity antibody obtains the compensation of affinity is smaller; the antibody whose concentration is not high, but affinity is high, obtains the compensation of affinity relatively high. For the adjusted individual, reserving the antibody with high value of affinity, forsaking the low one. This process is immune choose.

7. Cross of immunity. Crossing operation can take the good basic of parent era gene to create the better offspring through information exchanging. According to the crossing probability, selecting two chromosomes A and B from the population as a parent era, choosing two non-zero and unequal gene-bit x and y, thus to gain crossing interval [x, y] or [y, x]; to find out the corresponding crossing interval in B, exchanging the genes within the two interval, and then after the genes repair, we have two new offspring individual A ' and B '.

8. Variation of immunity. According to the mutation probability, selecting a new individual S from the parent era population. Selecting two gene bits x1 and y1 randomly to form the variant interval [x1, y1] or [y1, x1], in this interval, generating an integer array whose maximum value is [x1-y1], according to the array, system recomposes the gene of the interval, then it form a new individual S '.

9. Seek the local optimization near the maximum. When the cross and the variation are over, the affinities of new population antibody and antigen are sequenced to seek the optimal solution, the binary domain that the optimal solution corresponded is converted to the original problem domain , chaotic iteration is carried out by logistic equations, find the better values to replace the optimal values, and then system translate them into binary domain.

10. Implement the rule of environment judgement. Determining whether the environment is similar to a previous one or not, if it is, abstracting m (m <S ') memory cells are from the corresponding memory storehouse of the environment in the memory pool (which can use memory storehouse several times), and system produces N-m New antibodies which constitute the initial group of the current environment; if not, then generating N antibodies which constitute the initial group, to turn to Step 2.

11. Satisfy the condition of convergence, algorithm is over.

4. Experiment and Analysis

Figure 11 is the acquisition of an image and the extraction process. Figure 12 is the training result of time for co-ordination mechanisms of image acquisition, image storage and image processing. This indicates that it meets requirements of the real-time acquisition, real-time storage and real-time processing. The image acquisition system of embedded FPGA for quadruped search robot is designed in Figure 13. Monitor effect is shown in Figure 14. After some parameter and program debugging, home vision monitor of quadruped robot is controlled effectively.

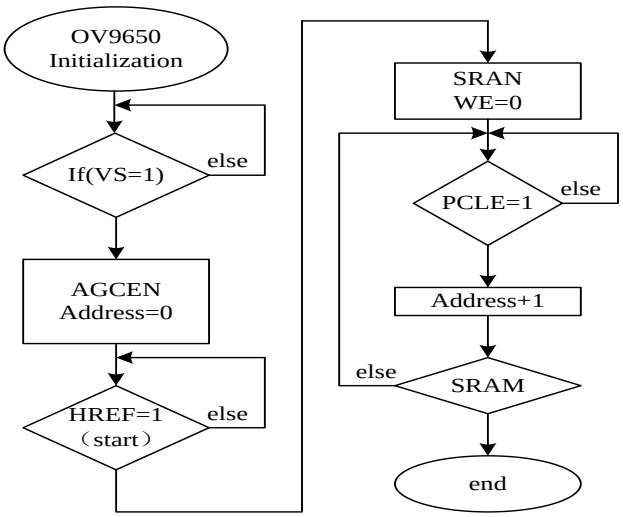


Figure 11. Acquisition of an Image and the Extraction Process

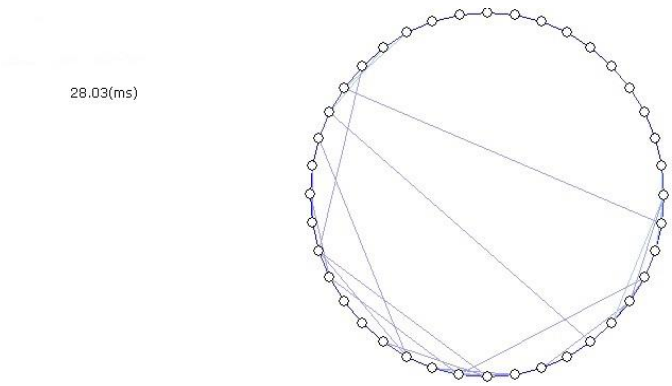


Figure 12. Training Result of Time for Co-ordination Mechanisms

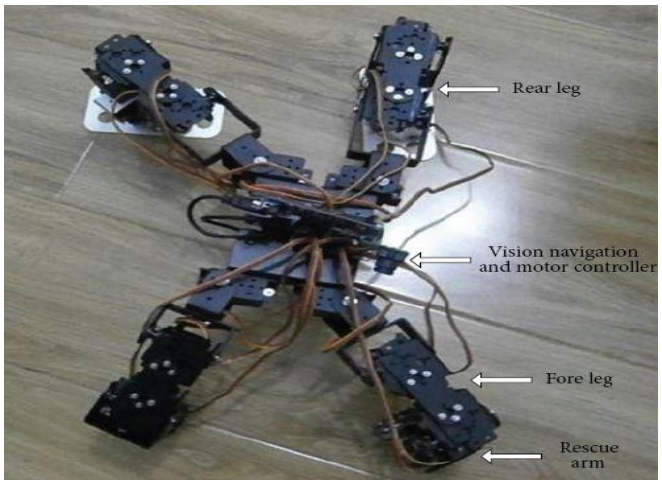


Figure 13. Quadruped Search Robot Monitor

Figure 14. Monitor Effect of Quadruped Search Robot

5. Conclusions

Aiming at the problems of stability and real-time for home vision monitor of the quadruped search robot, we put forward a new image acquisition system of FPGA in this paper. The development of FPGA technology, especially image acquisition module, makes this a competitive FPGA hardware architecture, and it is very suitable for image acquisition of quadruped search robot. Ping-pong operation design method is used to improve the acquisition speed based on FPGA. The host configures the slave machine through I2C bus to achieving data transmission. Co-ordination mechanisms of image

acquisition, image storage and image processing is designed to meet with buffer device. Our future research will focus on the problem of image processing algorithm based on FPGA.

Acknowledgments

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