International Journal of Smart Home
Vol. 10, No. 3, (2016), pp.131-138
http://dx.doi.org/10.14257/ijsh.2016.10.3.13

Voltage Scaling Based Wireless LAN Specific UART Design Based on 90nm FPGA

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Abstract

This research work emphasizes on the design of the wireless LAN specific UART. The frequencies that are standardized for the wireless LANs have been analyzed by scaling the voltage. The aim is to find out the most energy efficient specifications for the UART. After all the calculations, deduction comes over to a point that increasing the voltages increases the power consumption and therefore, the wastage gets elevated too. However, at lower values there is lesser wastage of power and hence the efficiency increases. Virtex-4 FPGA and WLAN standards have been focused upon to make the UART design. Xilinx software as well as the Verilog Hardware Description Language have been used for the purpose. The power consumption swings between 16% to 95.59% for different values of voltages at the specified WLAN frequencies. Various power loss parameters have been studied to get the most optimum operating condition for the UART.

Keywords: *Voltage Scaling, Wireless LAN, UART, 90nm, FPGA*

1. Introduction

We have analysed the volage scaling for the wireless LAN standards to eventually develop an energy efficient UART design. The frequncy standards for the WLAN have been specified in IEEE802.11. The standards are 802.11b for a frequency value of 2.4GHz, 802.11y for a frequency value of 3.6GHz, 802.11y public safety WLAN for a frequency value of 4.9GHz, 802.11a for a fequency value of 5GHz and 802.11p for the frequency value of 5.9GHz. UART is basically an asynchronous receiver transmitter which is used to rephrase the data between the parallel and serial forms. The word universal indicates that the speeds of transmision and the configuration of the data is reformable. We have basically worked on the 90nm UART technology, Virtex-4 which is extremely beneficial in terms of performance. We have employed the voltage scaling to obtain different results. Wireless LAN standards have been used to design the UART. UART supports the half duplex, full duplex as well as the simplex mode of the communication. We aim at finding that particular value of the standard WLAN frequency as well as the voltage at which the UART consumes the least power thereby proving to be of prime importance. FPGA (field programmable gate array) has been analyzed at different WLAN standards. FPGAs consume the least power and are the easiest to reprogramme. The power parameteters of the UART have been analyzed with respect to various frequency values as per the WLAN standards as well as the varying voltages. After the analysis we conclude that the UART behaves best at lower values of voltages as well as the standard WLAN frequncies. Therefore, the voltages should be kept as low as possible in order to have a maximum gain and least dissipation of the power.

ISSN: 1975-4094 IJSH

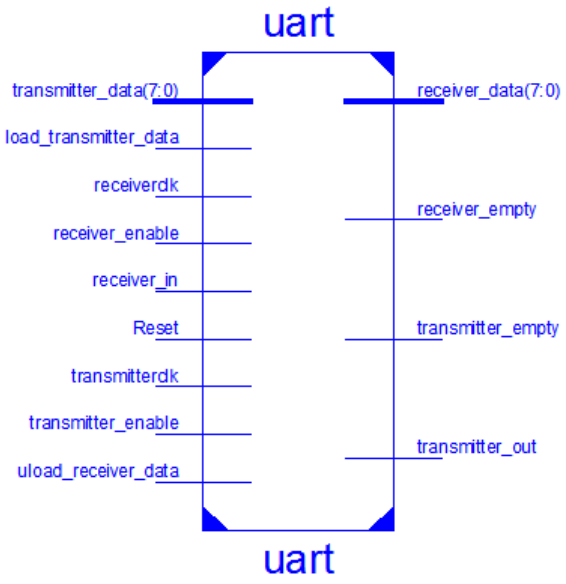

Figure 1. Universal Asynchronous Receiver Transmitter

As shown in Figure 1, the UART has 9 input ports enabling 8 bit data transfer and 4 output ports. These help in conversion of data from serial to parallel form and vice versa. Hence, this device is of prime importance in the field of communication.

2. Related Work

A researcher had worked on designing a mock up substructure for the wireless LANs using the antenna systems however we have used the wireless LAN to develop the UART design on 90nm FPGA technology [1]. An analyst had also developed a sensor network for the security related system using the FPGA technology. However, we focus on the designing of a voltage scaling based wireless LAN specific UART [2]. Another research scholar had worked on the energy efficiency issue in the wireless systems. Nonetheless, we have mainly considered the voltage scaling factor for the designing of the UART [3]. Some other researcher had designed a programmable cell array using rewritable electrolytic switch integrated in the 90nm CMOS whereas, we have mainly dealt with the 90nm FPGA technology [4]. Another researcher had worked on designing a voltage scaling based energy efficient design using the FPGA technology however we insist on the incorporation of the wireless technology as well in the design of our UART on the FPGA [5]. Another researcher had focused on making an FPGA based default simulator but we aim at developing a UART design based on the voltage scaling of a wireless LAN [6]. There are many other energy efficient techniques widely used in low power design [7-11].

3. Objective

The keen intent of the research is to design a UART with respect to the frequencies at which the wireless LANs are operable *i.e.*, 2.4GHz, 3.6GHz, 4.9GHz, 5.0GHz and 5.9GHz. The results have been scaled to varying values of the voltage that is 1V, 1.2V, 1.5V, 1.8V, 2.5V and 3.3V as shown in Figure 2. The values of all the forms of power are taken and the output is analyzed correspondingly. All the power consumption is tabulated and we notice that with the increase in the values of the voltage the clock, the logic the signal power, the I/O power, the leakage power as well as the total power consumption increases. Therefore, to entertain the minimum wastage and the maximum efficiency the

value of the voltage should be kept as less as possible. We aim at getting that combination of the parameters that ensures the minimum and the most efficient utilization of the resources.

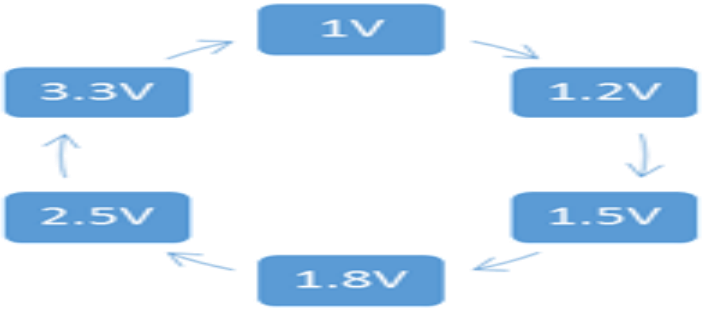

Figure 2. Different Voltage Taken Under Consideration

4. Results

Table 1. Results on 500MHz

Voltage	Clocks	Logic	Signal	I/O	Leakage	Total
1V	0.019	0.000	0.001	0.005	0.129	0.155
1.2V	0.028	0.001	0.002	0.005	0.165	0.201
1.5V	0.030	0.001	0.003	0.006	0.249	0.289
1.8V	0.038	0.002	0.004	0.007	0.381	0.430
2.5V	0.056	0.003	0.008	0.008	1.014	1.090
3.3V	0.081	0.005	0.013	0.010	2.950	3.060

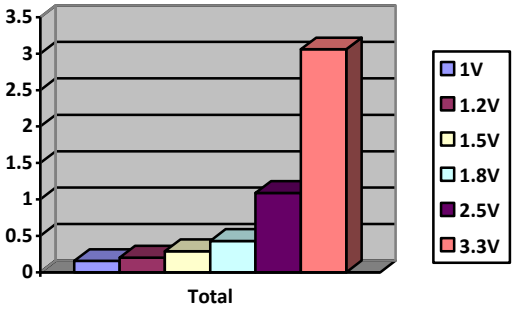

Figure 3. Total Power Consumption at Different Voltages and 500MHz

There is a fall of 76.54%, 65.43%, 62.96%, 53.08% and 30.86% in the clock power as the voltage is scaled down from 3.3V to 1, 1.2, 1.5, 1.8, 2.5V respectively. The logic power falls by 100%, 80%, 80%, 60% and 40%, the signal power diminishes by 92.30%, 84.61%, 76.92%, 69.23% and 38.46%, the I/O power reduces by 50%, 50%, 40%, 30% and 20%, the leakage power lessens by 95.62%, 94.4%, 91.55%, 87.08% and 65.62% and the total power goes low by a percentage of 94.93%, 93.43%, 90.55%, 85.94% and 64.37% as the voltage level is scaled down from 3.3V to 1, 1.2, 1.5, 1.8, 2.5V respectively as can be vividly concluded from Table 1. The comparison of total power consumption for different Voltage values is depicted in the Figure 3.

Table 2. Results on 2.4GHz (WLAN channel 802.11b)

Voltage	Clocks	Logic	Signal	I/O	Leakage	Total
1V	0.071	0.002	0.006	0.024	0.130	0.233
1.2V	0.092	0.003	0.008	0.026	0.167	0.297
1.5V	0.115	0.005	0.013	0.029	0.254	0.416
1.8V	0.144	0.008	0.018	0.032	0.393	0.595
2.5V	0.221	0.015	0.035	0.040	1.080	1.390
3.3V	0.323	0.025	0.061	0.048	2.951	3.409

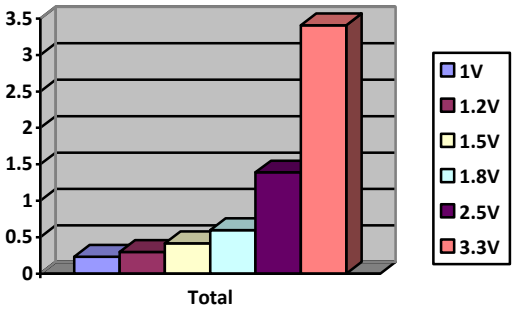

Figure 4. Total Power Consumption at Different Voltages and 2.4GHz

There is a fall of 78.01%, 71.51%, 64.39%, 55.41% and 31.57% in the clock power as the voltage is scaled down from 3.3V to 1, 1.2, 1.5, 1.8, 2.5V respectively. The logic power falls by 92%, 88%, 80%, 68% and 40%, the signal power diminishes by 90.16%, 86.88%, 78.68%, 70.49% and 42.62 %, the I/O power reduces by 50%, 45.83%, 39.58%, 33.33% and 16.66%, the leakage power lessens by 95.59%, 94.34%, 91.39%, 86.68% and 63.4% and the total power goes low by a percentage of 93.16%, 91.28%, 87.79%, 82.54% and 59.22% as the voltage level is scaled down from 3.3V to 1, 1.2, 1.5, 1.8, 2.5V respectively as can be vividly concluded from Table 2. The comparison of total power consumption for different Voltage values is depicted in the Figure 4.

Table 3. Results on 3.6GHz (WLAN channel 802.11y)

Voltage	Clocks	Logic	Signal	I/O	Leakage	Total
1V	0.102	0.003	0.008	0.036	0.130	0.280
1.2V	0.133	0.005	0.012	0.039	0.168	0.357
1.5V	0.166	0.008	0.019	0.044	0.257	0.494
1.8V	0.209	0.011	0.027	0.049	0.400	0.696
2.5V	0.322	0.022	0.053	0.060	1.123	1.578
3.3V	0.471	0.038	0.092	0.072	2.950	3.624

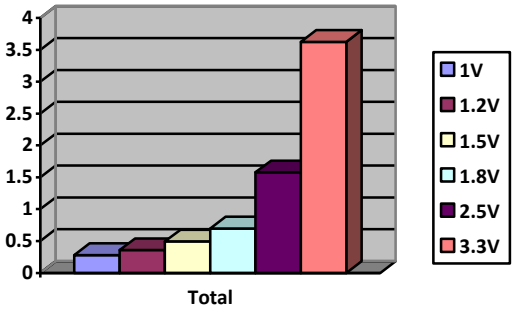

Figure 5. Total Power Consumption at Different Voltages and 3.6GHz

There is a fall of 78.34%, 71.76%, 64.75%, 55.62% and 31.63% in the clock power as the voltage is scaled down from 3.3V to 1, 1.2, 1.5, 1.8, 2.5V respectively. The logic power falls by 92.1%, 86.84%, 78.94%, 71.05% and 42.10%, the signal power diminishes by 91.30%, 86.95%, 79.34%, 70.65% and 42.39 %, the I/O power reduces by 50%, 45.83%, 38.88%, 31.94% and 16.66%, the leakage power lessens by 95.59%, 94.30%, 91.28%, 86.44% and 61.93% and the total power goes low by a percentage of 92.27%, 90.15%, 86.36%, 80.79% and 56.45% as the voltage level is scaled down from 3.3V to 1, 1.2, 1.5, 1.8, 2.5V respectively as can be vividly concluded from Table 3. The comparison of total power consumption for different Voltage values is depicted in the Figure 5.

Table 4. Results on 4.9GHz (802.11y Public Safety WLAN)

Voltage	Clocks	Logic	Signal	I/O	Leakage	Total
1V	0.136	0.005	0.011	0.049	0.131	0.332
1.2V	0.177	0.007	0.017	0.053	0.170	0.432
1.5V	0.222	0.011	0.026	0.060	0.260	0.578
1.8V	0.279	0.015	0.037	0.066	0.408	0.805
2.5V	0.430	0.029	0.072	0.081	1.172	1.785
3.3V	0.632	0.051	0.125	0.098	2.950	3.857

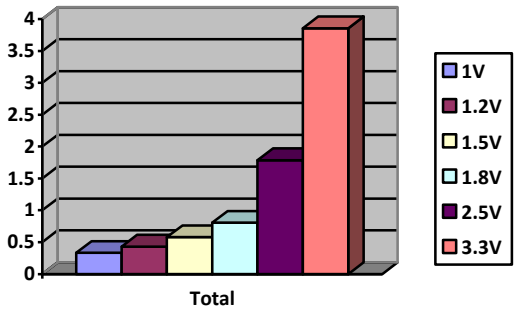

Figure 6. Total Power Consumption at Different Voltages and 4.9GHz

There is a fall of 78.48%, 71.99%, 64.87%, 55.85% and 31.96% in the clock power as the voltage is scaled down from 3.3V to 1, 1.2, 1.5, 1.8, 2.5V respectively. The logic power falls by 90.19%, 86.27%, 78.43%, 70.58% and 43.13%, the signal power diminishes by 91.20%, 86.40%, 79.2%, 70.40% and 42.4 %, the I/O power reduces by 50%, 45.91%, 38.77%, 32.68% and 17.34%, the leakage power lessens by 95.59%, 94.27%, 91.18%, 86.16% and 60.27% and the total power goes low by a percentage of 91.39%, 88.79%, 85.01%, 79.12% and 53.72% as the voltage level is scaled down from 3.3V to 1, 1.2, 1.5, 1.8, 2.5V respectively as can be vividly concluded from Table 4. The comparison of total power consumption for different Voltage values is depicted in the Figure 6.

Table 5. Results on 5GHz (WLAN channel 802.11a)

Voltage	Clocks	Logic	Signal	I/O	Leakage	Total
1V	0.139	0.005	0.012	0.050	0.131	0.336
1.2V	0.181	0.007	0.017	0.054	0.170	0.428
1.5V	0.226	0.011	0.026	0.061	0.261	0.585
1.8V	0.285	0.016	0.038	0.067	0.408	0.814
2.5V	0.439	0.030	0.073	0.083	1.176	1.801
3.3V	0.644	0.052	0.127	0.100	2.950	3.875

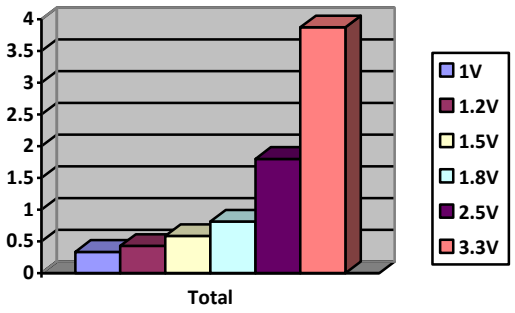

Figure 7. Total Power Consumption at Different Voltages and 5GHz

There is a fall of 78.41%, 71.89%, 64.90%, 55.74% and 31.83% in the clock power as the voltage is scaled down from 3.3V to 1, 1.2, 1.5, 1.8, 2.5V respectively. The logic power falls by 90.38%, 86.53%, 78.84%, 69.23% and 42.30%, the signal power diminishes by 90.55%, 86.61%, 79.52%, 70.07% and 42.51%, the I/O power reduces by 50%, 46%, 39%, 33% and 17%, the leakage power lessens by 95.56%, 94.23%, 91.15%, 86.16% and 60.13% and the total power goes low by a percentage of 91.32%, 88.95%, 84.90%, 78.99% and 53.52% as the voltage level is scaled down from 3.3V to 1, 1.2, 1.5, 1.8, 2.5V respectively as can be vividly concluded from Table 5. The comparison of total power consumption for different Voltage values is depicted in the Figure 7.

Table 6. Results on 5.9GHz (WLAN Channel 802.11p)

Voltage	Clocks	Logic	Signal	I/O	Leakage	Total
1V	0.162	0.006	0.014	0.059	0.131	0.372
1.2V	0.211	0.008	0.020	0.064	0.171	0.474
1.5V	0.265	0.013	0.031	0.072	0.263	0.643
1.8V	0.333	0.018	0.045	0.079	0.414	0.890
2.5V	0.514	0.035	0.086	0.098	1.212	1.945
3.3V	0.775	0.061	0.150	0.119	2.950	4.035

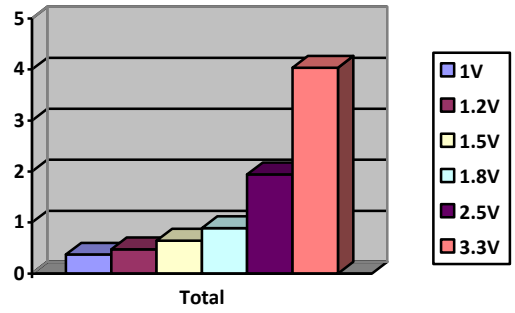

Figure 8. Total Power Consumption at Different Voltages and 5.9GHz

There is a fall of 79.09%, 72.77%, 65.80%, 57.03% and 33.67% in the clock power as the voltage is scaled down from 3.3V to 1, 1.2, 1.5, 1.8, 2.5V respectively. The logic power falls by 90.16%, 86.88%, 78.68%, 70.49% and 42.62%, the signal power diminishes by 90.66%, 86.66%, 79.33%, 70% and 42.66%, the I/O power reduces by 50.42%, 46.21%, 39.49%, 33.61% and 17.64%, the leakage power lessens by 95.59%, 94.20%, 91.08%, 86.16% and 58.91% and the total power goes low by a percentage of 90.78%, 88.25%, 84.06%, 77.94% and 51.79% as the voltage level is scaled down from 3.3V to 1, 1.2, 1.5, 1.8, 2.5V respectively as can be vividly concluded from Table 6. The

comparison of total power consumption for different Voltage values is depicted in the Figure 8.

5. Conclusion

We hereby conclude that with the increasing values of the voltages, all types of the power consumption be it the I/O power or the leakage power or the signal power increases. This leads us to a conclusion that the value of Voltages should be kept as small as possible at almost every possible value of frequency since with the increasing voltages the power consumption increases as proven by the results in Tables 1-6. The increase in power consumption varies between 16% to 95.59% when the voltage is scaled up from 1V to 3.3V at different values of the frequencies. Using the lower values of voltage would lessen the power consumption and would produce the most desirable outputs thereby increasing the efficiency. This would help us extract the maximum out of the UART, making the excessive power consumption issue to recede to the background. A special care is being taken for the minimal utilization of the energy resources. These days when power consumption is a major point of concern, designing a UART with lower values of the voltages would prove to be an asset in the field of the engineering since there would be no extravagancy at least in terms of the power consumption thereby coping up with the modern day communication demands.

6. Future Scopes

With the advancement in technology, the 2D IC FPGA could in the near future be replaced by some 3D IC which would aid in the advancement of the precision factor. Also, instead of the voltage scaling, results could be analyzed for various other parameters like resistive scaling or the capacitive scaling *etc*. The wireless LANs that have been analyzed as a part of this research could be replaced by some other, more advanced means of communication in the near succeeding times. Also, the 90nm technology could be replaced by a newer one. Even today 28nm technology is being used. 90nm might soon get outdated. Also analysis could also be carried out for a variety of networking devices like the routers, bridges and switches instead of the UART. This would open up a new chapter in the era of the advancement and efficient utilization of the resources in the communication field.

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