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Voltage Based Energy Efficient Mobile Charge Sensor Design Using LVCMOS

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Abstract

In this paper an approach is made to design the voltage based energy efficient mobile charge sensor design and for that reason we have used LVCMOS IO standards. Power dissipation is the major factor that has been analyzed and focused .Voltage sensor is operating at different frequencies and at fix temperature that is 25 degree Celsius. Frequencies of different mobile phones have been evaluated. Frequencies taken in consideration are 1400MHz for Nokia Lumia710, 1.2 GHz for Samsung Galaxy core, 2100 MHz for iphone6, 1700 MHz for HTC/T, 1800 MHz for micromax X091 and 2.2GHz for Song Xperia Z1. This research work, is basically done to check the charging status of a mobile phone. The coding is done in Verilog on 28nm FPGA that is Kintex-7. Kintex7 is 28-nm FPGA on which we implement our circuit to re-assure power reduction and reduction in junction temperature in sequential circuit.There is 4-19% reduction in power dissipation with LVCMOS33, 3-15% reduction in power dissipation with LVCMOS25, 2-13% reduction in power dissipation with LVCMOS18, 2-12% reduction in power dissipation with LVCMOS15, 1-5% reduction in power dissipation with BLVDS25 at 25 degree Celsius when we use 28nm FPGA. The performance of our sensor is evaluated and tested through simulations on Xilinx software development kit. . The quality of our sensor can be improved by changing IO standards.

Keywords*: Mobile Charge Sensor, energy efficient, LVCMOS, Power Dissipation*

1. Introduction

Our voltage based energy efficient mobile charge sensor design is implemented on 28nm Kintex7 FPGA. In this work, we studied mobile charge sensor design using LVCMOS.High performance mobile charge design is current research area. But, there is no specific work in energy efficient charge sensor design is taken under consideration by current research.

The paper is stressed upon a voltage based efficient fire sensor using four different kinds of Stub Series Terminated Logic (SSTL)IO standards[1].In our work, we are operating our sensor at 25 degree Celsius with different IO standards of LVCMOS family that are LVCMOS33. LVCMOS15, LVCMOS18, LVCMOS25, BLVDS2515.This paper discussesthe use of supercapacitors to power mobile phones[2].A specific charging scheme for the design is alsoproposed and simulated, enabling fast and efficient charging of the mobile device[2]. We have evaluated our design on Xilinx software on 28nm Kintex-7 FPGA due to its fast speed and it can be more improved by using different IO standards. The choice of various IO Standards [3] like LVCMOS33, LVCMOS15, LVCMOS 18, LVCMOS25 and BLVDS25 depends on our implementation purpose. We can also use other IO standards like SSTL15, HSTL_I, HSLVDCI_15, LVDC1_DCI_DV2_18 and many others. IO standards helpsus to achieve significant energy efficiency. The performance is evaluated by performing simulations on a magnetic recording channel [4]. We have designed our sensor and simulated on Xilinx software. For mobile applications a single-chip image sensors is realized in a standard 0.35-μm

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CMOS technology [5].There is already work is going on in power dissipation in a decoder[6], Internet of Things enabled decoder design[7] and energy efficient traffic light controller [8].To check the amount of charge left in the battery can be tested by considering the voltage. We have coded the logic in Verilog. Considering a mobile phone model like Nokia Lumia 530 maximum voltage in a battery is 3.7V. And if the voltage when we are charging it exceeds 3.7V it is considered to be overcharged. We have designed our mobile charge sensor by setting the limits if the voltage present in the battery is between 3 to 3.7 it is considered to be full charge, when the voltage is in between 2 to 3 it is optimal charge, when the voltage is in between 1-2 it is medium charge, when the voltage is in the range of 0 to 1 it is said to be low charging and if it approaches to 0 it is said to be discharged this can be shown in tabular form given below.

Voltage Level(V)	Status
>3.7	Over charged
3-3.7	Full charge
2-3	Optimal charge
1-2	Medium charge
0-1	Low charge
0	discharge

2. Power Analysis

A. IO Power Analysis on 28nm FPGA for LVCMOS33

Table 1. Power Dissipation at 25 Degree Celsius at Different Frequencies for LVCMOS33 IO STANDARD

Frequency	Power Dissipation
1400 MHz	0.110
1.2 GHz	0.105
2100 MHz	0.127
1700 MHz	0.117
1800 MHz	0.120
2.2GHz	0.129

From the above table we came across the results that minimum power dissipation is when frequency is 1.2GHz and maximum power dissipation is at 2100 MHz.

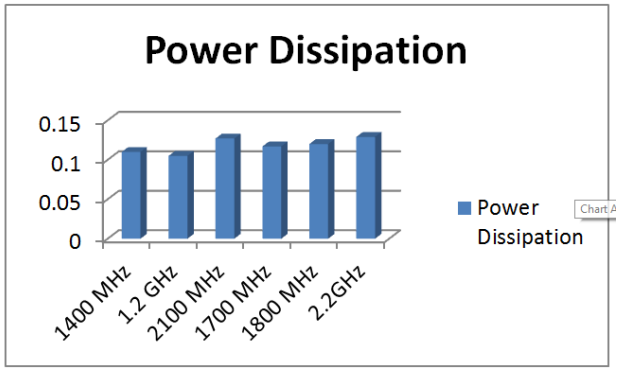

Figure 1. Power Dissipation at 25 Degree Celsius at Different Frequencies for LVCMOS33 IO STANDARD

There is 4.54% reduction in power dissipation with 1400 MHz, 13.38% reduction in power dissipation with 2100MHz, 10.25% reduction in power dissipation with 1700MHz, 12.5% reduction in power dissipation with 1800MHz ,18.60% reduction in power dissipation with 2.2 GHz with respect to 1.2 GHz when we use 28nm FPGA for LVCMOS 33as shown in Table 1 and Figure 1.

B. IO Power Analysis on 28nm FPGA for LVCMOS25

Table 2. Power Dissipation at 25 degree Celsius at different frequencies for LVCMOS25 IO STANDARD

Frequency	Power Dissipation
1400 MHz	0.100
1.2 GHz	0.097
2100 MHz	0.112
1700 MHz	0.106
1800 MHz	0.107
2.2GHz	0.114

From the above table we came across the results that minimum power dissipation is when frequency is 1.2GHz and maximum power dissipation is at 2100 MHz.

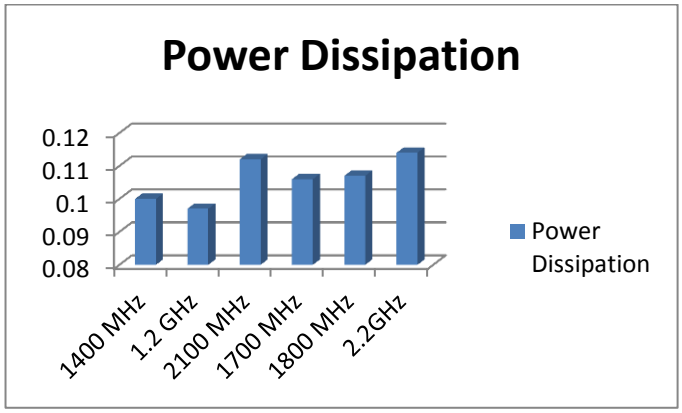

Figure 2. Power Dissipation at 25 Degree Celsius at Different Frequencies for LVCMOS25 IO STANDARD

There is 3% reduction in power dissipation with 1400 MHz, 13.39% reduction in power dissipation with 2100MHz, 8.49% reduction in power dissipation with 1700MHz, 9.34% reduction in power dissipation with 1800MHz ,14.91% reduction in power dissipation with 2.2 GHz with respect to 1.2 GHz when we use 28nm FPGA for LVCMOS25as shown in Table 2 and Figure 2.

C. IO Power Analysis on 28nm FPGA for LVCMOS18

Table 3. Power Dissipation at 25 Degree Celsius at Different Frequencies for LVCMOS18 IO STANDARD

Frequency	Power Dissipation
1400 MHz	0.094
1.2 GHz	0.092
2100 MHz	0.103
1700 MHz	0.098

1800 MHz	0.100
2.2GHz	0.105

From the above table we came across the results that minimum power dissipation is when frequency is 1.2GHz and maximum power dissipation is at 2.2 GHz.

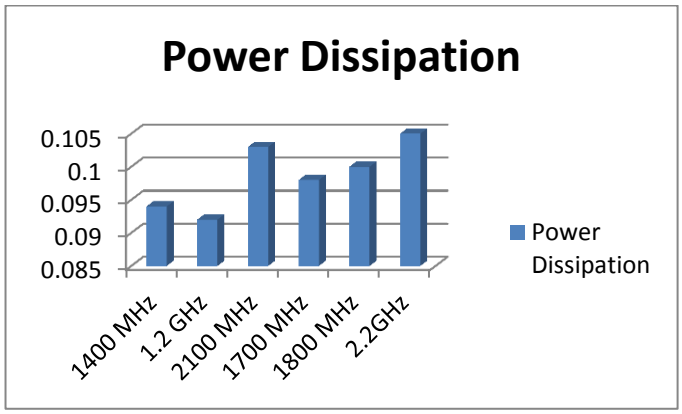

Figure 3. Power Dissipation at 25 Degree Celsius at Different Frequencies for LVCMOS18 IO STANDARD

There is 2.12% reduction in power dissipation with 1400 MHz, 10.67% reduction in power dissipation with 2100MHz,6.12% reduction in power dissipation with 1700MHz, 8% reduction in power dissipation with 1800MHz ,12.38% reduction in power dissipation with 2.2 GHz with respect to 1.2 GHz when we use 28nm FPGA for LVCMOS18as shown in Table 3 and Figure 3.

D. IO Power Analysis on 28nm FPGA for LVCMOS15

Table 4. Power Dissipation at 25 Degree Celsius at Different Frequencies for LVCMOS15 IO STANDARD

Frequency	Power Dissipation
1400 MHz	0.092
1.2 GHz	0.090
2100 MHz	0.100
1700 MHz	0.096
1800 MHz	0.097
2.2GHz	0.102

From the above table we came across the results that minimum power dissipation is when frequency is 1.2GHz and maximum power dissipation is at 2.2 GHz.

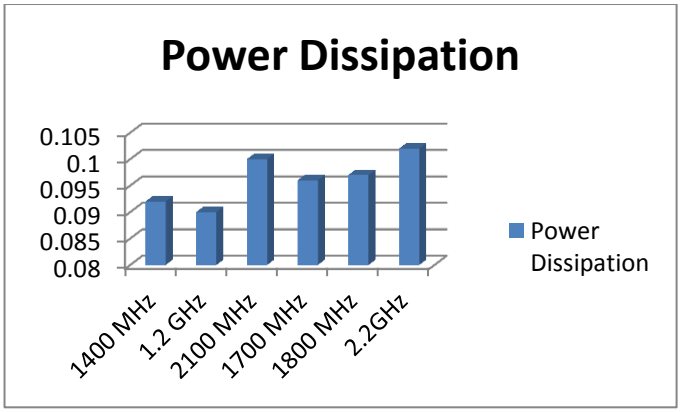

Figure 4. Power Dissipation at 25 Degree Celsius at Different Frequencies for LVCMOS15 IO STANDARD

There is 2.1% reduction in power dissipation with 1400 MHz, 10% reduction in power dissipation with 2100MHz, 6.25% reduction in power dissipation with 1700MHz, 7.21% reduction in power dissipation with 1800MHz ,11.76% reduction in power dissipation with 2.2 GHz with respect to 1.2 GHz when we use 28nm FPGA for LVCMOS15as shown in Table 4 and Figure 4.

E. IO Power Analysis on 28nm FPGA for BLVDS25

Table 5: Power Dissipation at 25 Degree Celsius at Different Frequencies forBLVDS25 IO STANDARD

Frequency	Power Dissipation
1400 MHz	0.299
1.2 GHz	0.296
2100 MHz	0.308
1700 MHz	0.303
1800 MHz	0.304
2.2GHz	0.309

From the above table we came across the results that minimum power dissipation is when frequency is 1.2GHz and maximum power dissipation is at 2.2GHz.

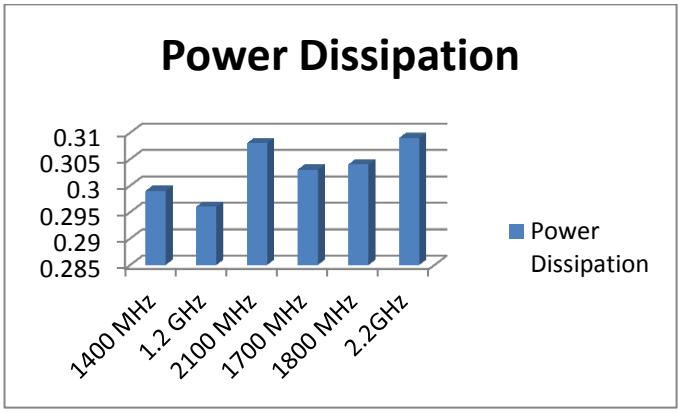

Figure 5. Power Dissipation at 25 degree Celsius at Different Frequencies for BLVDS25IO STANDARD

There is 1% reduction in power dissipation with 1400 MHz, 3.89% reduction in power dissipation with 2100MHz, 2.31% reduction in power dissipation with 1700MHz, 2.63% reduction in power dissipation with 1800MHz,4.20% reduction in power dissipation with 2.2 GHz with respect to 1.2 GHz when we use 28nm FPGA for BLVDS25 as shown in Table 5 and Figure 5.

F. IO Power Analysis on 28nm FPGA for Different IO STANDARDS

Table 6. Power Dissipation at 25 Degree Celsius at Different Frequencies for Different IO STANDARDS

Frequency	LVCMOS33	LVCMOS25	LVCMOS18	LVCMOS15	BLVDS25
1400 MHz	0.110	0.100	0.094	0.092	0.299
1.2 GHz	0.105	0.097	0.092	0.090	0.296
2100 MHz	0.127	0.112	0.103	0.100	0.308
1700 MHz	0.117	0.106	0.098	0.096	0.303
1800 MHz	0.120	0.107	0.100	0.097	0.304
2.2 GHz	0.129	0.114	0.105	0.102	0.309

There is 4-19% reduction in power dissipation with LVCMOS33, 3-15% reduction in power dissipation with LVCMOS25, 2-13% reduction in power dissipation with LVCMOS18, 2-12% reduction in power dissipation with LVCMOS15, 1-5% reduction in power dissipation with BLVDS25 at 25 degree Celsiuswhen we use 28nm FPGA shown in Table 6 and Figure 6.

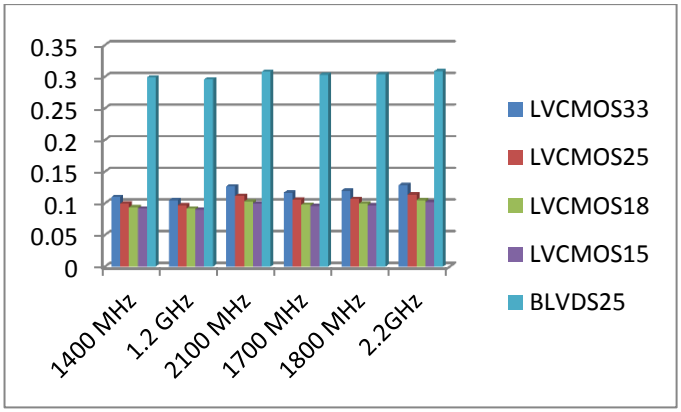

Figure 6. Power Dissipation at 25 Degree Celsius at Different Frequencies for Different IO STANDARDS

3. Conclusion

Our voltage based energy efficient mobile charge sensor design is implemented on 28nm Kintex7 FPGA.We came across the results that the least power dissipation is found when the frequency is 1.2 GHz and there is 4-19% reduction in power dissipation with LVCMOS33, 3-15% reduction in power dissipation with LVCMOS25, 2-13% reduction in power dissipation with LVCMOS18, 2-12% reduction in power dissipation with

LVCMOS15, 1-5% reduction in power dissipation with BLVDS25 at 25 degree Celsius when we use 28nm FPGA. From the above data least power dissipation range is 1-5% and is when we use BLVDS25 and maximum power dissipation range is 4-19% when we use LVCMOS33.

4. Future Scope

In our research work, Voltage Based Energy Efficient Mobile Charge Sensor Design Using LVCMOS is basically designed to sense the battery of a mobile phone we have implemented our schematic on 28nm FPGA that is Kintex-7. we can further extend our research by using other FPGA families like automotive Artix7, automotive Coolrunner2, automotive Spartan, automotive Spartan-3A DSP, automotive Spartan 3A, automotive Spartan 3E, automotive Spartan6, Spartan3, Spartan3E, Spartan low power, Kintex7 low voltage, Virtex5, Virtex4, Virtex6 and many others. We have focused only at 25 degree Celsius we can further change the temperature and enhance the quality of our charge sensor. Here, we are using LVCMOS I/O standard, there is wide scope to use other I/O standards like LVDCI, SSTL, HSTL, and LVTTL.

References

[1] T. Kumar, "Simulation of voltage based efficient fire sensor on FPGA using SSTL IO standards." Robotics and Emerging Allied Technologies in Engineering (iCREATE), 2014 International Conference on. IEEE, **(2014)**.
[2] J. Monteiro, N. Garrido, and R. Fonseca, "Efficient supercapacitor energy usage in mobile phones", *2011 IEEE International* Conference on Consumer Electronics-Berlin (ICCE-Berlin), **(2011)**.
[3] B. S. Chowdhry, B. Pandey, T. Kumar, T. Das, "Mobile DDR IO Standard Based High Performance Energy Efficient Portable ALU Design on FPGA", Springer Wireless Personal Communications, An International Journal, vol. 76, no. 3, **(2014)**, pp. 569-578.
[4] M. M. Mohammad , and R. S.Naresh. "High-throughput LDPC decoders", Very Large Scale Integration (VLSI) Systems, IEEE Transactions, vol.11, no. 6, **(2003)**, pp. 976-996.
[5] K. Yoon, "Single-chip CMOS image sensor for mobile applications", Solid-State Circuits, IEEE Journal, vol. 37, no. 12, **(2002)**, pp. 1839-1845.
[6] S. Madhok, A. Kaur and B. Pandey "Different IO Standard Based Energy Efficient Decoder Design For 64-bit Processor Architecture", IEEE International Conference "Computing for Sustainable Global Development (INDIACOM), Bharti Vidyapeeth, Delhi, **(2015)**, pp. 11-13.
[7] S. Madhok, S. Chakrabarti and B. Pandey, "Internet Of Things (IoTs) Enable Decoder Design For Wireless Sensor Network", IEEE International Conference on "Computing for Sustainable Global Development (INDIACOM), **(2015)**; Bharti Vidyapeeth, Delhi.
[8] S. Madhok, B. Pandey, "Energy Efficient Traffic Light Controller Design on FGPA ", IEEE International Conference on "Computing for Sustainable Global Development (INDIACOM), **(2015)**; Bharti Vidyapeeth, Delhi.

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