

Circuit Module Design of High-Voltage Side for Optical Current Transformer

Ying Zhang¹, Shenghui Wang¹, Xuejie Wang^{2,1} and Lei Qi^{3,4}

¹Shenyang Institute of Engineering, Shenyang 110136, China

²Harbin Institute of Technology, Harbin 150001, China

³Shenyang University of Technology, Shenyang 110023, China

⁴Liaoning Provincial Institute of Safety Science, 110004, China

wangxuejie-1985@163.com

Abstract

The Field Programmable Gate Array (FPGA) technology has been used for designing the signal processing circuit of A/D device, CRE code and Manchester module of high-voltage side for optical current transformer in this paper. The A/D controlling module, CRC code module, Manchester encoding module and the storage in FPGA has been designed and simulated. The signal processing circuit design program of high-voltage side for optical current transformer in this paper has been proved from the simulating results and can meet the requirements of optical current transformer on communication of data, which is rapid and reliability.

Keywords: Optical current transformer; CRC; Field Programmable Gate Array; Manchester code

1. Introduction

The current transformer (CT) is a significant equipment for the relay protection and the current measurement in power system. The accuracy and reliability of CT have a great influence on security, stability and economic operation. With the development of electric power, the increasing capacity of a generator, and the rise of the grid voltage, many new and stricter requirements are made for the emerge of the mutual inductor, while the traditional electromagnetic transformers cannot meet. Based on optical technology, electronic technology and modern signal processing technology, a new generation of optical current transformer overcomes a series of problems, which involve magnetic saturation and ferromagnetic resonance of the traditional current transformer. Combined with a new type of optoelectronic technique, with incomparable advantages, such as high precision and intelligence, the potential applications of the new generation of optical current transformer are brilliant. At present, a main research direction of hybrid optical current transformer (HOCT) is active electronic current transformer (ECT), which is composed of the high voltage side, the low voltage side and power supply.

The high voltage side mainly includes sensor and circuit module. Primarily, sensor adopts the Rogowski Coil. The high voltage side circuit module includes integrator, amplifier, a low-pass filter, A/D converter and embedded micro-controller. High voltage side circuit module is an important component of the current transformer. The main performance parameters are vital to the current transformer such as its precision, transient response speed and power consumption.

2. High Voltage Side Circuit Module Design

The traditional high voltage side circuit module is made by signal process circuit, A/D converter, Multi-point control unit (MCU), CRC unit and Manchester encoding unit *etc.*

As a main control unit of high voltage side, multi-point control unit (MCU) mainly reflects the transient response speed and power consumption, the choice of which can be DSP and MCU. DSP with high speed power, as well as, low power consumption MCU is difficult to meet the requirements in terms of speed. With the continuous development of large scale of integrated circuit technology and computer technology, FPGA (Field programmable Gate Array) as the current popular embedded chip has the advantages which cannot be substituted by other chips, becoming today's most widely used application specific integrated circuit. In this paper, the functions of A/D control module, CRC code module and Manchester encoding unit are merged into the FPGA. The inner block diagram of FPGA is shown in Figure 1.

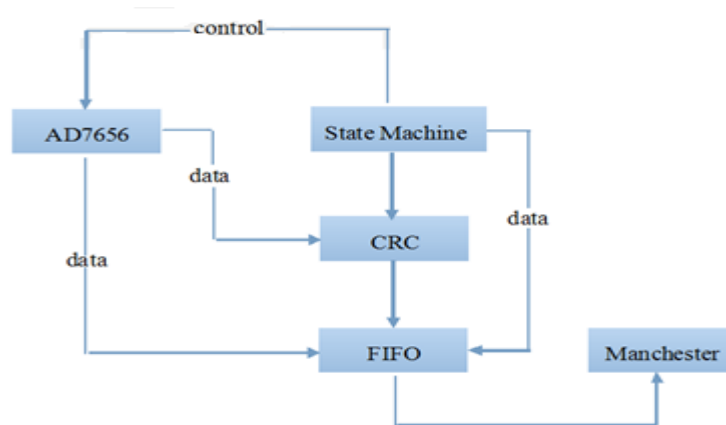


Figure 1. General Serial Principle of CRC

This latest version of AD7656 from ADI in 2006 is a six channel 16-bit successive approximation ADC. The chip is based on COMS technique, which combines the high voltage semiconductor technology and submicron COMS together with complementary bipolar process. The more signal link features are integrated in a chip by ICOMS device, the size of which is smaller than before, with the advantages of significantly low power consumption, small packaging size and improving chip performance etc, which can satisfy the need of high resolution, multi-channel and low power consumption in industrial field.

The power consumption of AD7656 is only 160milliwatts. In power saving mode, power down to 16.5milliwatts, the power consumption of AD7656 reduces by 60% in comparison with the same kind of bipolar input ADC. Under the sampling rate of 250 KSPS per channel, the accuracy is 2 times of similar products. And the voltage sampling rate is 250 KSPS when supply voltage is 5V. As the maximum sampling error is plus or minus 1.2 percentage points, the input frequency is 8MHz of sample-and-hold amplifier in chip.

The six-way analog input of AD7656 is divided into three groups, start-up control done by CONV STA, CONV STB and CONV STC. Each input has a track-and-hold amplifier to achieve the function of simultaneous sampling and conversion in the channel, which is very suitable for the need of multi-channel acquisition system. AD7656 provides optional high-speed parallel or serial interface in the direct connection with the microprocessor (MCU) or digital signal processor (DSP).

The maximum working frequency of the AD7656 is up to 5 MHz, sampling/conversion completed in 16 conversion cycles. AD7656 six channels can simultaneously complete sampling/converting, throughput rate up to 250 KSPS. According to internal reference voltage of 2.5V, bipolar analog input range of AD7656 can be plus or minus 10V or 5V. Or according to the external reference voltage for different range of bipolar analog input

signal, AD7656 is with 85db common-mode rejection of the differential input channels, as well as six 3 μ s successive approximation analog-to-digital converters and six differential sample amplifiers. There are positive 2.5V reference voltages in internal of the REF IN and FER OUT pin. The differential input of AD7656 can change between negative VREF to positive VREF, three transformations making signal CONV STA/B/C start a given channel. When the enable signals of three transformations are gated at the same time, the conversion results will be stored in the six registers. For each read operation, all the output of AD7656 are 16-bit data. The AD7656 has a low noise, broadband tracking to keep the amplifier process signals with the input frequency up to 8 MHz, the typical time of track and hold circuit to 20ns, which can make six A/D converters synchronously sample. The functional block diagram of the AD7656 is shown in Fig.2.

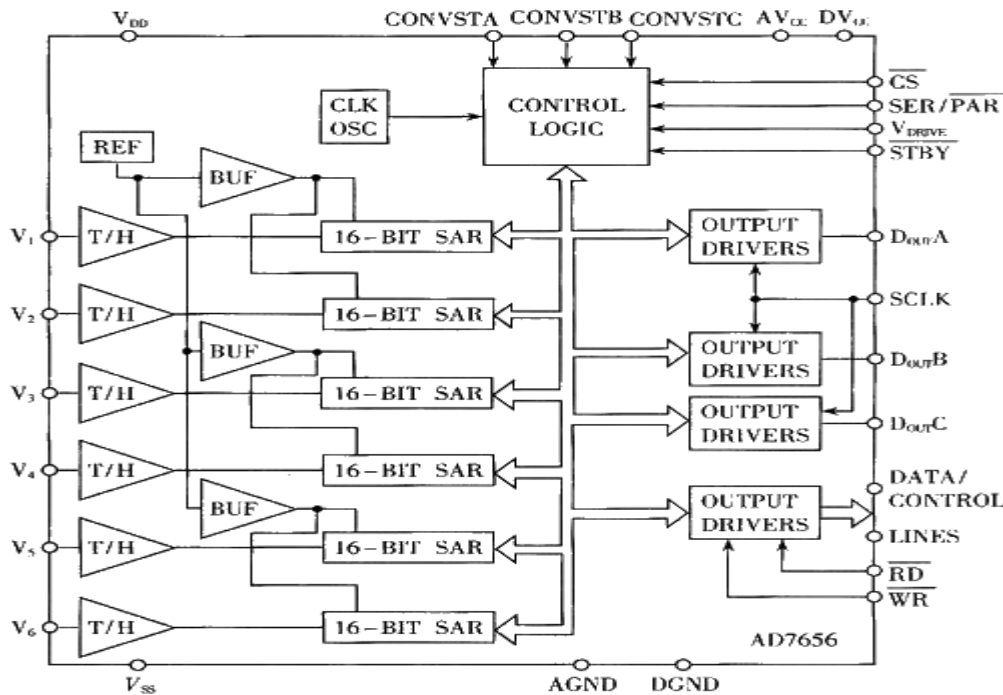


Figure 2. AD7656 Functional Block Diagram

The internal conversion timing diagram of AD765 is shown in figure 3. After three CONVST pins connecting together, six A/D converters can sample simultaneously. The rising edge of CONVST triggering A/D conversion, the conversion time is 3 μ s. In the conversion process, the BUSY signal keep high level until the end of the transformation, the BUSY signal converting from high to low, system into tracking mode and transformation results stored in the output data register. When keep low level constant of the choosing signal, the low level of consecutive six read signals can read transform data of six A/D converters in turn.

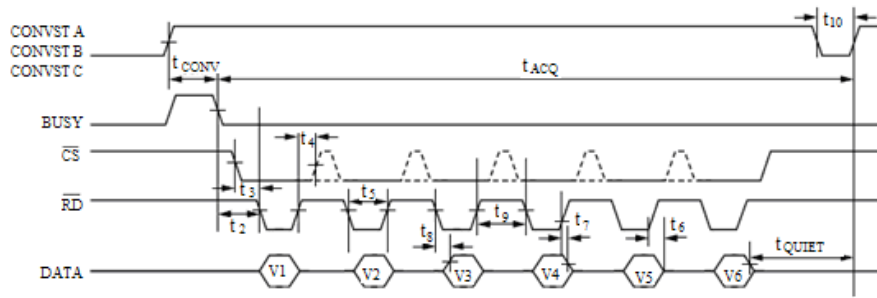


Figure 3. AD7656 Timing Diagrams Diagram

The signal processing circuit in the high voltage side is an important component of the optoelectronic current transformer, whose accuracy, transient response speed and main performance parameters such as power consumption have a significant impact on transformer. The precision includes all that of components in the high side, the most important parts of which are the sensor and the A/D converter. The transient response speed is the speed with which transformers respond to transient conditions of bus. In the high-voltage side, the transient response speed mainly depends on the conversion rate of the A/D converter and the processing speed of the microprocessor. As the largest integrated circuit modules, the A/D converter, microprocessor and code circuit are the chief sources of power consumption of the high-voltage side.

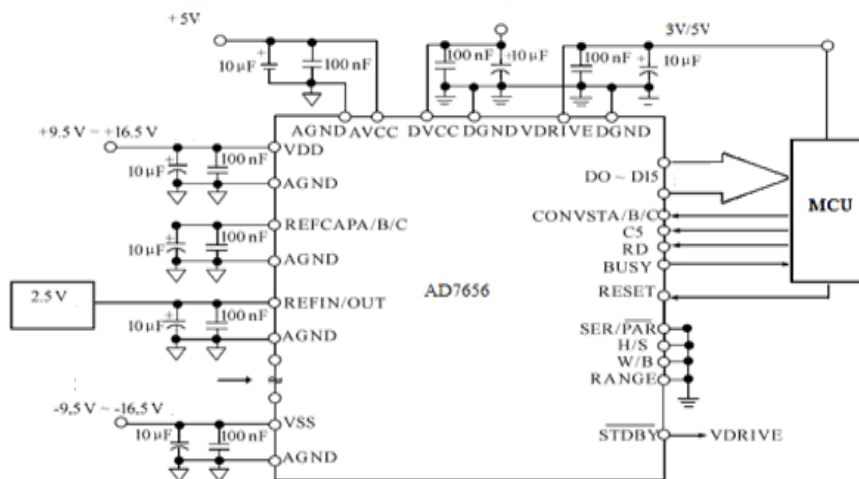


Figure 4. AD7656 Parallel Connection Periphery Circuit Diagram

The application of the AD7656 in optoelectronic current transformer, the selection of sampling frequency varies according to the specific requirements of the system. The electronic current transformer is required in the transient case collecting 13 harmonics, this is, the waveform with frequency of 650Hz. If a cycle with 40 sampling points, it requires the conversion rate is more than 26k, but the sampling rate of AD7656 is 250k, which is more than 26k. As for the power consumption, the power consumption of AD7656 is 140mW in the case of full sampling rate operation, which is quite low in the similar chip. Therefore AD7656 can completely meet the requirements of the signal processing circuit in photoelectric transformer high voltage side. In the signal processing circuits of photoelectric transformer high voltage side, the role of microprocessor MCU is to control ADC chip to process an uniform time sampling of voltage signals in the secondary side of the Rogowski Coil. After each time the conversion, ADC conversion

results are received by parallel lines, the parallel data into serial, while the Manchester encoded serial data output.

2.1. The Control of A/D via System States

A/D converter is the important device in the whole system. This paper uses six input-channel simultaneous sampling A/D converters AD7656, which manufactured by ADI. In the design, FPGA implements to control over AD7656 and literacy timing by the state machine. In this paper, the control process is divided into four states, *ST0*, *ST1*, *ST2*, *ST3* respectively. *ST0*: A/D initialization, *ST1*: start the conversion and wait the end of conversion, *ST2*: finish conversion and get ready to read data, *ST3*: read data and control of counter.

2.2 The Design of the Storage in FPGA Chip

In this paper, a 16-bit FIFO is designed for data storage in the internal FPGA by VHDL language, the structure diagram of chip memory as shown in Figure 5. In the diagram, the data for the data input, *Wreq* for a control signal, *Rdreq* to read the line of control, *q* for the data output, Clock of the clock, *Usedw* to address signal output line.

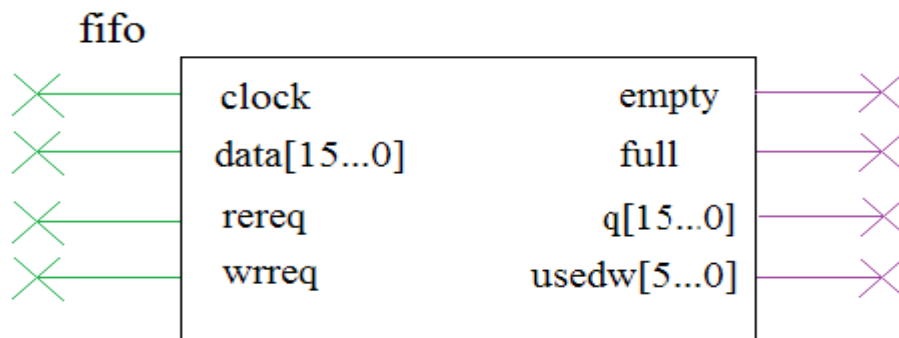


Figure 5. RAM Structure Diagram

2.3. CRC Checksum for the FPGA Design

In the process of optical fiber communication, the receiver can determine whether the data are correct by a variety of detection methods. Currently, the cyclic redundancy check (CRC) is one of the most widely used check coding methods and powerful detection means in such aspects as the network communication and the storage. When the technique is used in several digital communication systems, the performance has been greatly improved. In order to satisfy the requirement of quickness and reliability of electric power communication, this paper adopts parallel CRC algorithm to implement the CRC encoding.

The principle of the CRC check code is that the sender uses CRC algorithm to calculate the CRC check code of sent data, attached at the end of the sent data, that is, at the same time of adding CRC code (coding process). After the data has been sent, the receiver computer starts to check whether the mathematical relationship is correct between data and the CRC code (decoding process). If not correct, it means that the data information has error code during transmission.

FPGA has become today's the most widely used programmable dedicated device, which solves the encountered many problems in the traditional design of digital circuit, able to quickly and flexibly implement complex digital system design. In this paper, the development software is Max + plus II, realizing test algorithm of CRC by VHDL

language, as well as, conducting simulations of a set of random hexadecimal number. The simulation results as shown in Fig.6, the data not only accurately reflect the array of CRC check code, but also get the smooth waveform by optimization. Simulation results show that the development software has come to an anticipated result.

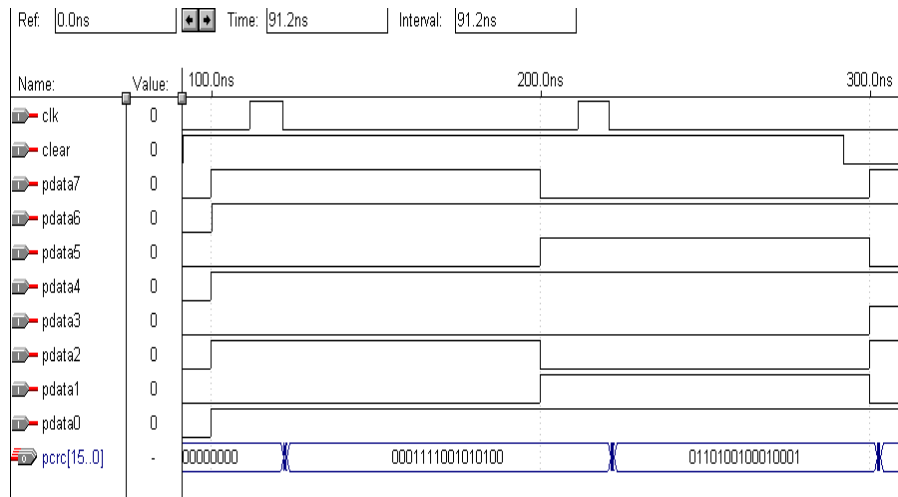


Figure 6. CRC Simulation Results Diagram of VHD

2.4. The Realization of Manchester Code

It is not practical to timing recovery by asynchronous methods, as optical fiber allowing quick data transmission over long distances. If the clock signal could not recover from the data at the receiving end, another optical fiber is needed to transmit the clock, which is uneconomic and time base swing. To choose the right line code, Manchester code is the most commonly used in the modern optical fiber transmission system.

Also known as bi-phase data coding, Manchester code is often expressed as level jump to represent the transmission of binary information in the center of code elements. The element level jump is a kind of clock synchronization encoding technology. The method of Manchester code encoding is that each element is divided into two equal intervals. Then 0 is encoded as a low-high transition and a 1 as a high-low transition. Its advantage is that a level conversion appears in the middle of each element, which not only prevents the base-band signal with a succession of "1" or "0"but also is very beneficial to extract a synchronous signal on the receiving end. In the actual process of circuit design, the xor gate is used to the design of coding. This paper uses the D flip-flop to eliminate the burrs that are caused by the clock signal rise time and fall time in the encoding process.

In this paper, the Manchester coding circuit is simulated. As shown in Fig.7, the hops of output signal appear in the center of the input signal. It is successful to complete the coding, as smooth signal without burrs.

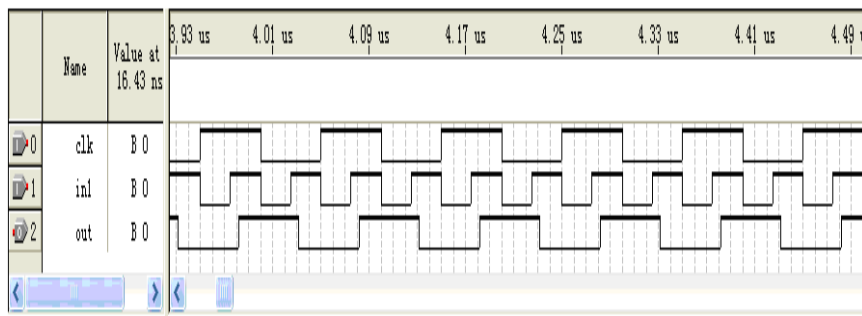


Figure 7. Manchester Simulation Results Diagram

2.5. Integrated Modules of MCU

Each main module in figure 1 is already compiled and simulated by VHDL language. It is concluded that each module has completed its own function from the simulation results. But sequential logic synthesis of FPGA is a very complicated work. There is a lot to think about, especially how to combine the functions of various modules together to complete the function of the whole system and how to match the timing sequence between various modules to make the timing sequence of the whole system more reasonable.

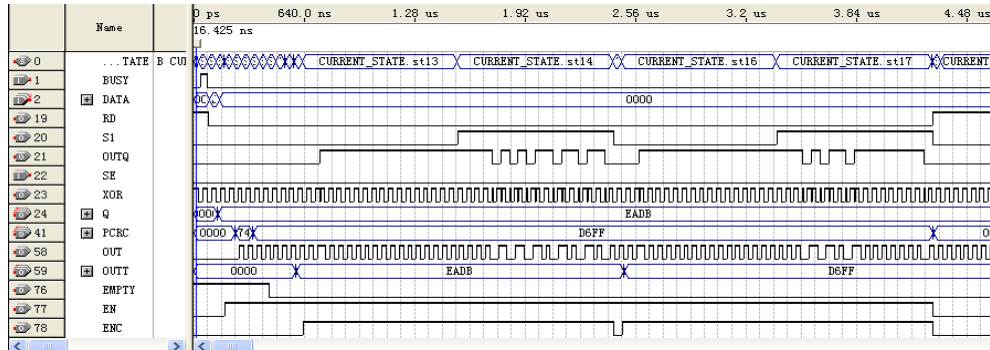


Figure 8. MCU Simulation Results Diagram

The simulation results are shown in Fig.8, which is one sampling period of circuit in the high side. It can be seen from the simulation diagram that the MCU module completes the control of A/D converter as the data acquisition and of the generation of check code in CRC circuit. The data stored in the memory after combination are sent into Manchester coding module, finally displayed as the output results.

3. Conclusion

In this paper, the application of FPGA technology is that the control of A/D converter in high voltage side, CRC check code and the design of Manchester coding circuit. The main functions achieved in the system include signal acquisition of A/D converter, CRC check on acquisition of digital signal, data storage and the sort of data according to the format, data input in Manchester code circuit and transmission to the low voltage side through the optical fiber. The Field Programmable Gate Array (FPGA) is used as a sequential controller in high voltage side, as well as the realization of encoding and decoding part. The integration of multiple functions into further a silicon chip increases efficiency. The simulation results can prove that the design of the signal processing circuit is feasible. The requirements of the efficiency and timeliness stipulated in the standard are met.

The innovative points of this article include: FPGA technology is used to design of each module circuit, which integrates the multiple functions into a chip to make the system smaller size, higher precision, more powerful, able to quickly and flexibly realize the functions required by the system.

Acknowledgment

This work is supported by National Nature Science Foundation of China under Grant 61304069, 61372195, 61371200.

References

- [1] J. J. Zhao and L. S. Feng, "A New Type of Fiber Optical Current Sens", *Microcomputer Information*, vol. 7, no. 135, (2005).
- [2] H. Z. Zhang, W. K. Li and S. X. Zheng, "Study and Design of Digital Output Interface on Electronic Transformers According to Iec 60044-8", *High Voltage Apparatus*, vol. 41, no. 286, (2005).
- [3] Y. N. Ning, Z. P. Wang and A. W. Palmer, "Recent Progress in Optical Current Sensing Techniques", *Rev. Sci. Instr.*, vol. 66, no. 3097, (1995).
- [4] J. H. Peng, "A Simple Algorithm of Parallel Crc Check for Ten Gigabits Ethernet Interface", *Microcomputer Information*, vol. 7, no. 213, (2006).
- [5] "The Principle and Implementation of a Parallel CRC Computing", *Acta Electronica Sinica*, vol. 4, no. 143, (1999).
- [6] R. Rob, L. Mark and H. Jim, "Pushing the State of the Art with Multichannel A/D Converters", *Analog Dialogue*, (2005).
- [7] L. Mark, "Advanced Digital Post-Processing Techniques Enhance Time Interleaved A/D Performance", *Analog Dialogue*, (2003).
- [8] E. P. Suomalainen and K. J. Hallstrom, "Onsite Calibration of a Current Transformer Using a Rogowski Coil", *IEEE Trans. Instrum. Meas.*, vol. 58, (2009), pp. 1054.
- [10] F. Pan, R. Chen, Y. Xiao and W. Sun, "Electronic Voltage and Current Transformers Testing Device", *Sensors*, vol. 12, no. 1042, (2012).
- [11] V. B. Djokic, D. J. Ramboz and E. D. Destefan, "To What Extent Can the Current Amplitude Linearity of Rogowski Coils be Verified", *IEEE Trans. Instrum. Meas.*, vol. 60, no. 2409, (2011).
- [12] K. Sasaki, M. Takahashi, Y. Hirata, T. Murao, H. Takeda, Y. Nakamura, T. Ohtsuka, T. Sakai, and N. Nosaka, "Development of DC Optical Current Transformer for Cable Protective Relay in Hokkaido-Honshu HVDC Link", *International Conference on Electrical Engineering*, (2009); Shinyo.
- [13] "Design of Temperature Acquisition System for Three-Phase Transformer", *Proceedings of 3rd IEEE International Conference on Computer Science and Information Technology*, (2010).
- [14] Z. P. Wang, C. Kang, Z. J. Huang and X. Y. Zhang, "Faraday Mirror-Typed Optical Current Transformers and Its Theoretical Analysis", *Optics & Laser Technology*, vol. 39, no. 368, (2007).
- [15] E. F. Donalson, J. R. Gibson, G. R. Jones, N. A. Pilling and B. T. Taylor, "Hybrid Optical Current Transformer with Optical and Power-Line Energisation", *IEEE Proceedings Generation, Transmission and Distribution*, (2006).
- [16] J. Shao, N. Ye and X. Y. Zhang, "The Implementation of High-speed Floating-Point DBF Based on FPGA", *Jdcta: International Journal of Digital Content Technology and its Applications*, vol. 5, no. 142, (2011).
- [17] Q. F. Shang, Y. C. Qi, Z. Y. Xie, B. Chen and Y. H. Yang, "Hybrid Optical Fiber Current Transformer based on DSP and Ultra-Low-Power Consumption Micro-Controller", *Proceeding of IEEE International Conference on Power System Technology Proceedings*, Kunming, vol. 1137, (2002).
- [18] "Emerging Technologies Working Group, Power Systems Instrumentation and Measurements Committee, the Fiber Optical Sensors Working Group", *Optical Current Transducers for Power Systems: A Review*, *IEEE Trans. Power Delivery*, vol. 9, no. 1778, (2004).

Authors



Ying Zhang, she received her M.E degree from Northeastern University, China, in 1998 and now is a professor in Electrical Engineering department of Shenyang Institute of Engineering. Her research direction is power system automation technology.



Shenghui Wang, he received his PH.D degree from Shenyang University of Technology, China, in 1999, and now is a professor in Electrical Engineering department of Shenyang Institute of Engineering. His research interests include Application of PV Systems, and also electrical engineering control and automation.



Xuejie Wang, she received her M.E degree from Northeast Dianli University in 2010, and now is a Engineer in Electrical Engineering department of Shenyang Institute of Engineering and a PH.D candidates in Harbin Institute of Technology. Her research interests include intelligent electrical apparatus and its automation.



Lei Qi, he received his M.E degree from Northeast Dianli University in 2010, and now is a Engineer in Liaoning Provincial Institute of safety science china and a PH.D candidates in Shenyang University of Technology. His research interests include intelligent electrical apparatus and its automation.

