Performance Enhancement of Wireless Datalink Modem using Channel Coding

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Abstract

In this paper the model having D8PSK modulation applied by channel coding of Convolution Turbo Code (CTC) was designed and analyzed to improve the performances of wireless communication system for data link between ground equipment and aircraft. The suggested modem was differential 8PSK modulation system and channel coding of Convolution Turbo Code (CTC) system, and TDMA system was used for transmission. The hardware was embodied for the test and done by using 2 FPGA's and DSP. The function of FPGA has the one of modulation and demodulation of signal, acquisition and maintaining of TDMA synchronization and generating timing signal. As the test results, it was recognized that the transmission rate can be maintained though the code rate is increased based on 28.8 Kbps and the performance of SNR gets 15dB when BER performance criteria is 10^{-6}. And, it was recognized that the performance of BLER satisfies 10^{-4} based on BER 10^{-6}. And, it was also recognized that the performance of SNB was improved by 4dB comparing with the case which channel coding was not used from the test results.

Keywords: *CTC, D8PSK, Convolution Turbo Code*

1. Introduction

Generally, 8PSK is used for broadband video system monitoring as well as for modulation system of aircraft wireless data transceiving or the data link equipment between military ground equipment and aircraft. And while QPSK modulation method used in DVB-S that is the existing satellite communication system, 8PSK modulation is used in DVB-S2 to enhance transmission rate. In this paper, 8PSK modulation was designed to improve the performance of modem for wireless data communication between ground and aircraft as modulation method and the data link modem applied by CTC was designed as the channel coding method.

The conventional communication system processed the coding and modulation independently each other, but the method that processes the coding and modulation in the integrated way in tended to be selected to design the high speed data transmission and highly-reliable communication system in the recent digital communication system. Regarding designing the digital communication system, the channel coding method is used to correct the error in the channel in case of designing the coding and modem of modulation system.

The channel code can be divided into block and convolution codes in large. Block code has been developed based on error correction theory and there are BCH and RS codes as the representative code. Regarding convolution code, there are the standardized convolution code and turbo code transformed by parallel connection with that. Regarding turbo code, there is one which transforms block code and another which transforms convolution code. To distinguish them, turbo code using convolution code is called CTC (Convolutional Turbo

Code) and turbo code using block code is called BTC (Block Turbo Code). Turbo code has the performance of error correction which is close to the limit of Shannon using the relatively easy code and large interleave. That is, Eb/No of about 0.7dB is required in AWGN channel to obtain the bit rate of 10^{-6} using 1/2 turbo code. It is used as the representative method of chain code by such an excellent performance. Convolution code and convolution Turbo code have the characteristics of outstanding error correction in wireless communication environment. In case of low speed data like voice level area, convolution code is used and in case of high speed data like data and image areas, convolution turbo code is used. And, its performance of error correction is more excellent than convolution code as the code which is made to minimize the bit error.

In this paper, 8PSK modem using channel coding of Convolution Turbo Code (CTC) was designed and analyzed for wireless communication system between ground and aircraft. The suggested modem used the modulation method of Differential 8PSK and channel coding system of Convolution Turbo Code (CTC). The hardware of D8PSK modem was embodied for the test. The hardware was embodied using 2 FPGA's and DSP and the function of FPGA has the one of modulation and demodulation of signal, acquisition and maintaining of TDMA synchronization and generating timing signal and DSP has the functions of control and decoding[1][2].

2. 8PSK Modem using Channel Coding

Modem system designed in this paper is for the communication system between ground and aircraft and the applied modulation method is 8-PSK. The modulation of 8-PSK has the high frequency efficiency because it transmits 3 times of information amount than BPSK in the condition of same bandwidth, but it can be interfered by noise easily because the distance between the phases gets closer. So, power for transceiving was consumed more to have the same error transmission rate. And, the performance should be improved by adding channel coding to correct such error rate.

2.1 Design of the Suggested Modem

The performances of modulation and demodulation of signal are processed for data communication between ground and aircraft. Figure 1 shows the entire system structure of the suggested modem. The suggested modem system has the functions of creating transmission frame, de-framing, data modulation and demodulation, channel encoder and decoder, transceiving operation control, synchronization and control of TDMA, creating and control of system timing.

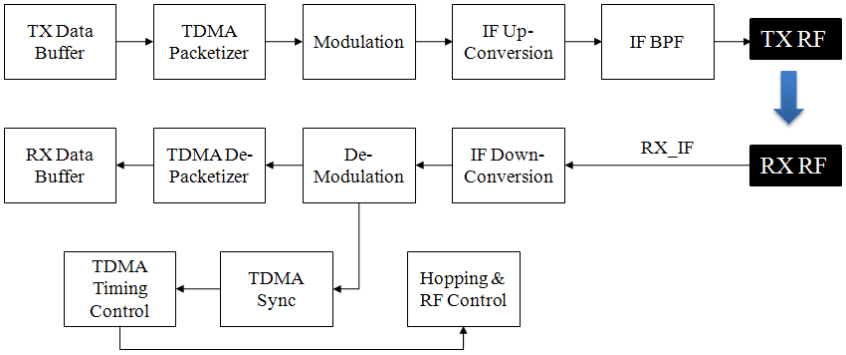

Figure 1. Development Modem System Structure

There is channel encoder and decoder module as well as packet generator in baseband signal processor module before IF down conversion of Figure 1. Channel encoder and decoder block is composed of FEC (Forward Error Correction) encoder/decoder for correcting error that can be generated in case of wireless transceiving, puncturing that controls the bit rate by controlling the output of channel encoder with the uniform regulation to reduce the complexity in case of demodulation, interleaver/deinterleaver to prevent scrambler/descrambler and burst error to disperse power density of transmitting data and differential encoder/decoder to resolve the phase ambiguity of receiving signal. Clock of 1.25 MHz and 2.5 MHz is used in channel encoder and the sync signal that notifies the starting point of FEC data is input. Channel encoder was applied by Convolution Turbo code (CTC) as the channel coding method in this paper by abstracting the meaningful information from source data and Figure 2 shows channel encoder block using CTC and its coding rate is 2/3[3][4].

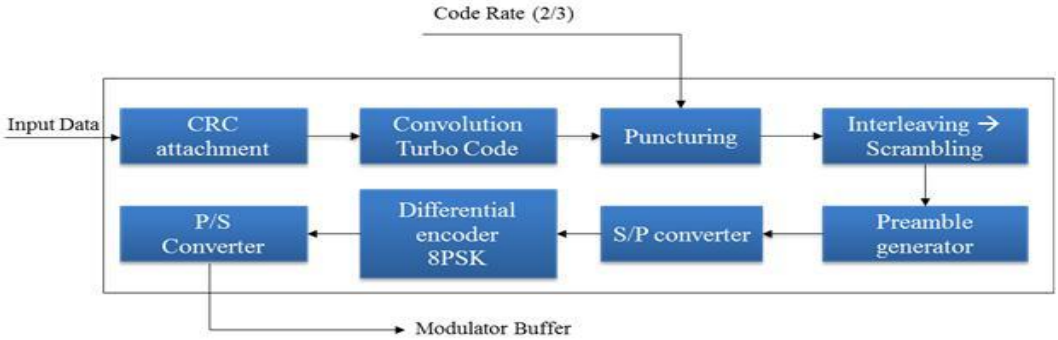

Figure 2.Channel Encoder Block Diagram (Convolution Turbo Code 2/3)

The burst error which can be broken out due to sudden change of channel in Figure 2 can cause the severe degradation during decoding process. Interleave is used to prevent that. Data input to interleave is input in the unit of row and output in the unit of column by chord inversion according to the following regulation and the original sequence is recovered by passing through the reversed process. And, scrambler/descramble are used to disperse power density and let transmitting data show random distribution. The random signal is generated by the function of scrambling though data of '0' or '1' input serially. Scrambler has the same structure as descrambler. Preamble means the data such as GCP, CTR, FSP and HSP inserted into SYNC Hop and Data Hop for demodulation of data other than data transmitted for actual transceiving, and is inserted after sorting it as frame and slot[5][6][7].

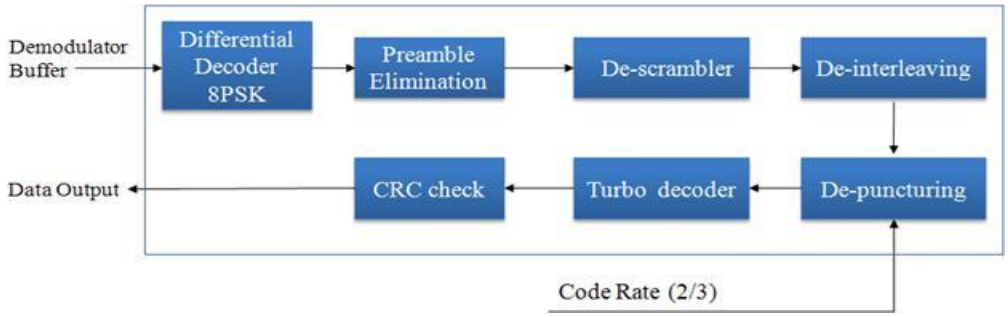

Figure 3.Channel Decoder Block Diagram (Convolution Turbo Code)

Figure 4 shows the structure of modulator of D8PSK modem. The modulator carries out the function of generating the modulated signal of D8PSK by receiving the input of bit information channel-coded and it is composed of input Buffer, mapper, interpolation & SRRC (Square Root Raised Cosine) filter, interpolation & LPF (Low Pass Filter), D8PSK modulator and NCO as shown in Figure 4. Modulation is composed by using D8PSK and makes the parallel signal of real number and imaginary number using differential encoder signal and symbol mapper and makes data of 80Ksps by implementing 4 times of interpolation of mapped signal and implements 768 times of interpolation again through SRRC filter and outputs it to DAC by making the transmitting data of 61.44Msps whose center frequency is 20.48MHz[8].

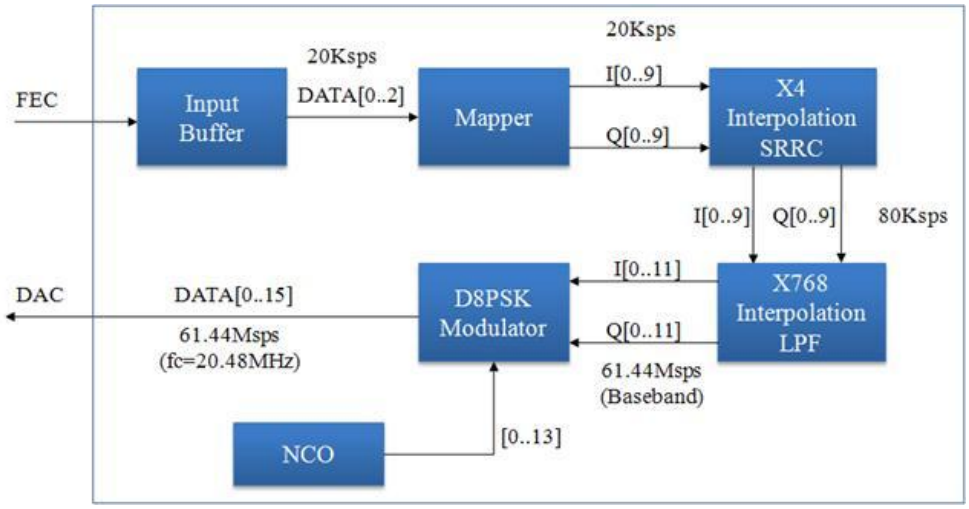

Fig 4.Modulation Block Diagram

Input buffer saves FEC output data processed by the unit of slot and forwards the data to mapper in each hop dividing it in the unit of hop. Mapper implements 8PSK mapping onto the data read from input buffer and generates the values of I and Q. In case of 8PSK, a pair of I and Q values are generated against the input data of 3 bit and the values of I and Q are described in 10 bit. In case of mapping 8PSK, the values of I and Q output through mapper are shown as Table 1.

Table 1. 8PSK Mapping

Transmission data	I Value	Q Value
000	01 1101 1001	00 1100 0100
001	00 1100 0100	01 1101 1001
011	11 0011 1100	01 1101 1001
010	10 0010 0111	00 1100 0100
110	10 0010 0111	11 0011 1100
111	11 0011 1100	10 0010 0111
101	00 1100 0100	10 0010 0111
100	01 1101 1001	11 0011 1100

Interpolation and SRRC filter carry out the function of preventing the interference between surrounding channels through SRRC filtering after 4 times of over-sampling of I and Q values mapping-implemented in mapper. SRRC filter of sending part carries out the function of making total transferring function get raised cosine together with SRRC filter of receiving part. Now that it should be converted to sample rate which is higher than the frequency to be up- converted by NY Quist rate to implementing up-conversion of frequency in baseband, it carries out interpolation of 61.44MHz which is 768 times of 80 kHz and passes through LPF to remove the image after carrying out each interpolation. The center frequency to be up-converted is 20.48MHz.

NCO (Numerical controlled Oscillator) was used to generate local signal required for up-conversion of frequency. NCO is composed of 4096 samples with 14bit and leaps to generate the sine wave and cosine wave of 20.48MHz along sample clock of 61.44MHz. It is forwarded to DAC to convert it to analog signal after up-conversion of frequency to 20.48MHz by mixing interpolated data to 61.44MHz with the signal of NCO.

Demodulator implements down conversion of frequency of digital IF signal of center frequency 20.48MHz received from ADC operating in clock of 61.44MHz and converts it to baseband and abstracts transmission symbol by correcting timing, frequency and phase error of baseband, and forwards the abstracted symbol to channel demodulator.

2.2 Performance Simulation of the Suggested Modem

Figure 5 is the performance simulation results of D8PSK CC 3/4 and CTC 2/3 of suggested modem. Based on 10-6, CC 3/4 has the performance of about 18dB in AWGN and CTC 2/3 does that of about 11.5dB. In simulation, applying CTC 2/3 shows the performance improvement by about 6.5dB than applying the existing CC 3/4 based on 10^{-6}. The simulation was carried out according to the structure of suggested model and simulation parameter is shown as Table 2, and channel environment was simulated in AWGN environment. Coding rate 3/4 was applied to convolution code and coding rate 2/3 was applied to convolution turbo code in the simulation.

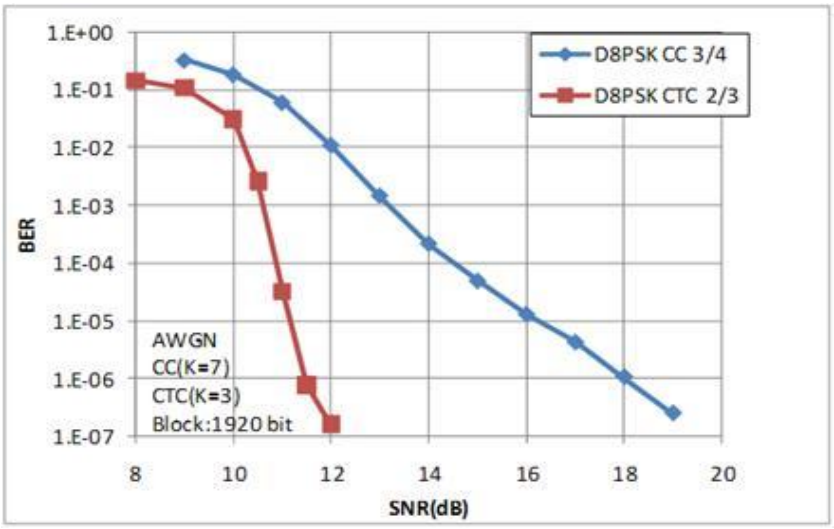

Figure 5. 8PSK BER simulation along channel coding

3. Experimental Results

Figure 6 shows the hardware configuration of D8PSK embodied for the test. Hardware is composed of 2 FPGA's and has the functions of modulation/demodulation of signal, acquisition and maintaining of TDMA synchronization and timing signal generation. FPGA #0 carries out the function of timing control and modulation of modem by receiving local clock and synchronized division clock from clock generator and transceives data with DSP. FPGA #1 carries out the function of demodulation of modem and has the function of RF control[9].

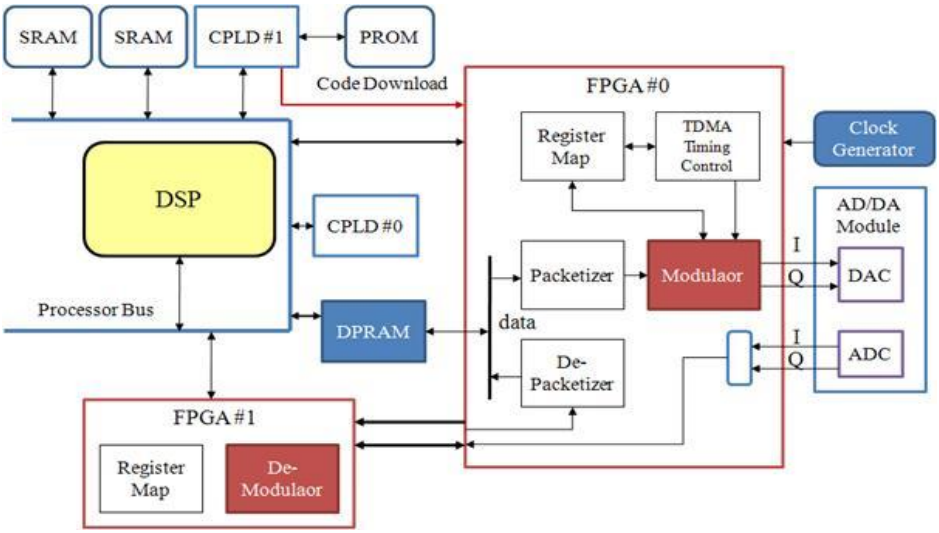

Figure 6. Modem H/W Block

Table 2 shows the system design specification of development system. If frequency is 21.4 MHz TDMA system was used for transmission and channel spacing was 25KHz and signal bandwidth was ±10.8kHz.

Table 2. System Design Specification of Development System

Item	Value of specifications
Channel bandwidth	25KHz
Signal Bandwidth	±10.8kHz
Transmission method	High speed leap (over 300 Hop/sec)
Modulation	Digital Modulation (8PSK)
Data transmission rate	Over 28.8KBps
Multiple access method	TDMA
Data receiving sensitivity	-100dBm@10E^{-6} BER, 28.8KBps
Input Frequency, Level	21.4MHz, -15dBm ± 1dB
Output Frequency, Level	21.4MHz, -15dBm ± 1dB

Receiving SNR was measured at the range of 13dB ~ 16dB that generates BER. Table 3 shows the data measured SNR against the suggested model in test environment so data can be received to receiving module after adding noise to the original signal by combining noise generator with transmitting data between transmission module and receiving module. BER

measurement was tested using the signal analyzer with BER and BLER in cases of uncode and applying channel code(CTC 2/3).

Table 3. Results for each SNR (Uncoded, CTC 2/3)

Modem Input (Signal)	SNR	Modem Input (Noise)	Num of uncoded symbols	uncoded BER	Coded BER	Bler	Test Time (Second)
-18.5	13	-31.5	29884800	0.099205349	0.051935849	0.565106007	11.79
-18.5	13.5	-32	10662960	0.0920493	0.010838672	0.151522654	4.20
-18.5	14	-32.5	16346880	0.08442192	0.001076013	0.011789406	6.45
-18.5	14.5	-33	17682720	0.078697508	3.35E-05	0.001343685	6.97
-18.5	15	-33.5	19501680	0.074093155	8.19E-06	0.000541492	7.69
-18.5	15.5	-34	22804320	0.071166472	1.39E-06	0.000115768	8.99
-18.5	16	-34.5	86174880	0.068560873	5.4706E-07	3.06354E-05	34.00

SNR was tested from 13dB to 16dB. Now that the value of -18.5dB is given as the input signal of modem and it reduces the input noise of modem from -31.5dB to -34.5 dB by the unit of 0.5dB, receiving BER was measured along the change of SNR after changing SNR adjusting the input level in receiving unit.

As the test results, when the number of uncoded symbol was 19,501,680, SNR should have been over 19dB if BER wants to have 10^{-6} in case which such symbol was transmitted with uncoded, and error was not broken out when SNR was over 17dB in case of applying Convolution Turbo Code and BER was broken out when it got lower than 16dB, and SNR satisfying 10^{-6} was 15dB. And it was recognized that BLER (Block Error Rate) was 10^{-4} in case which BER was 10^{-6}. Testing time was about 7 minutes.

4. Conclusion

In this paper, 8PSK modem using channel coding of Convolution Turbo Code (CTC) was designed and analyzed for wireless communication system between ground and aircraft. The suggested modem used differential 8PSK method and Convolution Turbo Code (CTC) channel coding method.

In order to analyze the performance of the suggested modem, the performances of D8PSK CC 3/4 and CTC 2/3 were simulated. CC 3/4 has about 18dB in AWGN and CTC 2/3 has about 11.5dB in AWGN based on 10-6 in the simulation. Applying CTC 2/3 shows the functional improvement by about 6.5dB than the existing CC 3/4 based on BER 10-6 in the simulation.

In order to analyze the performances of the suggested modem experimentally, hardware of D8PSK modem was embodied. Hardware was embodied using 2 FPGA's and DSP. FPGA has the functions of modulation/demodulation of signal, obtaining and maintaining of TDMA synchronization and timing signal generation.

As the test results, it was recognized that the transmission rate could be sustained though code rate was increased based on 28.8Kbps and that SNR performance got 15dB when BER performance criteria was 10-6. And, it was also recognized that the performance of BLER satisfied 10-4 based on BER of 10-6 rate.

In cases of embodying the simulation results and hardware actually, the implementation loss is broken out due to heating of the components. It was recognized that the performance was improved by about 4dB considering such implementation loss. Now that the structure should have been changed for the optimization of block size in case of applying CTC 2/3 and the length of data hope was increased by double and the number of data hop for each slot was decreased, the problem that hopping rate of frequency was decreased appeared. Further study should be carried on for improvement of that.

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