A New Programmable RF System for System-on-Chip Applications

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Abstract

This paper presents a new programmable radio frequency (RF) system for a System-on-Chip (SoC) transceiver. A 5-GHz low noise amplifier (LNA) is integrated with an on-chip programmable RF circuits using 0.18㎛ SiGe technology. Proposed system is very useful for concurrent RF ICs in a complete RF system environment. The programmable circuit helps it to provide DC output voltages, hence, making the RF system chain automatic. The programmable RF system automatically adjusts performance of an LNA with the processor in the SoC when it goes out of the normal range of operation. It also compensates abnormal operation due to the unusual PVT (Process, Voltage and Thermal) variations in RF circuits.

Keywords: *System-on-Chip, SoC, programmable RF system, low noise amplifier.*

1. Introduction

A rapid growth in RF integrated circuit devices demands high density, high speed and low-cost RF systems. To realize these recent trends, system-on-chip (SoC) has become a new solution in today's RFIC industry. However, the suitable test technique and reduction of test cost for SoC still remain to be the major bottleneck to make affordable wireless systems. To solve these problems, the test technique using DFT (Design-for-Testability) circuit in the RF and mixed-signal domain is applied as a suitable test structure on SoC [1-5].

To design an effective RF DFT structure, proper identifications of catastrophic faults and parametric variations in RF system play an integral part of the design. Analog systems have only a few inputs and outputs, and their internal states exhibit low time constants compared to digital circuits [6]. To test point-to-point transceiver, loop-back technique using spectral signature analysis is generally used with lower effort and very small test overhead [4-5]. However, this test technique has disadvantages such as lower test coverage due to the fact that the complete transceiver is tested as a whole and the need of an additional DSP due to the higher complexity of the test signature generation [5].

In this paper, a new low-cost alternative system for RF SoC testing to adjust PVT (Process, Voltage and Thermal) variations in RF circuits is proposed. The alternative method utilizes automatic programmable RF system for 5-GHz low noise amplifier (LNA) as a typical RF front-end chip. The system involves RF DFT circuit, Capacitor

Mirror Bank (CMB) and digital signal processor (DSP). The RF DFT circuit helps it to provide DC output voltages, hence, making the compensation system automatic.

2. Approach

Fig. 1 shows the SoC-based receiver configuration with an automatic programmable RF system for the LNA. The proposed system contains RF DFT circuit, CMB and DSP. The system automatically adjusts and compensates performance of the 5-GHz LNA (typical RF chip) by the processor when the LNA goes out of the normal range of operation due to the unusual PVT (Process, Voltage and Thermal) variations in RF circuits. The RF DFT circuit helps it to provide DC output voltages, thus, making the system automatic.

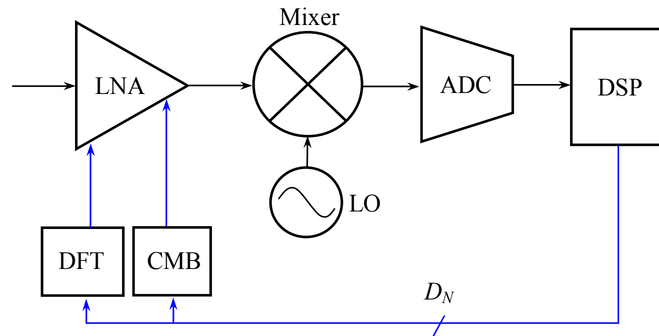


Figure. 1. SoC-based receiver configuration with an DFT and CMB for the LNA.

The RF DFT hardware consists of a test amplifier (TA), a band-gap reference and two RF peak detectors (PD1 and PD2) as shown in Fig. 2. This additional hardware occupies a very small area on the SoC, and it helps to measure LNA performance without expensive external equipment. Two RF peak detectors are used to provide DC output voltages (V_{T1} and V_{T2}) for easy measurement.

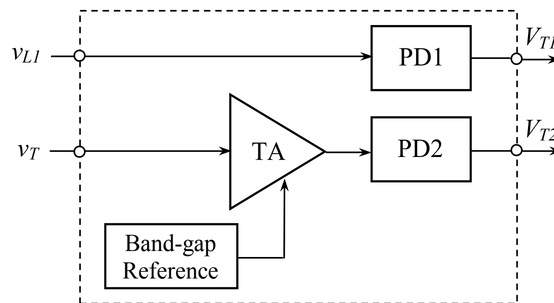


Figure. 2. RF DFT hardware.

The proposed DFT circuit is shown in Fig. 3, and it is designed using 0.18µm SiGe technology. It consists of TA and PD2 circuit stages. The PD1 circuit is also a part of the DFT circuit and it has the same topology as the PD2 circuit as shown in Fig. 3. The test amplifier is designed with the input and output impedances of 50 ohms, respectively. The gain of the test amplifier is designed to be 3 to increase the output voltage level. The RF peak-detectors are

used to convert RF signal to DC voltage. The bias stage utilizes a band-gap reference circuit for the low supply voltage and the low power dissipation.

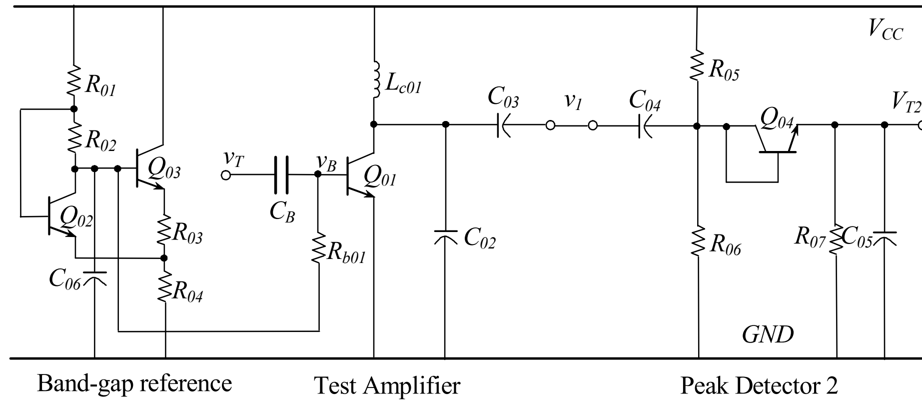


Figure. 3. Schematic diagram of an RF DFT.

Fig. 4 shows details of the proposed CMB. It has N-bit capacitor banks to accurately compensate an LNA performance. In this approach, we have designed an 8-bit CMB considering a chip area overhead. The capacitor bank is controlled by using digital signals ($D_8 \ldots D_2 D_1$) from the digital signal processor (DSP) hardware. The input data streams of ($D_8 \ldots D_2 D_1$) = (0…01) for (1/8)(C_b) and (1…11) for C_b have been used to compensate LNA performance, respectively. The C_b is under fault-free value. It was designed with LNA on a single chip using 0.18μm SiGe technology to demonstrate this idea. It is powered by 1.8V supply voltage.

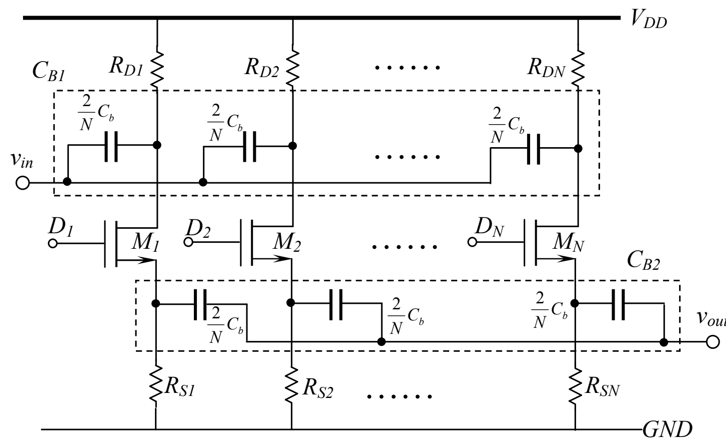
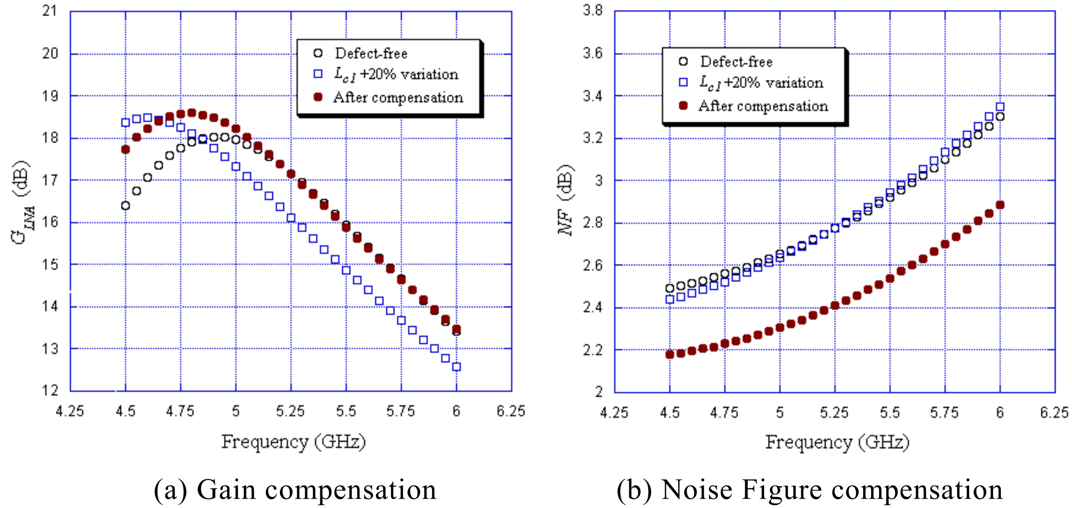


Figure. 4. N-bit CMB.

3. Results

Figs. 5(a) and (b) show the gain and noise figure variations and their compensation results for a +20% process variation of the most sensitive component (L_{c1}). The gain and noise figure compensations shown in this figures were done at the operation

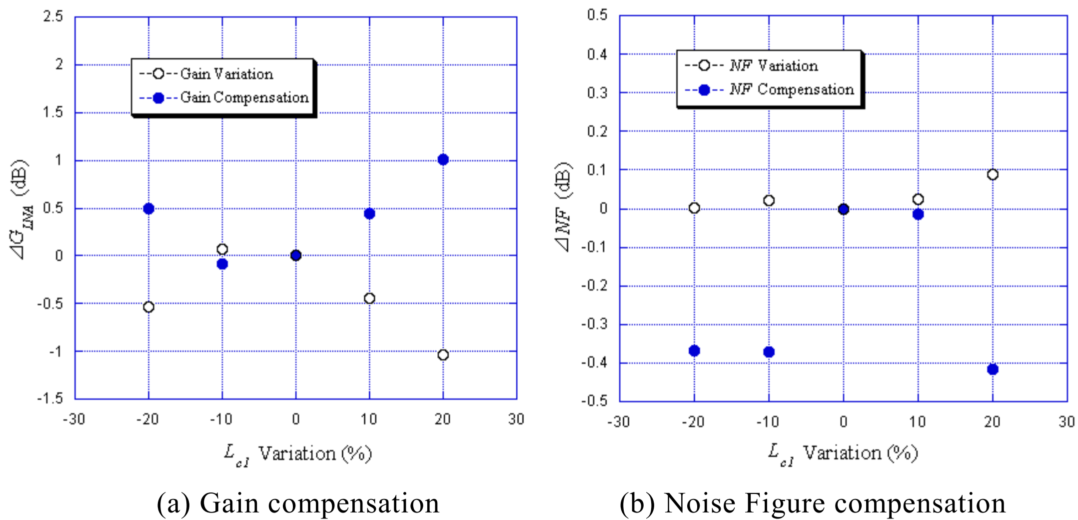
frequency of 5.25GHz. We identified a variation of 1.04dB (11.32%) in the LNA gain from the +20% process variation. To compensate a 1-dB LNA gain, the input data stream of (D_8…D_2D_1) = (0…01) providing C_B = (1/8)(C_b) was applied. The C_b is under fault-free value. As can be seen from Fig. 10, our ACN can compensate the gain of LNA due to the process variation at 5.25 GHz. The noise figure compensation shown in this figure was done at the operation frequency of 5.25GHz. The L_{c1}+20% process variation showed a small variation in the LNA noise figure as shown in Fig. 5(b). We identified a variation of 0.022dB (0.5%) in the LNA noise figure from the +20% process variation.



(a) Gain compensation (b) Noise Figure compensation

Figure. 5. LNA compensation results for L_{c1}+20% process variation.

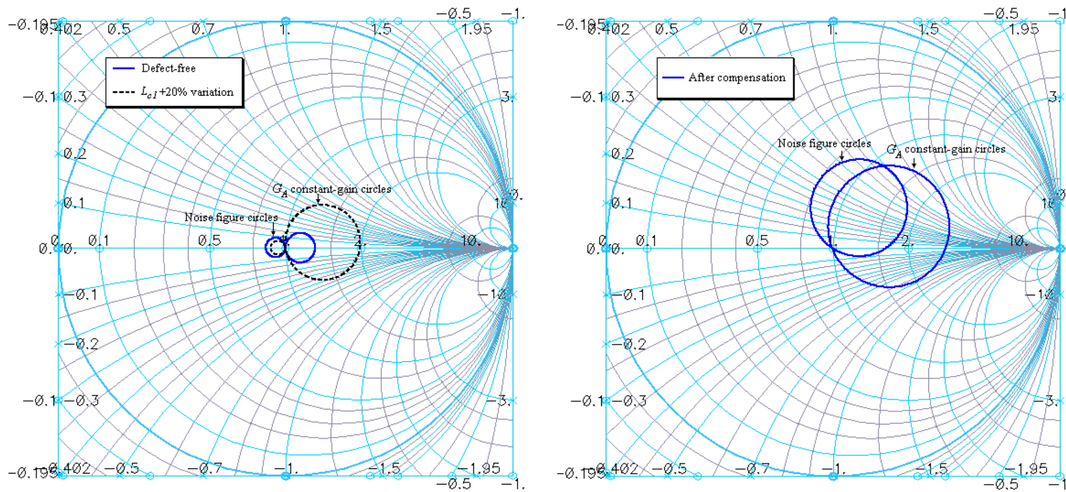
Figs. 6(a) and (b) show the LNA gain and noise figure variations and their compensations for L_{c1} process variation, respectively. We considered process variations of L_{c1}-20% to +20%. As shown in these figures, our compensation network showed good compensation results for the variations of the LNA gains and noise figures.



(a) Gain compensation (b) Noise Figure compensation

Figure. 6. LNA compensation results for L_{c1} process variation.

Fig. 7(a) shows constant noise figure circles and constant available power gain (G_A) circles for defect-free and L_{c1}+20% process variation at 5.25GHz. These circles are drawn in the Γ_s plane. For the process variation, the Smith chart in the Γ_s plane is useful to investigate variations of both gain and noise figure. Maximum gain and minimum noise figure cannot, in general, be obtained simultaneously [1-2]. As shown in Fig. 7(a), the noise figure circle is decreased and the G_A circle is increased due to the process variation. Fig. 7(b) shows constant noise figure circle and constant available power gain (G_A) circle after compensation for L_{c1}+20% process variation at 5.25GHz. These circles are also drawn in the Γ_s plane. After compensation, the noise figure circle moved to clockwise. The phase of Γ_{opt} is approximately 57°. The available power gain circle moved to counterclockwise.



(a) L_{c1}+20% process variation

(b) Compensation

Figure. 7. G_A and noise figure compensations for parametric variations (Smith Chart).

Table 1 summarizes the noise figure and gain variations and their compensation results for process, thermal and coupled variations. Data codes used for compensation are listed. As can be seen in this table, the proposed programmable RF system showed good compensation results for the variations of the LNA gains and noise figures.

Table 1. Comparisons of variations and their compensations.

Variations			Compensations			
Components	ΔG_{LNA}(dB)	ΔNF(dB)	Data Codes	C_B	ΔG_{LNA}(dB)	ΔNF(dB)

L_{c1}+10%	-0.450	0.003	(00000011)	$0.250C_b$	0.440	-0.367
L_{c1}+20%	-1.040	0.022	(00000001)	$0.125C_b$	1.010	-0.370
T+10°C	-0.103	0.108	(00111111)	$0.750C_b$	0.146	-0.141
T+20°C	-0.188	0.191	(00001111)	$0.500C_b$	0.283	-0.275
T+30°C	-0.277	0.274	(00000011)	$0.250C_b$	0.403	-0.393
L_{c1}+10%&T+10°C	-0.560	0.113	(00001111)	$0.500C_b$	0.305	-0.272
L_{c1}+10%&T+20°C	-0.649	0.197	(00000011)	$0.250C_b$	0.443	-0.368
L_{c1}+10%&T+30°C	-0.744	0.281	(00000011)	$0.250C_b$	0.445	-0.396

4. Conclusions

This paper proposed a novel programmable RF system for a System-on-Chip (SoC). We proved that our programmable RF system can help to compensate RF circuits with PVT (Process, Voltage and Thermal) variations. Utilizing proposed system, we measured input impedance, gain and noise figure, and it automatically adjusted performance of a low noise amplifier (LNA) when it went out of the normal range of operation. The new system provided successful measurement results of RF chips. We believe that this new capability will provide industry with a low-cost technique to test RF SoC.

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