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Novel Binary to Gray Code Converters in QCA with Power Dissipation Analysis

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Abstract

Quantum dot cellular automata (QCA) are pledging nanotechnology which has been used widely in digital circuits and systems. Conventional lithography based VLSI model encounter acute challenges of tunneling, variation of doping and short channel issue. In a remarkably fast development of VLSI technology, it is the cardinal of the age to reach a stable model with area and low power consumption. QCA is a promising alternative to complementary metal–oxide–semiconductor (CMOS) technology with many enticing features such as high-speed, low power consumption and higher switching frequency than transistor based technology. The code converters are the basic unit for transformation of data to execute arithmetic processes. In this paper, a novel QCA based 2-bit binary-to-gray, 3-bit binary-to-gray, and 4-bit binary-to-gray code converter have been proposed. The proposed design reduces the number of cells, area, and raises switching speed. The energy dissipation by the proposed circuits are evaluated which certifies the prospect of QCA nano-circuit presenting as a substitute level for the attainment of reversible circuits. The consistency of the proposed circuits is tested under thermal randomness that reveal the functioning effectiveness of the circuits. The proposed circuits are simulated using QCADesigner and Microwindlite tool which is widely used for simulation and verification.

Keywords: *Binary to Gray Converter, Quantum Dot Cellular Automata, Gray Code, Power Dissipation*

1. Introduction

QCA is an innovative access towards the present age of nanotechnology and a substitution of contemporary CMOS technology [1] and proposes a novel designing technique which is appropriate for logic circuits. Material limits of CMOS such as severe effort of lithography, deteriorating supply voltage and technological limits like power dissipation; hinder the microelectronics momentum using regular circuit scaling [2]. QCA is an evolving nano-technological archetype which permits functioning frequencies in THz range [3] that is not feasible in existing CMOS model and it has been recognized as one of the first six enhancing technologies with feasible applications in designing computational circuit at a superior phase in future computers [30, 31]. This paper demonstrates a unique binary to gray code converters in QCA technology and assessed the energy dissipation and constancy of the proposed designs. Then the efficiency of the proposed circuits is illustrated under thermal randomness.

The paper is arranged as follows, Section 2 itemizes a concise background to QCA layout. The proposed code converters are illustrated in section 3. Simulation outcomes in QCA and CMOS is illustrated is Section 4. Section 5 exhibited the energy depletion and constancy of the proposed designs. Finally, Section 6 presents conclusion with future work.

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2. QCA Overview

Each QCA structures are made up of similar square-formed QCA cells. Every single four-dot QCA cell is made of quantum dots which are located at the vertices of a square cell [4-6]. The dots comprise two electrons that can quantum-mechanically tunnel between them. Coulombic contact among the inter-cell electrons creates two firm arrangements P= -1 and P= +1, which are allocated to encode a logic "0" and logic "1" status, correspondingly [7, 8], as shown in Figure 1. Switching is achieved by switching the tenancy of the two electrons, in QCA technology [20].

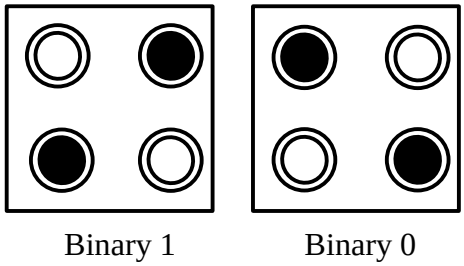


Figure 1. Formation of a Primary QCA Cell

Several QCA based combinational [1, 5, 9-22], sequential [23-27] and reversible [28-39] circuit have been proposed in current years based on inverters and three input majority gate [10, 17, 22]. The primary structures for QCA are inverter and the majority gate.

2.1. QCA Wire

The proper composition of QCA cells patterns a binary wire [31]. The 90º wire, as a line of cascaded QCA cells, which proliferates signal from one end to another, is shown in Figure 2(b). Figure 2(a) represents the 45º QCA wire, which exchanges encoded binary signal polarization in successive QCA cells [34, 40]. Along with the Coulomb repulsion, the least energy condition for two transversely adjoining cells is when they have reverse polarities.

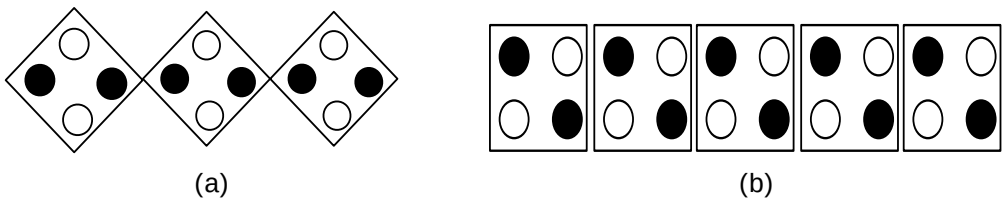


Figure 2. QCA Wire (a) 45º (b) 90º

2.2. QCA Inverter

The easiest arrangement, the inverter, is typically designed by disposing the cells with only their corners touching. The electrostatic interface is reversed, since the quantum-dots of separate polarizations are misaligned between the cells. QCA inverter returns the inverted value of the input value [34, 37].

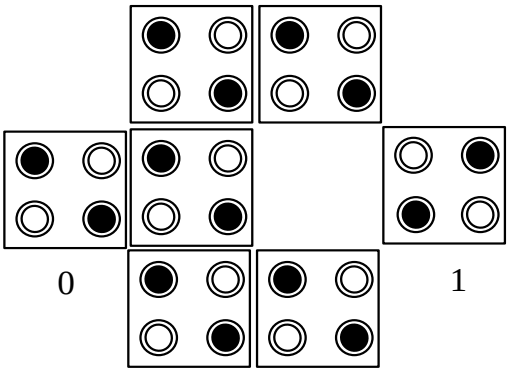


Figure 3. QCA Robust Inverter

2.3. Majority voter (MV)

Every QCA structure can be proficiently made using only majority voters and inverters. The majority voter holds four terminal cells where three are stating as input cells. If the gate inputs are A, B and C, then majority gate is stated as logic function [41]

$$MV (A, B, C) = AB + BC + CA \quad (1)$$

For creating an AND/OR function with majority voters it only requires to place the polarization of one input to a stable logic '0' or '1', individually [37, 38] shown in Figure 4(a) and (b). To generate well- structured QCA design, the digital circuits are realized with the help of majority voter-based design techniques are needed [42].

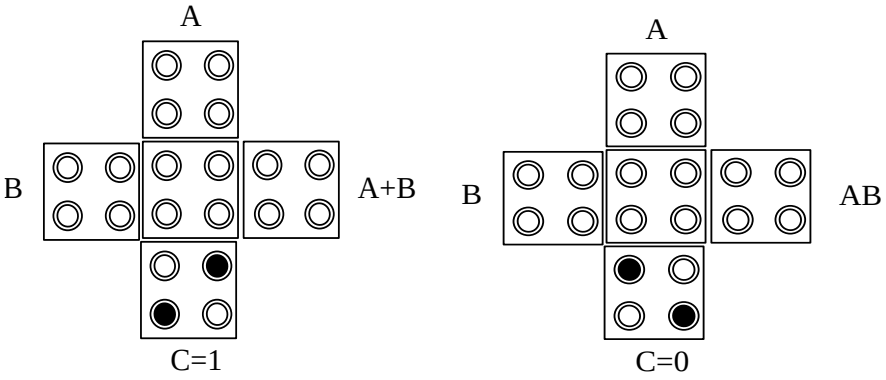


Figure 4. 2-input OR Gate and 2-input AND Gate Using Majority Voter

2.4. Clocking

In QCA, the clocking system defines via an electric domain once the cells are un polarized, latch their input values, and begin forcing other cells. It is operated both for fabricating sequential circuits and driving the circuit to remain in the quantum mechanical ground position, which rest on the inputs of the circuit, and signifies the precise computational output and effective signal proliferation. The QCA clock delivers additional energy, permitting signal gain on the nanotechnology. In the signal clocking, QCA cells are allocated to four time segments. Each segment, also named clock zone, corresponds to one of the four phases: switch, hold, release, and relax as presented in Figure 5.

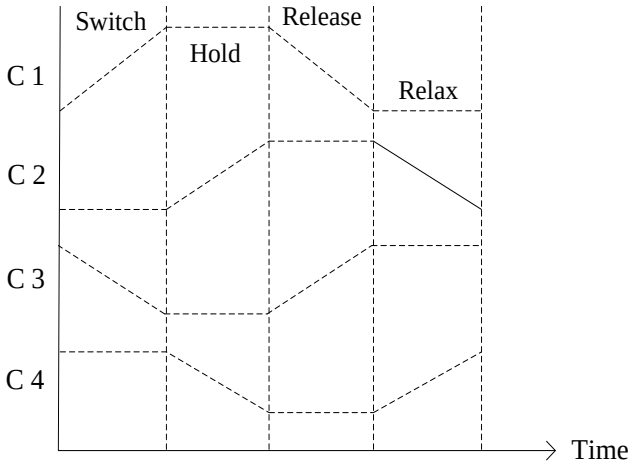


Figure 5. QCA Four Phased Clock Waveforms

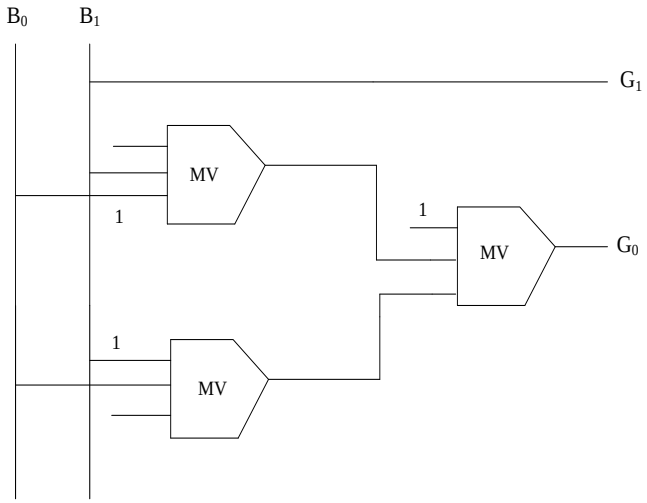
Polarization of the cell begins in the switch level and remains until the cell turn into polarized entirely [31, 38]. Once the clock reaches an elevated level (Hold stage), the cell hoards its polarization. Reduction in the cell polarization arises once the clock goes through the release level. Lastly, at the relax level of the clock, the cell turn into unpolarized. Number The zones number in the critical channel of a QCA circuit regulates its complete delay [43].

3. Proposed Design and Presentation

The computation in QCA continues by direction of cells based on polarization of neighboring cells. Estimation is performed to understand the suitable tools and confirm the proposed design. Then QCADesigner 2.0.3 is chosen and this simulation tool is explained [43]. The functionality of the design is confirmed by QCADesigner 2.0.3 which contains default values as the size of the cell, samples number, radius effect, total relaxation time, relative permittivity etc. For realization the code converter in CMOS, MICROWIND [44] is applied which is an integrated engine for circuit simulation.

Code converters are circuits which transform a given code into another that is encoded in logic arrays and operated in several areas as strengthen data flexibility and maintaining information from third parties. Binary code is a typical arrangement of data and accomplishes text information using the number system e.g. binary sequence of seven bits 1100100 is equivalent to decimal number 100. Gray code is a numeral arrangement where every value varies only a unique bit from the preceding bit. The gray code has various beneficial uses as analog-to-digital converter, simplify fault correction, and peripheral devices.

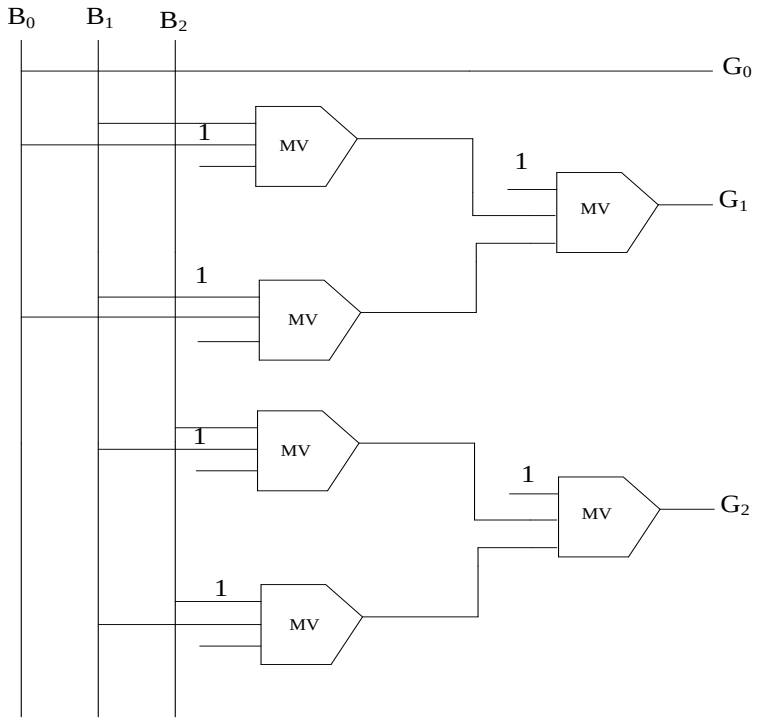
Two binary inputs B_1 and B_0 are applied for a two bit binary-to-gray code converter and their corresponding outputs are G_1 and G_0. In the same way, the inputs of three bit code converters are B_0, B_1, and B_2, the outputs are G_0, G_1, and G_2. In four bit binary-to-gray code converters the inputs are B_3, B_2, B_1, and B_0 where the consistent outputs are G_3, G_2, G_1, and G_0. Figure 6 displays the QCA block diagram of 2-bit, 3-bit, and 4-bit binary-to-gray code converter using majority gate.



(a)

Table 1. Truth Table Illustrations of Proposed Two bit Binary to Gray Code Converter

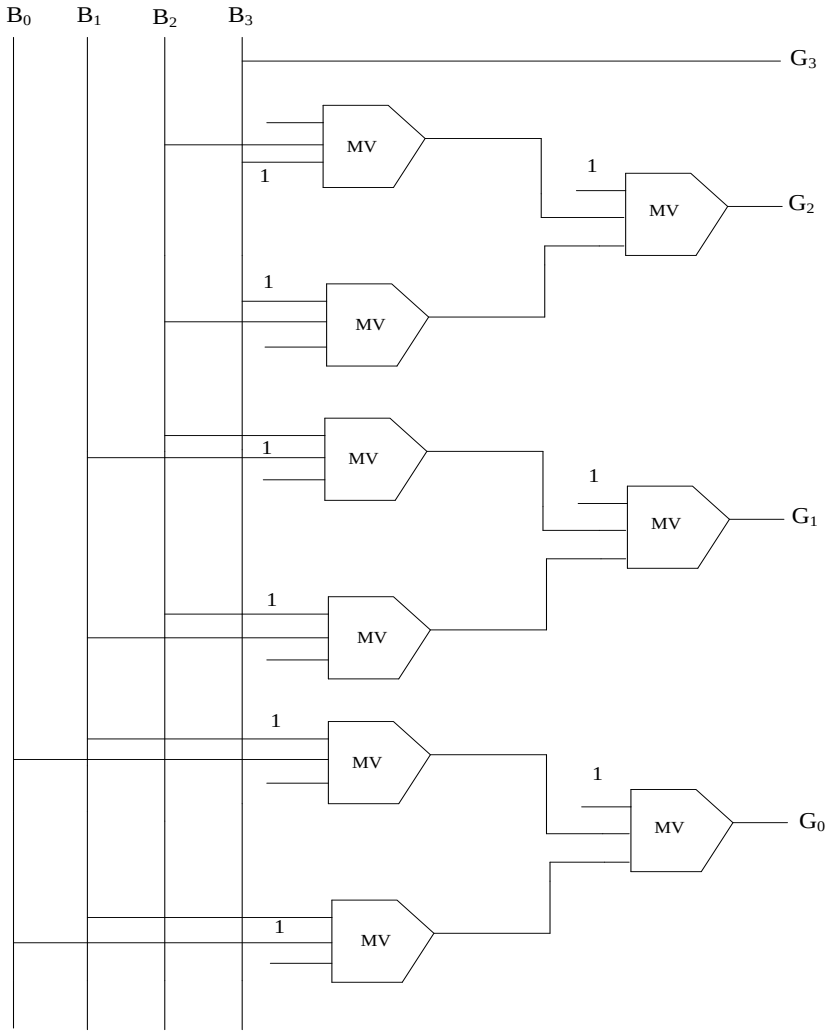
Input		Output	
B_1	B_0	G_1	G_0
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0



(b)

Table 2. Truth Table Illustrations of Proposed Three bit Binary to Gray Code Converter

Input			Output		
B_0	B_1	B_2	G_0	G_1	G_2
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	1
0	1	1	0	1	0
1	0	0	1	1	0
1	0	1	1	1	1
1	1	0	1	0	1
1	1	1	1	0	0



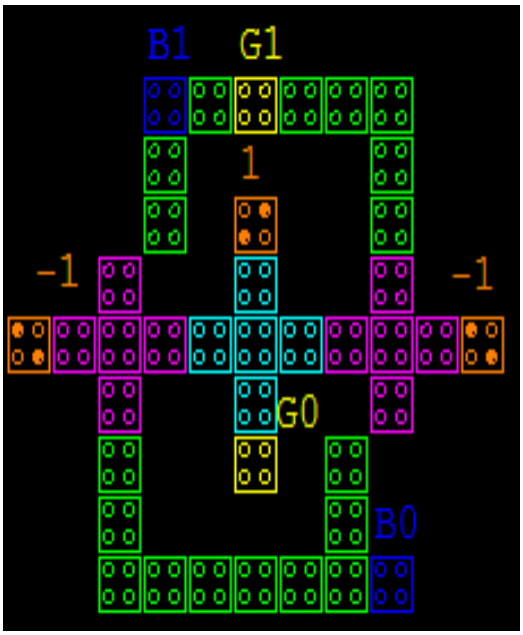
(c)

Figure 6. Block Diagram of (a) 2-bit (b) 3-bit, and (c) 4-bit Binary-to-Gray Code Converter

Table 3. Truth Table Illustrations of Proposed Four bit Binary to Gray Code Converter

Input				Output			
B_3	B_2	B_1	B_0	G_3	G_2	G_1	G_0
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	1
0	0	1	1	0	0	1	0
0	1	0	0	0	1	1	0
0	1	0	1	0	1	1	1
0	1	1	0	0	1	0	1
0	1	1	1	0	1	0	0
1	0	0	0	1	1	0	0
1	0	0	1	1	1	0	1
1	0	1	0	1	1	1	1
1	0	1	1	1	1	1	0
1	1	0	0	1	0	1	0
1	1	0	1	1	0	1	1
1	1	1	0	1	0	0	1
1	1	1	1	1	0	0	0

In the logical expression of 2-bit binary to gray code converter, input B_1 is identical to output G_1 and output G_0 is XOR-ed value of inputs B_1 and B_0.



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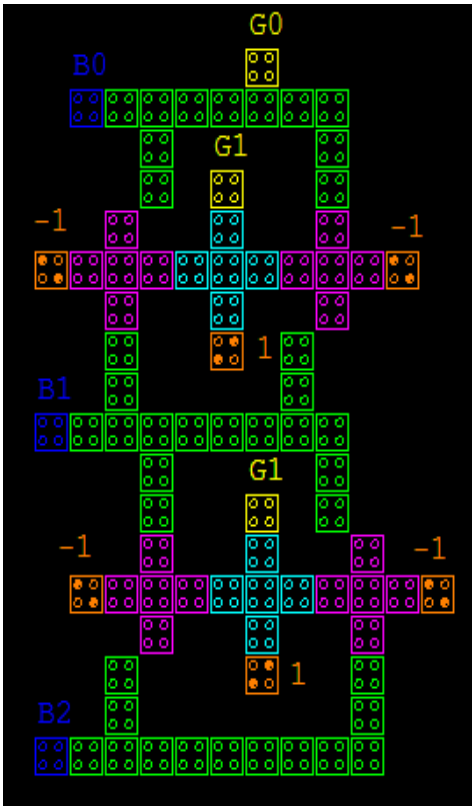

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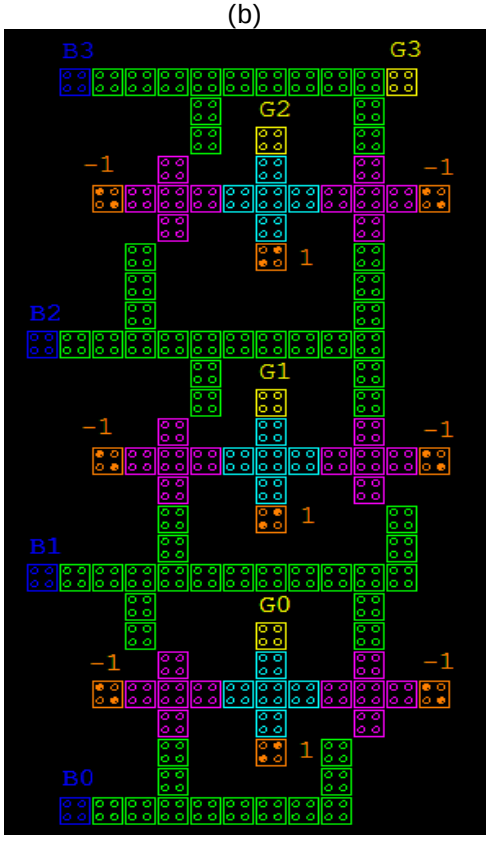


(c)

Figure 7. QCA Layout of (a) 2-bit (b) 3-bit, and (c) 4-bit Binary-to-Gray Code Converter

For 3-bit binary to gray code converter, input B_0 is identical to output G_0, output G_1 and G_2 is XOR-ed value of inputs B_1, B_0 and B_2, B_1 correspondingly. In 4-bit binary to gray code converter, input B_3 is same to output G_3, output G_2 is XOR-ed value of inputs B_3 and B_2, output G_1 and G_0, is XOR-ed value of inputs B_2, B_1 and B_1, B_0 correspondingly. The simulated circuit layout of proposed 2-bit, 3-bit, and 4-bit binary to gray code converter are presented in Figure 7 (a), (b), and (c) respectively.

4. Simulation Results

The functionality of the proposed circuit is accepted from the simulated output. Figure 8 (a), (b), and (c) organizes the output waveforms of the proposed circuits respectively. The bi-stable approximation is accomplished using the factors as follows:

i. Number of samples =12800;

ii. Convergence tolerance = 0.001000;

iii. Radius of effect = 65.000000nm;

iv. Relative permittivity =12.900000;

v. Clock low = 3.800000e–023J;

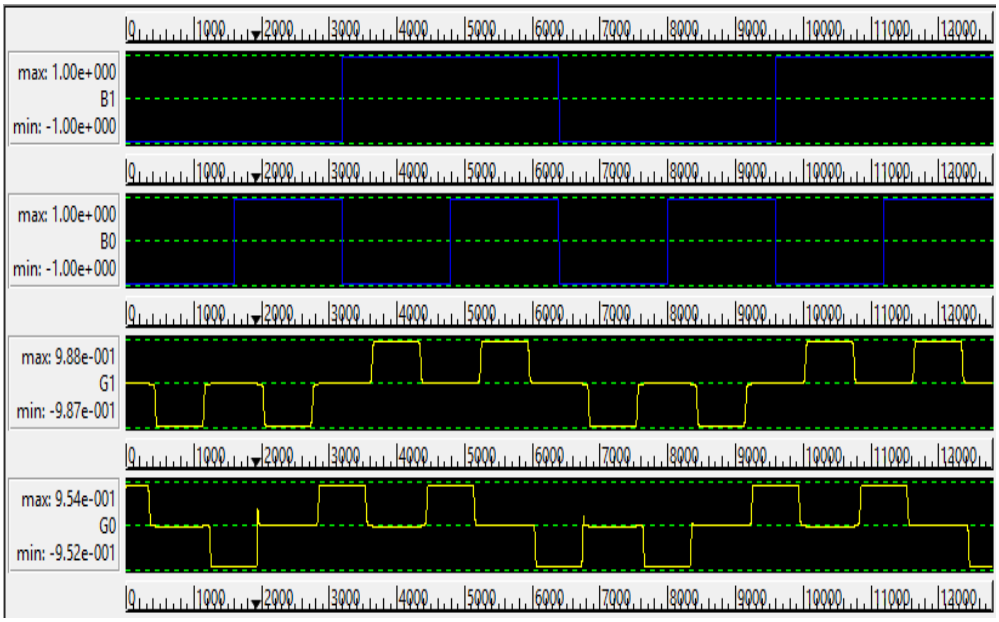
vi. Clock high = 9.800000e–022J;

vii. Clock amplitude factor = 2.000000;

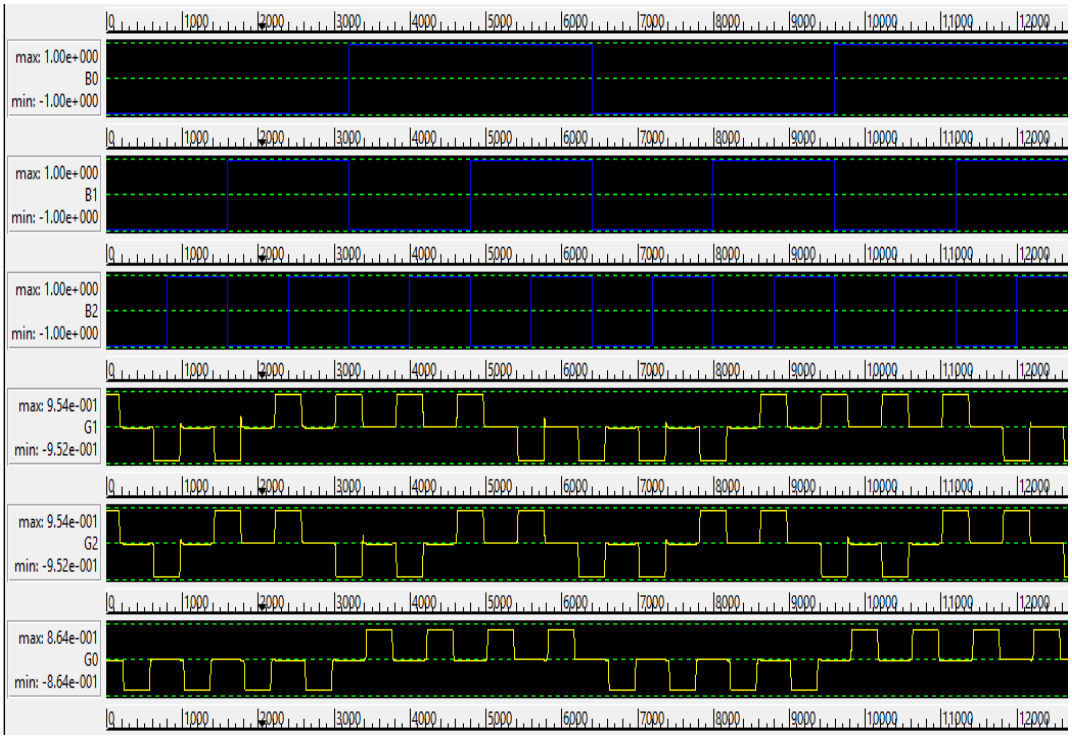
viii. Layer partition =11.500000;

ix. Highest iterations per sample =100;

x. cell width x height =18 x 18 nm.



(a)



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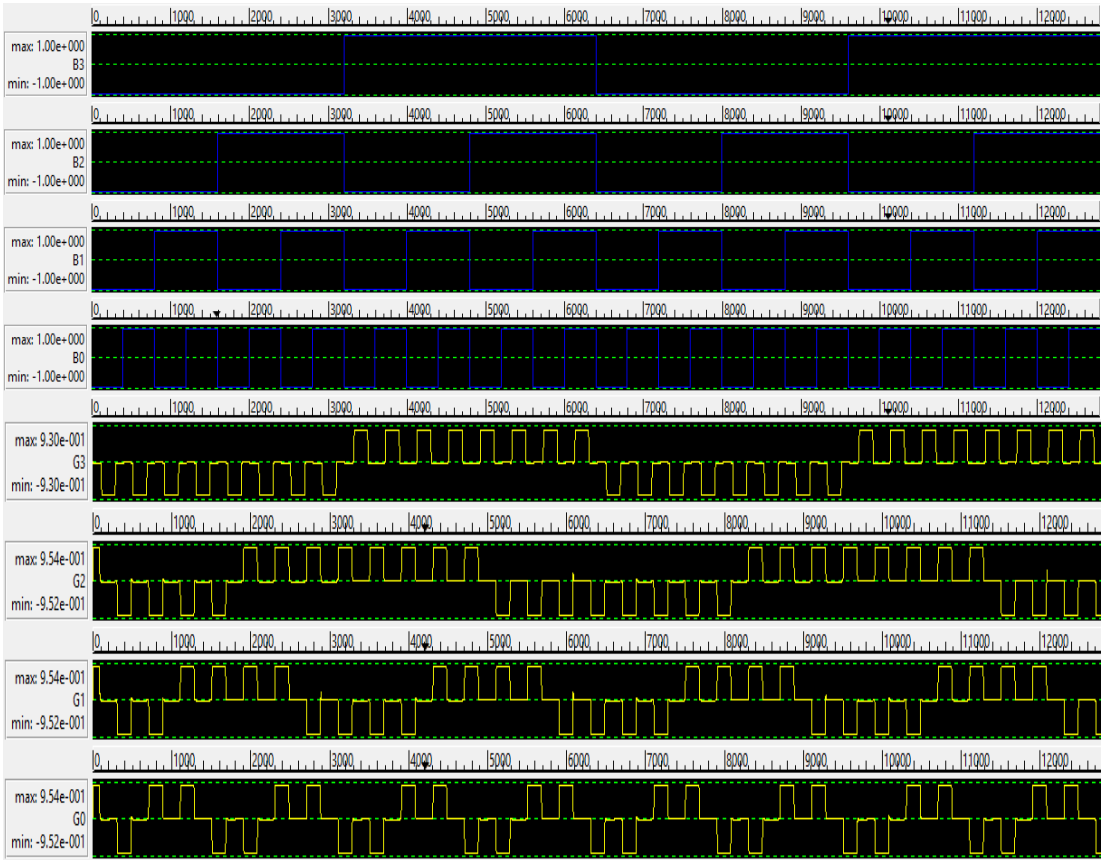
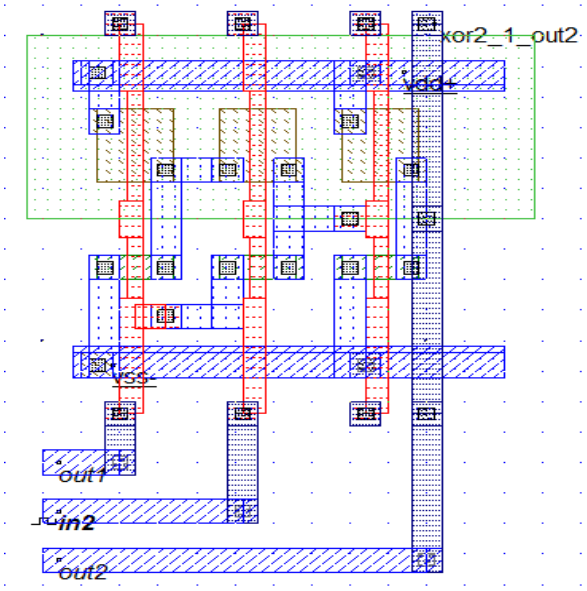


(c)

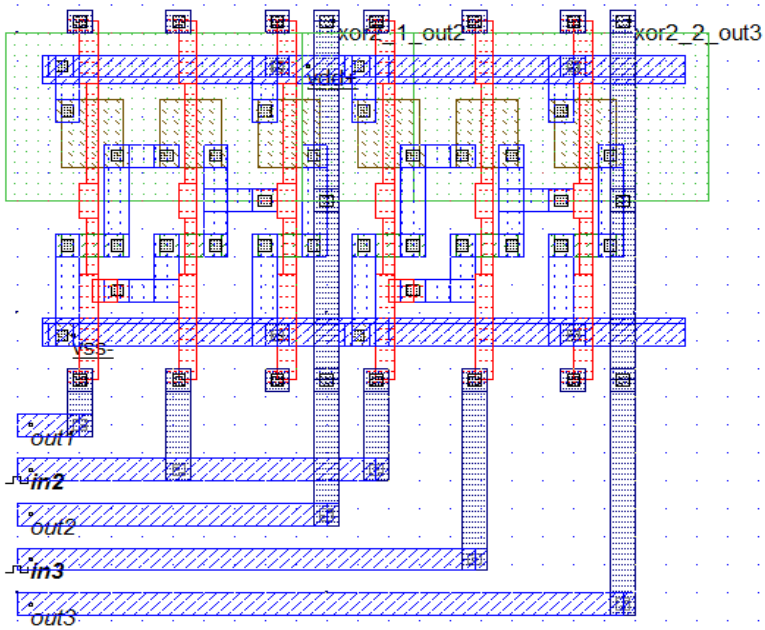
Figure 8. Simulated Results of (a) 2-bit (b) 3-bit, and (c) 4-bit Binary-to-Gray Code Converter

Figure 8(a) displays that for 2-bit binary-to-gray code converter if the inputs are B_0=0 and B_1=0, then the results will be G_0=0 and G_1=0, individually and if the inputs are B_1=0 and B_0=1, then the results will be G_1=0 and G_0=1, separately, and so on. Similarly for 3-bit code converter presented in Figure 8(b) if the inputs are B_0=0, B_1=0, and B_2=1, then result will be G_0=0, G_1=0, and G_2=1, respectively, and so on. For 4-bit code converter in Figure 8(c) if the input B_0=1, B_1=0, B_2=0, B_3=0 then outcome will be G_0=1, G_1=0, G_2=0, and G_3=0, respectively, and so on. Thus, the proposed circuits operate efficiently.

For simulation and design the proposed circuits in CMOS, MICROWIND is employed. This is a user-friendly tool to design and find out the enclosed space of logic circuit. Figure 9 (a), (b), and (c) shows the simulated design of the proposed 2-bit, 3-bit, and 4-bit binary-to-gray code converter in CMOS respectively.



(a)



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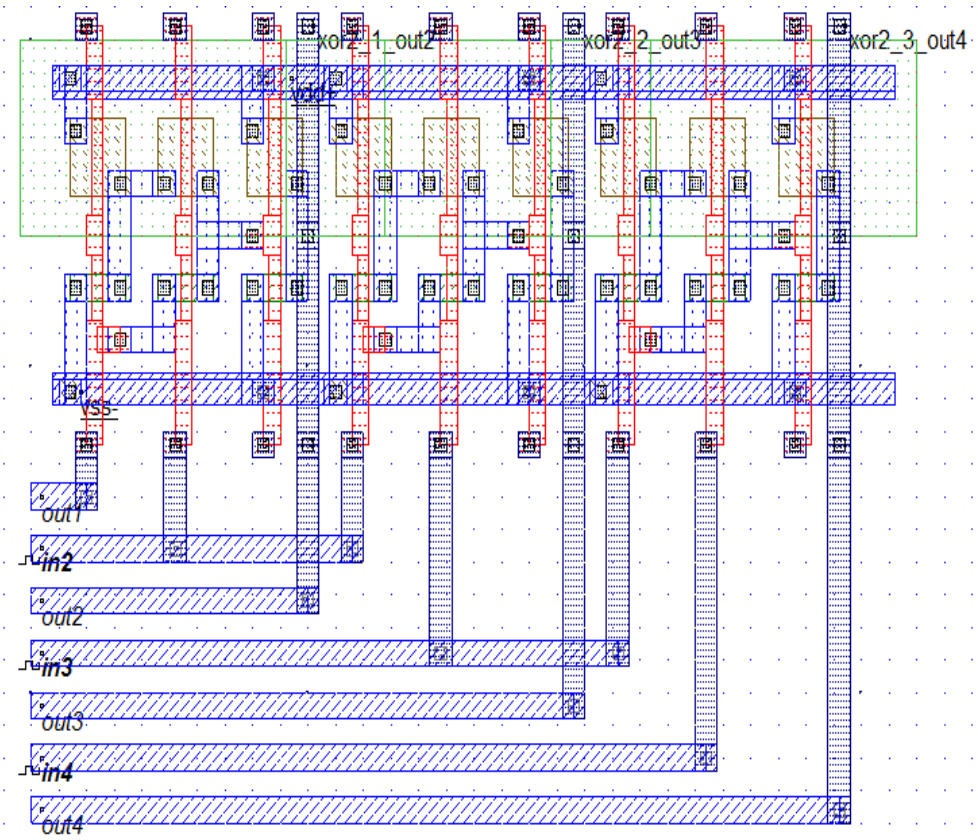
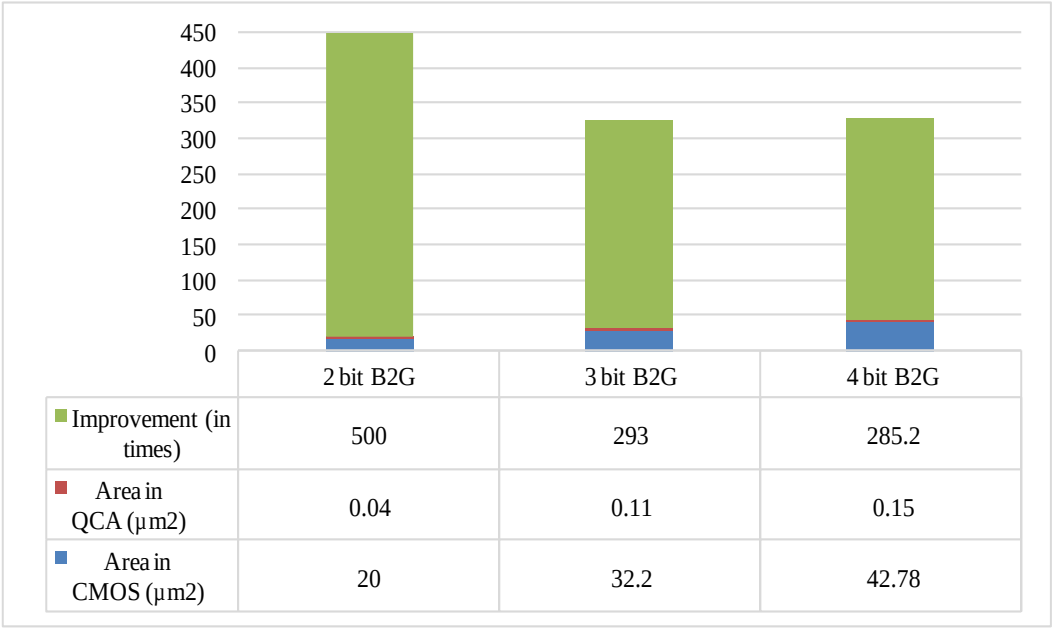


(c)

Figure 9. CMOS Layout of (a) 2-bit (b) 3-bit, and (c) 4-bit Binary-to-Gray Code Converter



	2 bit B2G	3 bit B2G	4 bit B2G
Improvement (in times)	500	293	285.2
Area in QCA (µm2)	0.04	0.11	0.15
Area in CMOS (µm2)	20	32.2	42.78

Figure 10. Comparative Diagram for Area (size) of QCA and CMOS with Improvement

Table 4. Complexity of the Proposed Design

Parameter	2 bit B2G	3 bit B2G	4 bit B2G
Number of Cells	40	82	126
Clock Used	3	3	3
Time Delay	0.75	0.75	0.75
Area in QCA (μm^2)	0.04	0.11	0.15
Area in CMOS (μm^2)	20	32.2	42.78
Improvement (in times)	500	293	285.2

5. Energy Depletion and Consistency of the Proposed Code Converter Circuits

The energy depletion by every single QCA cell in a circuit is identical [45]. So, in an arrangement of identical QCA cells, the entire dissipated energy can be assessed by computing the depleted energy of all QCA cells within the arrangement. The energy depletion by the circuit is reliant on the logic gates used in originating the circuit [45]. The depleted energy of the circuit is the computation of the power depleted by all the majority voters, inverters, and the QCA cells. Estimation of power dissipation by QCA circuits has been attained at temperature T=2K and at separate channeling energies as $0.25E_k$ and $0.5E_k$. The computation is achieved by using the QCA energy dissipation engine QCAPro [46]. This paper, in spite of using the QCAPro energy depletion engine, mathematical valuation of Hamming distance based estimation of energy dissipation [45] is employed to complete the power depletion calculation of the proposed circuits. It has been described that for a variation in the Hamming distance between inputs to the QCA layout, the energy depletion will also be differed. For the inverter, 0→0 or 1→1 input transferring means Hamming distance '0', and the inverter has 0.8 meV depleted power at $\gamma=0.25E_k$ and 8.0 meV at $\gamma=1.0E_k$. Highest Hamming distance of '3' is measured for the majority voter for 000→111 input transferring, which causes the utmost depleted energy of 41.0 meV by the majority voter at $\gamma=0.25E_k$ and 42.9 meV at $\gamma=1.0E_k$. Likewise, the energy dissipation by the majority voter for separate Hamming distances was described in [45]. The proposed QCA design 2-bit binary to gray code converter is shown in Figure 7(a) where three majority voters with single static polarization cell and two inverters is used. Therefore, the majority voter has a Hamming distance of '2' and highest energy depletion the inverter has a Hamming distance of '1'.

Table 5. Power Dissipation of the Proposed Designs

Proposed QCA circuit	Depletion of energy at T=2K			
	$\gamma=0.25E_k$	$\gamma=0.5E_k$	$\gamma=0.75E_k$	$\gamma=1.0E_k$
2-bit code converter	106.7	114.4	120.6	128.7
3-bit code converter	209.4	227.8	241.2	260.4
4-bit code converter	339.1	357.3	383.7	403.4

Table 5 expresses that the power depletion by the proposed 2-bit code converter is 106.7 meV and 114.4 meV at $\gamma=0.25E_k$ and $\gamma=0.5E_k$, separately. A comparable method is applied for assessing the energy dissipation by the proposed 3-bit and 4-bit code converter and the outcomes are presented in Table 5. In Table 5, E_k is the kink energy and γ represents the tunneling energy. The power depletion outcomes are delineated in Figure 11.

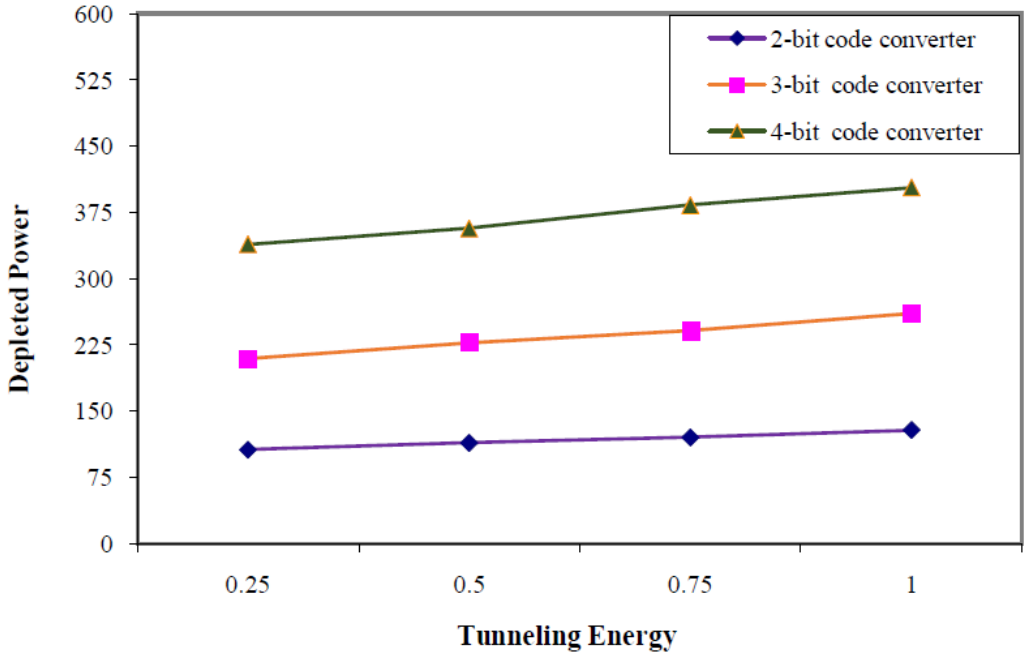
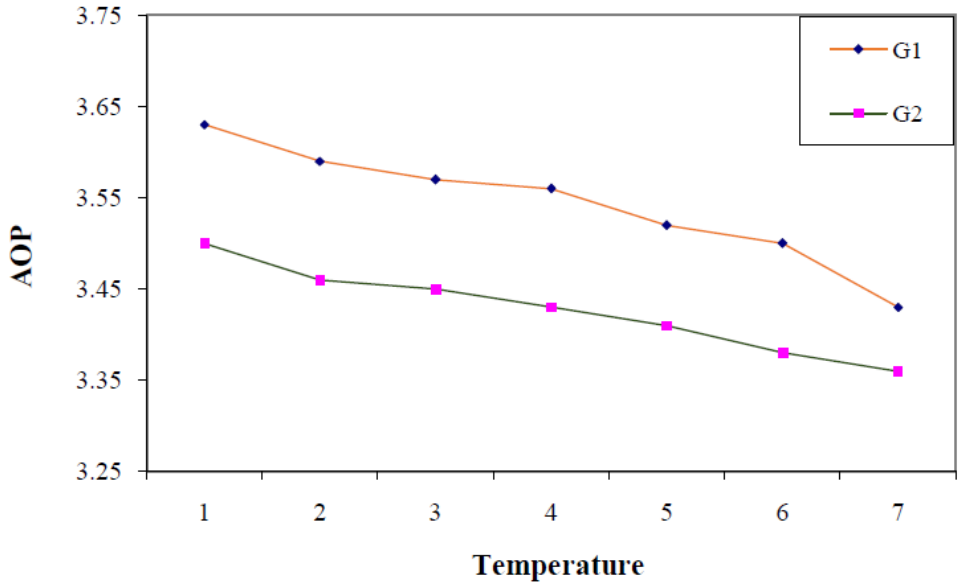
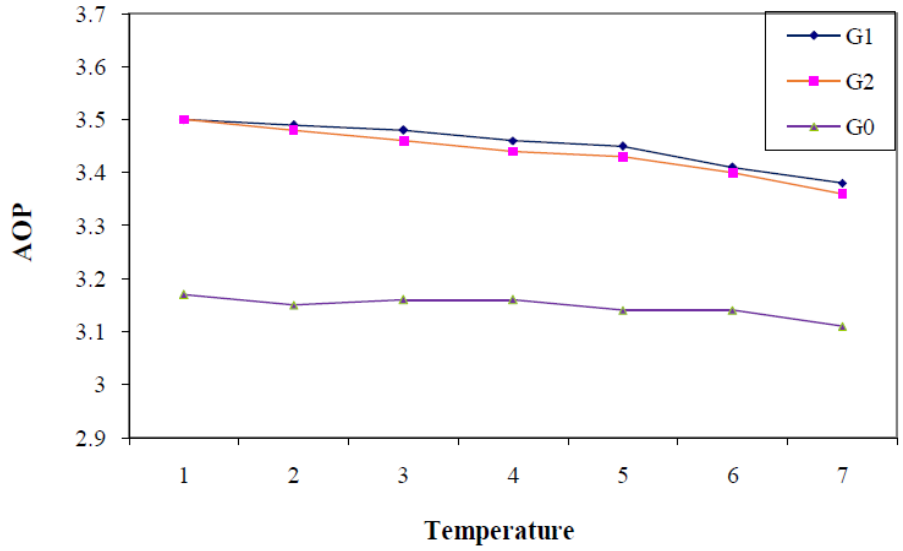


Figure 11. Power Dissipation of the Proposed QCA Designs

The average output polarization (AOP) of QCA output cell is declined by rising the temperature. The temperature consequence on the AOP of the proposed designs is presented in Figure 12. All the proposed code converters will work proficiently between 1 K and 6K as shown in Figure 12. For instance, at T=1K, the highest and least polarizations of output cell G_0 of 3-bit binary-to-gray code converter are 8.64e–1 and –8.64e–1, individually. Hence, the average output polarization for cell G_0 is [(8.64e–1)–(–8.44e–1)]/2 = 3.18. Likewise, the AOPs for separate output cells of every proposed circuit at separate temperatures are analyzed.



(a)



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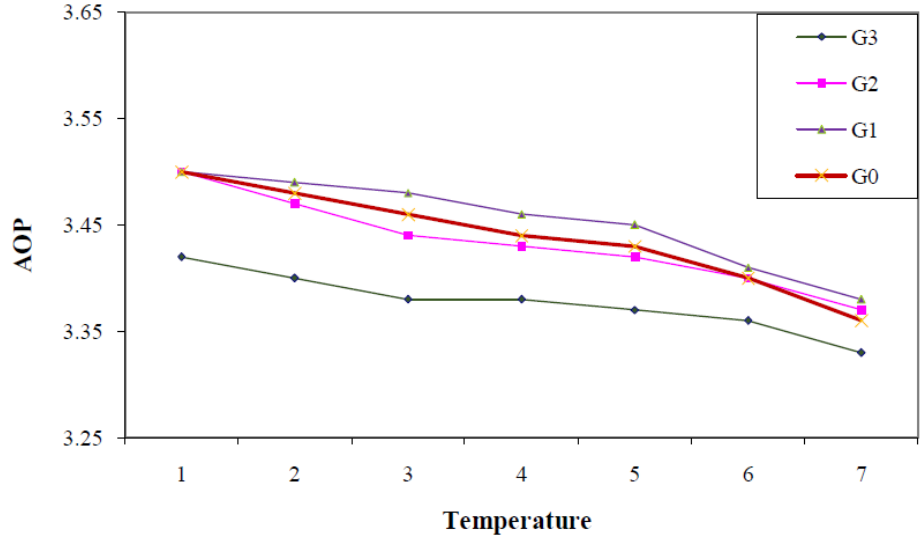

(c)

Figure 12. Effect of Temperature on AOP of the Proposed Circuits (a) 2- bit, (b) 3-bit, and (c) 4-bit Binary to Gray Code Converter

6. Conclusion

QCA is a promising nanotechnology where modules are micro sized and clock speed on terahertz range. In this paper, three binary to gray code converter has been proposed which is 500, 293, and 285.2 times lesser respectively in extent than current CMOS model. QCA based technique exposes a massive direction for circuit design with reduced sizes and by using this technique power efficient circuits can be assembled with enhance accuracy. The proposed circuits have extremely low heat energy depletions, presenting that QCA nano-designs are apposite for realizing reversible circuits. The constancy evaluation of the proposed designs under thermal randomness displays the firmness of the circuits. These layouts could be a potential phase to building ALU's and model more complex circuits in smaller scopes. The simulation outcomes of the proposed circuits with theoretical values verify the functionality of the circuits.

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