International Journal of Multimedia and Ubiquitous Engineering
Vol.11, No.8 (2016), pp.359-366
http://dx.doi.org/10.14257/ijmue.2016.11.8.36

A Fingerprint Sensor with Pipelined Scan Driver for Mobile Applications

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Abstract

This paper proposes a pipelined scan driver architecture for a fingerprint sensor based on an integrator. The proposed pipelined scan driver secures enough time to integrate sensor signals of a fingerprint sensor because a fingerprint sensor based on an integrator requires a large number of clocks to get sensor signals of reasonable SNR. Therefore, the proposed pipelined scan driver reduces an overall image capture time effectively without performance degradation by integrating the sensor signals for several sensor cells simultaneously. A prototype 88x2 array fingerprint sensor combined with the proposed pipelined scan driver were designed in this paper. The implemented pipelined scan driver was simulated with Verilog HDL for the functional verification. The 88x2 fingerprint sensor with a synthesized pipelined scan driver were implemented and simulated using a standard 0.18μm CMOS technology. The simulation results were presented and analyzed in this paper.

Keywords*: fingerprint sensor, pipelined scan driver, capacitive sensor, AOVF integrator, signal integration*

1. Introduction

Mobile devices, such as a mobile phone, performs a lot of things, such as an internet surfing, emailing, SNS, mobile banking, even payment service which require personal identification for secure transactions [3]. A fingerprint is a method of biometric identification and is now widely adopted as a security strengthen device in mobile system because it offers relatively high secure personal verification as well as its convenience in use [2-3].

There are several types of fingerprint sensor, which are based a capacitive array, optical array, a thermal array, an ultrasonic method and *etc.* Among them, the fingerprint sensor based on capacitive array is easy to be integrated to a mobile system because it is very small and low cost as well.

The fingerprint sensor which is based on an AOVF integrator as a capacitive sensor has been introduced [4]. The fingerprint sensor based on an AOVF integrator is easy to be implemented and has very good noise performance and also offers a simple fingerprint sensor architecture. However, the fingerprint sensors based on the integrator require enough time to integrate the signal to get reasonable SNR signal, which will increase the fingerprint image capture time.

This paper propose a pipelined scan driver architecture for a fingerprint sensor based on an AOVF integrator. The proposed pipelined scan fingerprint sensor driver can effectively reduce the image capture time without performance degradation. The proposed fingerprint sensor with pipelined scan driver was designed and simulated using Verilog HDL and 0.18μm standard CMOS technology. The pipelined scan fingerprint sensor driver implemented and simulated using Ultrasim. The simulation results were presented and analyzed in this paper.

ISSN: 1975-0080 IJMUE

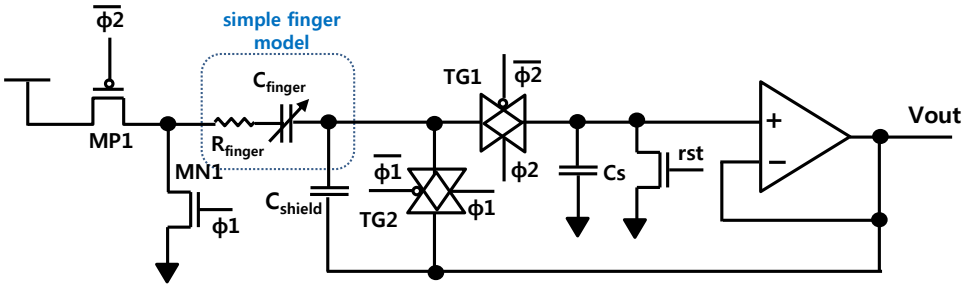
2. Fingerprint Sensor Cell Circuit

Figure 1(a)(b) shows the fingerprint sensor based on an AOVF integrator and non-overlapping two-phase clock which controls the switches of the AOVF integrator, respectively[4].

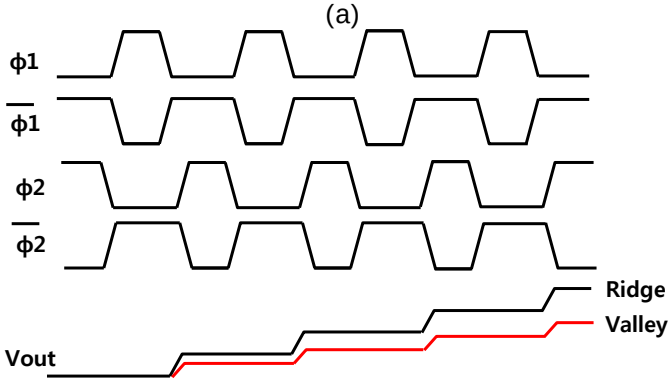
Note that this fingerprint sensor requires an external bezel in order to drive a signal into a finger [4]. The signal fed into a finger returns back through the capacitor formed between fingerprint and the sensor plate, $C_{ridge/valley}$, as shown in Figure 1(c). It is true that enough integration clocks are necessary to get enough output signal difference between a ridge and a valley with reasonable SNR. A variable clock is used to adjust proper gain of the output signal by varying integration intervals [4]. The SNR of the output signal after n-clock integration is expressed as (1) [4].

This circuit structure is applied to each sensor cells which is shown in Figure 1(c). In order to secure reliability issues of a fingerprint sensor in mobile applications, a passivation film might be coated on the fingerprint sensor chip. However, it cannot be avoided degradation of sensitivity of the sensor because the capacitance formed between a sensor plate and a fingerprint is inversely proportional to the thickness of the passivation film. If a 100μm-thick passivation film of relative dielectric constant of 4 is coated, the capacitance value of each sensor cell is less than 1fF for a sensor plate of 50μm x 50μm.

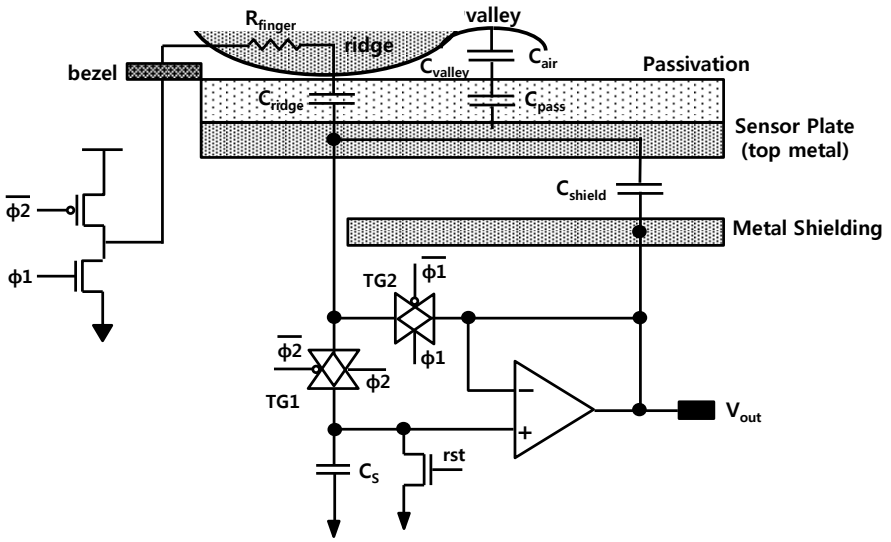
$$SNR_{n-\mathrm{int}} = 10 \cdot \log\left(\frac{V_S^2}{\sigma^2}\right) = 10\log\left(\frac{(n \cdot \Delta V_{out})^2}{\sigma^2}\right) = SNR_{\mathrm{single}} + 20\log(n)dB \quad (1)$$



(a)



(b)



(c)

Figure 1. (a) AOVF Integrator for Fingerprint Sensor Cell, (b) Non-Overlapping Two-Phase Clocks and Integrator's Output Signals, (c) Vertical Circuit and Layout Structure of An AOVF Integrator-Based Fingerprint Sensor Unit Applied in MOS Technology[4]

Although a fingerprint sensor based on the integrator can obtain a high SNR signal by integrating the sensing signal, the increased integration interval of each sensor cell could increase an overall image capture time. This paper propose a pipelined scan fingerprint sensor driver architecture which reduces the fingerprint image capture time effectively without performance degradation. Figure 2(a) shows the proposed a pipelined scan fingerprint sensor driver architecture. The sensor cell array of n x m has been chosen for the proposed pipelined scan driver. V_CK1~m, m of column signal generator, generate a reset and an evaluation signals for the column sensor cells. Every m column cells receives the clock signal from the same column signal generator. For example, V_CK1 controls 1, m+1, 2m+1, and so on. Each column signal generator generates functional signals for the sensor cells, which are a reset signal for starting integration of signal and an evaluation signal for evaluating integrated signal. The m-shift Ring Counter chooses column clock generators at regular intervals. For example, V_CK2 starts to operate at fixed clock interval after V_CK1 starts. Similarly, V_CK3 starts to operate at fixed clock interval after V_CK2 starts and so on. Repeating the processes, V_CK1 starts to operate again at fixed clock interval after V_CKm starts. In this way, m pipelined scan processes are performed. Consequently, m sensor cells can be scanned simultaneously and evaluated in order. V_CK1~m can generate variable period signals which are adjustable for the proper gain of the integrating sensor signal.

XMUX selects a proper column output of the sensor cell array. The 1st-stage XMUX has m inputs and one output. Normally, an analog MUX implemented with transmission gates as shown in Figure 2(c). In order to choose a proper column line for the evaluation sensor cell, it is controlled by V_CKm. Every m-th column lines of the sensor outputs are fed into a 1st-stage XMUX. The 1st-stage XMUX selects one of the column lines using the signals generated from V_CK1~m. Figure 2(b) shows a 2nd-stage XMUX structure. The 2nd-stage XMUX selects one input out of n/m inputs. The 2nd-stage MUX is controlled by the signals generated from XDEC. XDEC uses one of the clock signal from m-Shift Ring Counter as shown in Figure 2(a). In this way, XMUX selects the proper column line output of the sensor array for the evaluating sensor cell.

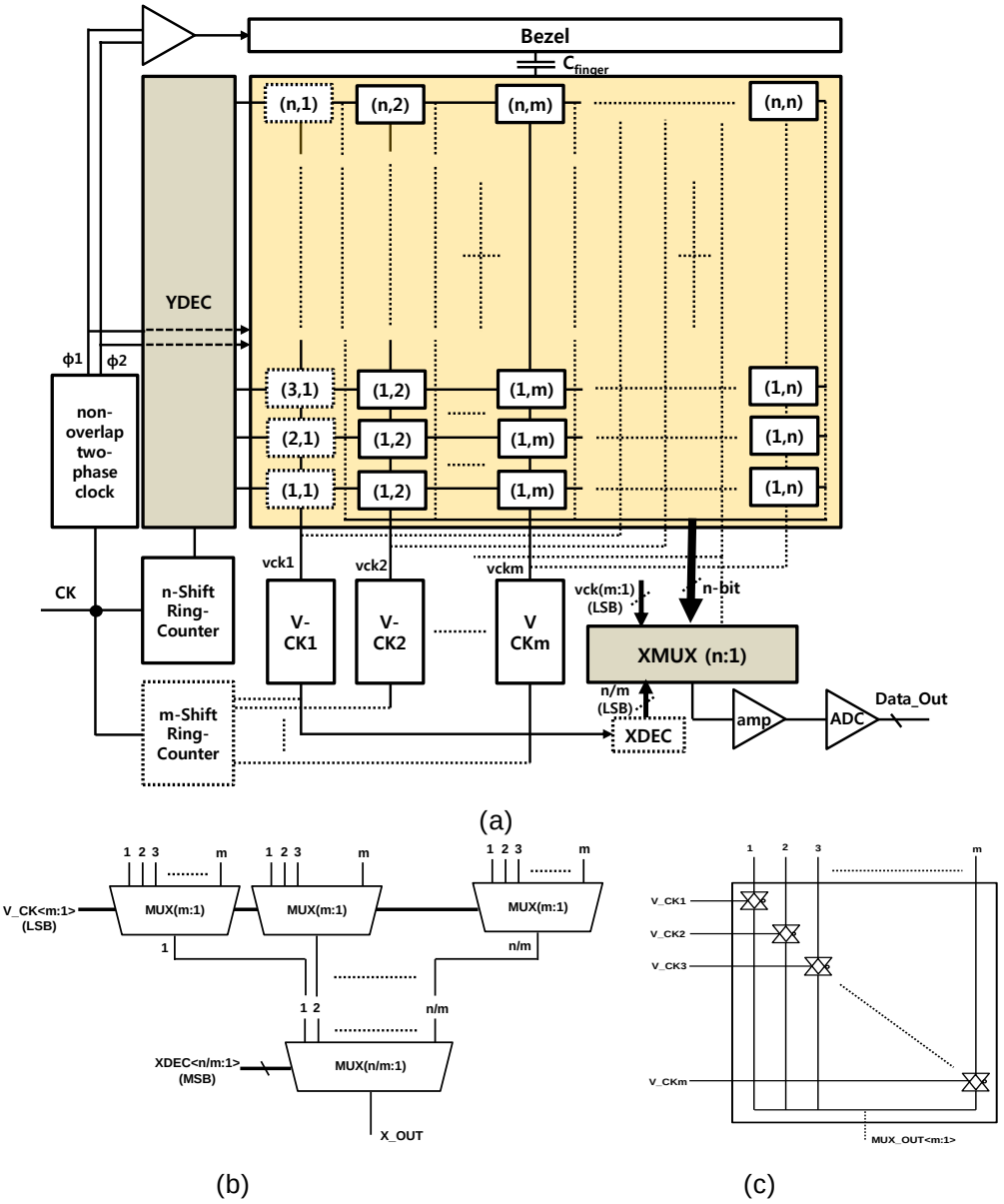


Figure 2. (a) The Proposed Pipelined Scan Driver Architecture for M X N Fingerprint Sensor Based on Integrator (b) N Inputs Two-Stage XMUX Structure (c) 1st-Stage M Input Analog MUX Structure

Figure 3(a) shows the pipelined scan fingerprint sensor driver's simple timing diagrams of V_CK1~m. First, V_CK1 generates a reset signal which is for resetting the signal outputs of the sensor cells and prepares signal integrations. And then V_CK1 generates an evaluation signal after finishing sensor signal integration during a selected period. Meanwhile, V_CK2 generates a reset signal and an evaluation signal like V_CK1. So, V_CK1~m operate at every fixed clock period and have i-clock integration interval between a reset and an evaluation signals as shown in Figure 3(a), where i is an integer. The integration interval, period between a reset and an evaluation signals, can be adjustable to set proper gain of the sensor signal which might determine SNR. m-Shift Ring Counter selects V_CK1 again after V_CK8 finishes operations and then the pipelined scan processes are repeated.

Figure 3(b) shows another example of j-clock interval timing diagrams. V_CK1 starts to generate a reset signal and an evaluation signal with j-clock interval.

V_CK2 starts to generate reset signal at fixed clock period after V_CK1's reset signal. So, V_CK1~m start to generate a reset and an evaluation signals at every fixed clock period of a selected integration interval. Similarly, the pipelined scan processes are carried out as the previous example. The voltage difference between the signals for a ridge and a valley of fingerprint becomes wider because the sensor signals are integrated for j clocks instead of i clocks, where j is an integer greater than i. The different integration intervals would result different output signal level and difference between the signals for a ridge and a valley of fingerprint.

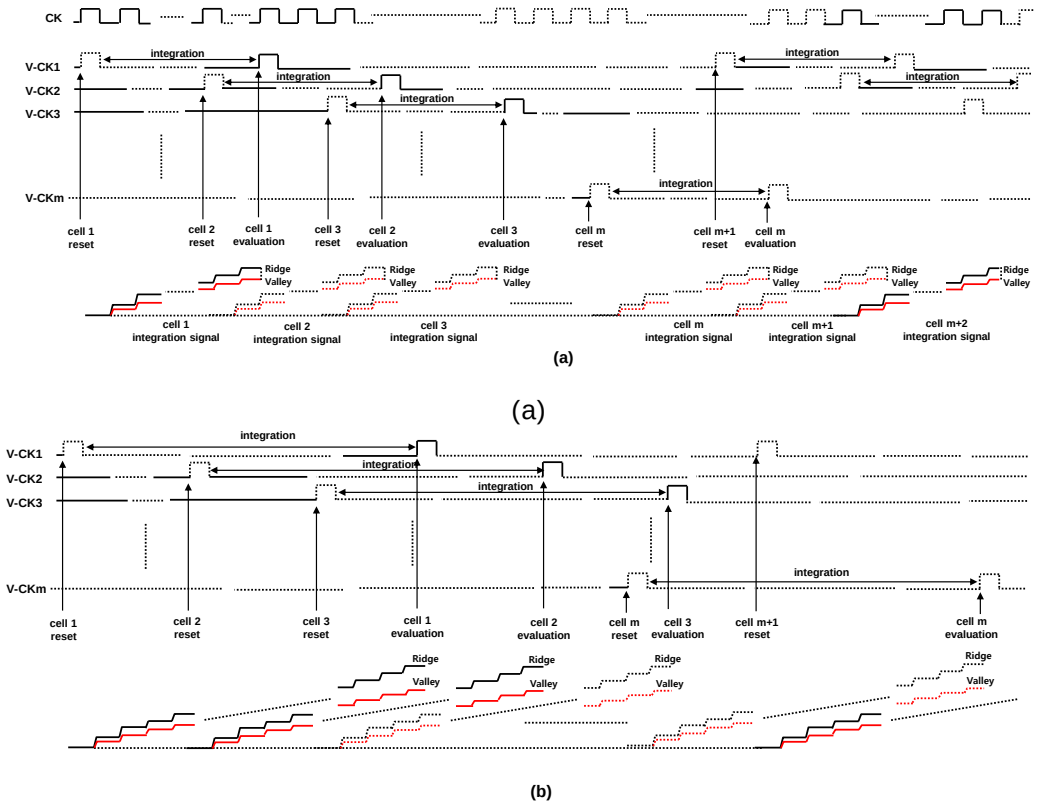


Figure 3. Timing Diagram of the Proposed Pipelined Scan Driver For (a) I –Clock Integration Interval (b) J-Clock Integration Interval

3. Simulations

The eight pipelined scan fingerprint driver was implemented and simulated with Verilog HDL in order to verify the proposed conceptual pipelined scan fingerprint driver's architecture. Figure 4(a)(b)(c) show the timing results of reset and evaluation signals of the proposed pipelined scan driver for 16, 32, and 112-clcok integration interval implemented with Verilog HDL. Since the evaluation signals are required at regular intervals for the pipelined scan processes, only the reset signals are generated from V_CK1~8 and the evaluation signals independently for the implemented pipelined scan fingerprint driver as shown in Figure 4, the logic simulation results. The period of the evaluation signals is 16 clocks regardless of the integration intervals. The start of the evaluation signal varies, which is dependent on the integration interval as shown in Figure 4. And V_CK1~8 start to generate the reset signals in turn at every 16-clock interval regardless of the different integration intervals. The reset signal for 9th sensor cell is generated from V_CK1 again after the reset signal from V_CK8. The simulation results

confirmed that the pipelined scan fingerprint driver implemented with Verilog HDL was working properly.

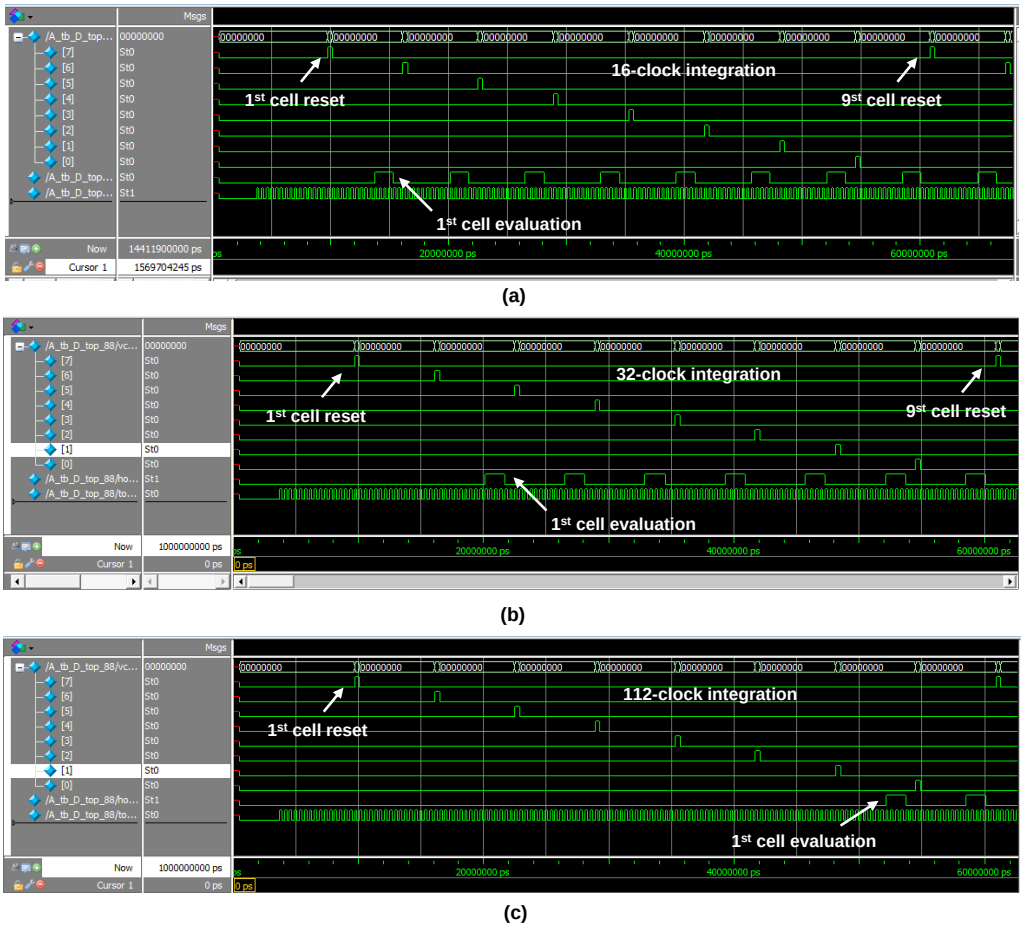


Figure 4. Logic Simulation Results of the Proposed Pipelined Scan Driver for Fingerprint Sensor (a) 16-Clock Integration Interval, (b) 32-Clock Integration Interval, (c) 112-Clock Integration Interval

For the circuit simulations, the proposed pipelined scan fingerprint driver implemented with Verilog HDL was synthesized and fingerprint sensor of 88x2 array based on AOVF integrator combined with synthesized pipelined scan driver was designed using 0.18μm standard CMOS technology. The simulations were performed using Ultrasim. The capacitance formed between a sensor plate and fingerprints was modeled as a capacitor with a series connected 1MΩ resistor. The capacitance of the 1st-cell was 0.6fF which was modeled as a ridge contact sensor cell. This is a comparable capacitance to a capacitance formed between a 50μmX50μm sensor plate and a ridge which is separated with more than 100μm-thick passivation film of relative dielectric constant of 4. Obviously, the thicker the passivation film, the smaller the capacitance of the sensor cell, which is inversely proportional to the thickness of the passivation film. The capacitance of the 2nd-cell was 0.75fF which was modeled as also a ridge contact with different capacitance. Similarly, the third and the fourth cells were modeled as a 0.45fF and 0.75fF. The other cells were modeled as 0.3fF which represents a valley of a fingerprint. The blue solid line in Figure 5 shows the output voltages for 16-clcok integration interval of the each fingerprint sensor cells. The integrated output voltage of the 1st sensor cell was about 0.6V. The integrated output voltages of the 2nd, the 3rd, and the 4th sensor cells were 0.8V, 0.4V, 0.8V, respectively. The output voltage of the other sensor cells were about 0.25V.

The results shows that the sensor cells generate enough voltage levels to identify a ridge and a valley of fingerprint. The red dotted line in Figure 5 shows the output voltage of the each fingerprint sensor cells for 32-clcok integration interval. The output voltages of the 1st, the 2nd, the 3rd, and the 4th sensor cells were increased and the voltage difference between the signal outputs of a ridge and a valley of fingerprint was also increased compared to that for16-clock integration interval as expected. The black dotted line in Figure 5 shows the output voltage of the each sensor cells for 112-clock integration interval. The integrated output voltage of 1st-cell is more than 1.1V and the voltage difference between the signal outputs of 1st-cell and other cell modeled as a valley is more than 0.7V. As shown in Figure 5, the start of evaluation clocks of the 1st-cell was delayed as the integration interval increases. The sensor cells were evaluated at every 16-clock as expected in the pipelined scan process after 1st-cell evaluation. Therefore, the designed pipelined scan driver for 88x2 array fingerprint sensor performs pipeline operations well. As a result, the pipeline scan driver for fingerprint sensor reduces overall image capture time effectively without SNR degradation of the sensor signals.

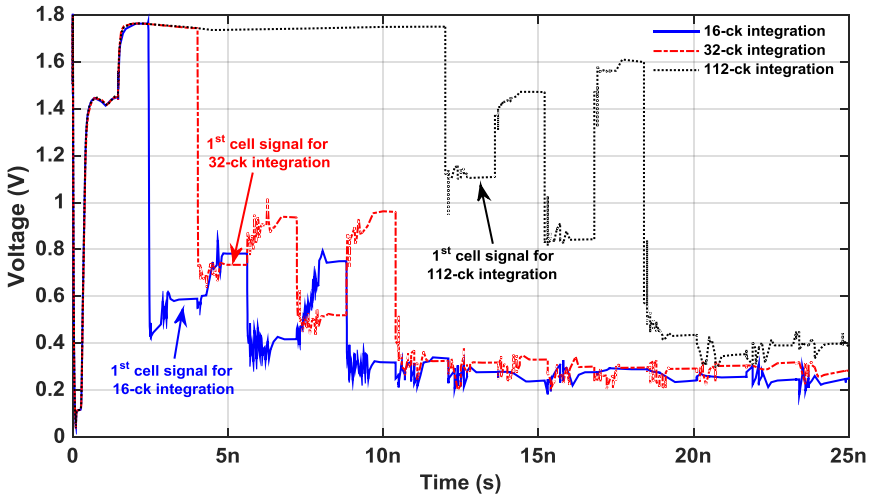


Figure 5. Senor Signal Outputs of the Proposed Pipelined Scan Fingerprint Sensor Based on AOVF Integrator for 16, 32, and 112-Clock Integration Interval

4. Conclusion

This paper proposed a pipelined scan driver architecture for a fingerprint sensor based on an integrator. The proposed pipelined scan driver reduces an overall image capture time effectively by scanning fingerprint sensor cells simultaneously and evaluating sensor cells at regular intervals. An eight pipelined scan fingerprint driver was implemented and simulated with Verilog HDL to verify the proposed conceptual pipelined scan fingerprint driver's architecture. The logic simulation results were verified that the pipelined scan processes of the implemented pipelined scan driver worked well.

For the circuit simulation, a prototype 88x2 array fingerprint sensor based on an AOVF integrator combined with the proposed pipelined scan driver were designed using a standard 0.18μm CMOS technology. And the proposed pipelined scan driver was synthesized using the same technology.

From the simulation results, the evaluation of the integrated output signals of the sensor cells were performed at a regular interval which is 16-clock period regardless of integration intervals. Only the start timing of 1st-cell evaluation varied with the integration intervals. The integrated output signals of the sensor cell were increased

as the integration interval increases, which is roughly proportional to the integration interval.

In conclusion, this paper proposed a pipelined scan driver architecture for a fingerprint sensor based on an integrator for the fast image acquisition without SNR performance degradation. The simulation results showed the proposed pipelined scan driver can effectively be used in fingerprint sensor based on an integrator. Therefore, a fingerprint sensor with a pipelined scan driver can acquire a fingerprint image with fast capture time and high SNR signals. It is also very suitable for mobile applications because the proposed pipelined scan driver enables the fingerprint sensor to acquire a fingerprint image with small power consumptions.

Acknowledgements

This work was supported by Hanshin University Research Grant.

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