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Model-Based Design Methodology for Digital Up and Down Conversion of Software Defined Radio

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Abstract

This paper proposes an efficient implementation of digital up and down conversion for Software Defined Radio (SDR) using Model-Based Design (MBD). In particular, a novel flow for designing digital up and down conversion is detailed. Using MBD, a system model is at the center of the development process, from requirement development, through design, implementation, and testing. Using MBD, code can be automatically generated for system and create test benches for system verification, which is saving time and avoiding the introduction of manually coded errors. Design example shows that the proposed method can greatly reduce the complexity of digital up and down conversion while providing the efficient and reliability of design flow.

Keywords*: Digital up conversion; Digital down conversion; MBD; SDR*

1. Introduction

In terms of signal processing, narrowband systems are generally characterized by the fact that the bandwidth of the signal of interest is significantly less than the sampled bandwidth; that is, a narrow band of frequencies must be selected and filtered out from a much wider spectral window in which the signal might occur in SDR [1]. Digital Up Converter (DUC) and Digital Down Converter (DDC) is two of the most fundamental building blocks for transmission or reception in SDR [2]. Although the algorithms are relatively simple, the number of system variations can be immense and a huge time burden for hardware engineers today, especially when considering the rapid proliferation of new air interface standards and radio architecture requirements. So, engineers are faced with a series of development bottlenecks in the design. Rapidly, effectively to design the new products, which are becoming a new challenge.

On the other hand, the traditional manual of the development process has been difficult to adapt to the current requirements. To solve these problems, the visual design of the model-based development process to introduce circuit design, it is quite necessary. Using models to ensure that a final product meets the system requirements. Models enable engineering teams with different specializations to work together efficiently and to communicate between people working on various stages of the design process; to identify and fix errors early in the development process; and to automatically generate robust, efficient, and high-quality embedded software code and synthesizable HDL code.

The structure of the paper is the following. Key concepts regarding MBD are introduced in Section 2. The main contribution of this work is presented in Section 3 and Section 4, where digital up and down conversion is designed using MBD. The implementation of a design example is illustrated in Section 5. Finally, Section 6 summarizes the main conclusions of this work.

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2. The Development Flow Based on MBD

With the continuous development of embedded systems, people are increasingly demanding for real-time of electronic products, which greatly increased the complexity and difficulty of embedded systems product development. If adopted the traditional development flow, it is not conducive to the development of efficient, high-quality products in the fierce competition of market. In addition, different departments shall be responsible for different processing and communication between departments easily lead ambiguity through paper document. Errors will be transferred and influence the progress of the development flow. If there is a problem, the problem need to be analyzed and validated for a long time due to testing in the completion of the entire design. If the problem occurs at the beginning of the design, the whole design cycle and cost bring great negative effects.

In the MBD [3-4], a system model is at the center of the development process, from requirements development, through design, implementation, and testing. The development flow by MBD is shown in Figure 1. Through the establishment of floating point model, the fixed-point model and the system-level model for presenting a complete system design requirements, different professional engineers work efficiently, and can communicate at different stages of the development flow.

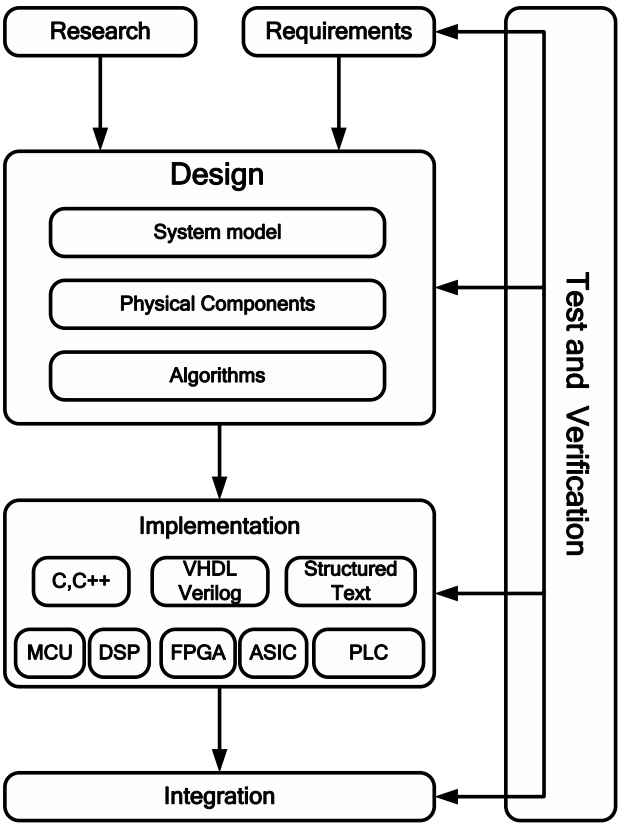

Figure 1. The Development Flow by MBD

All aspects of the design can be tested and verified according to the model of the system level and the demand. Figure 2 is the joint development flow of MBD. System model is performed by MATLAB. HDL tool provides a workflow advisor that automates the programming of Xilinx® and Altera® FPGAs. It can control HDL architecture and implementation, highlight critical paths, and generate hardware resource utilization estimates. HDL tool generates VHDL and Verilog test benches for rapid verification of generated HDL code, automatically generates two

types of cosimulation models. HDL cosimulation model is applied for performing HDL cosimulation with Simulink and an HDL simulator, such as Cadence Incisive or Mentor Graphics ModelSim. FPGA-in-the-loop (FIL) cosimulation model is applied for verifying design with Simulink and an FPGA board.

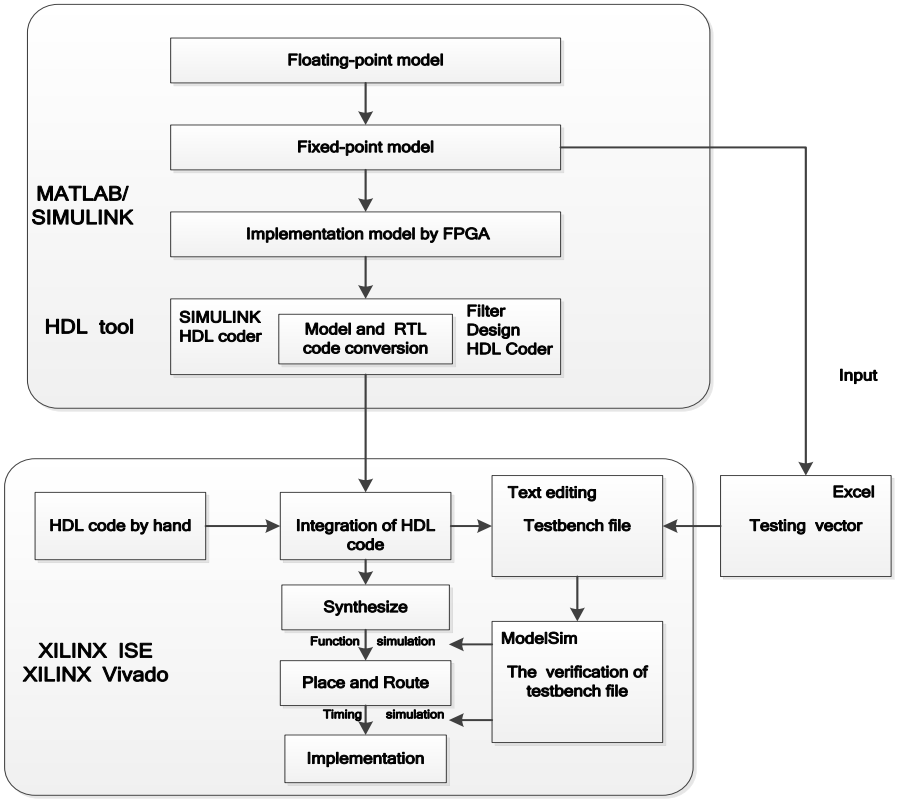

Figure 2. The Joint Development Flow of MBD

3. The Design of DDC Using MBD

Software-Defined Radio (SDR) defines SDR technology as radios that provide software control of a variety of modulation techniques, wide-band or narrow-band operation, communications security functions (such as hopping), and waveform requirements of current & evolving standards over a broad frequency range. It is a rapidly evolving technology that is receiving enormous recognition and generating widespread interest in the telecommunication industry. Over the last few years, analog radio systems are being replaced by digital radio systems for various radio applications in military, civilian and commercial spaces.

The system consists of three main functional blocks: RF section, IF section and baseband section [5-6]. The functional blocks in a generic SDR transceiver system is depicted in Figure 3. The RF section consists of essentially analog hardware modules while IF and baseband sections contain digital hardware modules.

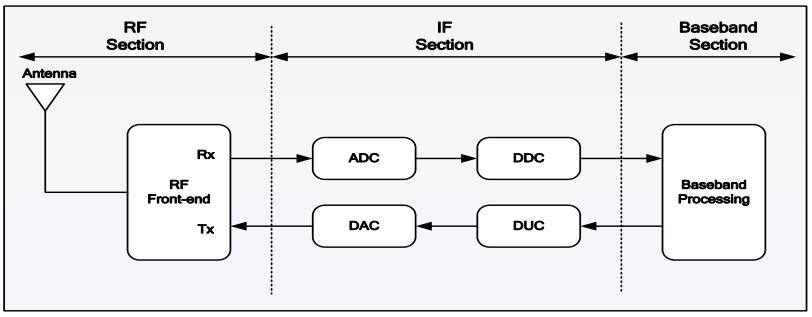

Figure 3. Block Diagram of a Generic SDR Transceiver

A Digital Down Converter (DDC) [7] is the counterpart component to the DUC and is, therefore, equally important as a component in the same application systems. Its function is to translate a passband signal comprising one or more radio or intermediate frequency (RF or IF) carriers to one or more baseband channels for demodulation and interpretation. It achieves this by performing: mixing to shift the signal spectrum from the selected carrier frequencies to baseband, decimation to reduce the sample rate, and filtering to remove adjacent channels, minimize aliasing, and maximize the received signal-to-noise ratio (SNR). The DDC input signal has a relatively high sample rate, generally, the output sample rate of an Analog-to Digital Converter (ADC) which samples the detected signal (often after analog frequency translation and pre-processing), while the output is a much lower rate, for example, the symbol rate of a digital communications system for demodulation.

The DDC System consists of an Numerically Controlled Oscillator (NCO) that down converts an input signal from a specific passband frequency to 0 Hz. The object down samples the down converted signal using a cascade of three decimation filters. The following block diagram shows the DDC in Figure 4. The DDC implements decimation using three filter stages. When the designs the filters internally, the first stage consists of a CIC decimator, the second stage consists of a CIC compensator, and the third stage consists of a halfband, or a lowpass, decimation filter. As in the DUC, the DDC can be allowed to specify characteristics that define the response of the cascade of the three filters, including passband and stopband frequencies, passband ripple, and stopband attenuation.

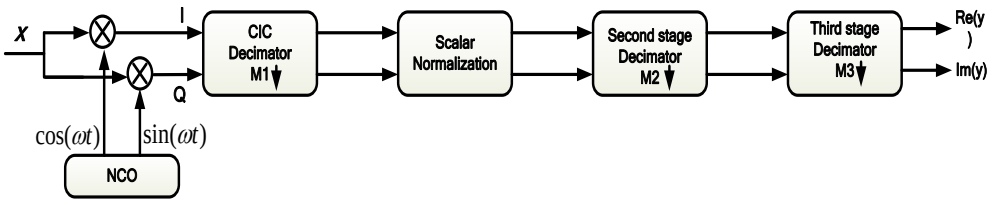

Figure 4. Block Diagram of DDC

The System objects is used for DDC in MATLAB. Design minimum order decimation filters to receive an signal centered at an IF frequency of 455 KHz. Decimate the signal by 40 to downsample it from 2 MHz to 50 KHz. Set the Stopband Frequency Source property to 'Property' and the stopband attenuation to 60 dB to design a cascade response that achieves an ACR of 60 dB. Analyze the responses of the decimator filters and verify that the cascade response achieves an attenuation of 60 dB at 25 KHz. Note how the DDC relaxes the response of the second stage (CIC compensator) to the edge of the left stopband of the first alias of the third stage (lowpass decimator) to minimize order. the cascade response of the decimation filters of DDC is shown in Figure5, and the

response of each individual filter stage and of the overall cascade of DDC is shown in Figure 6.

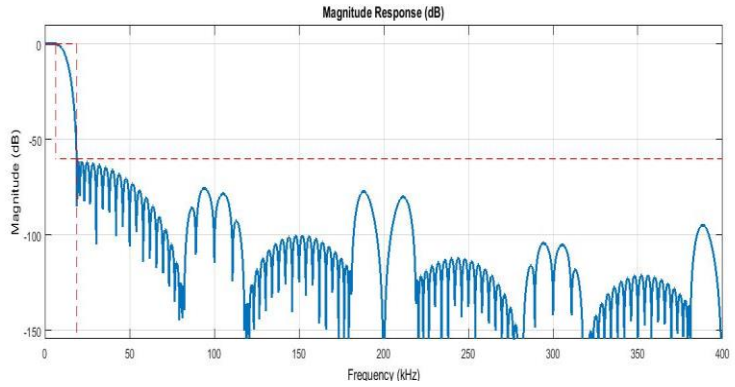

Figure 5. The Cascade Response of the Decimation Filters of DDC

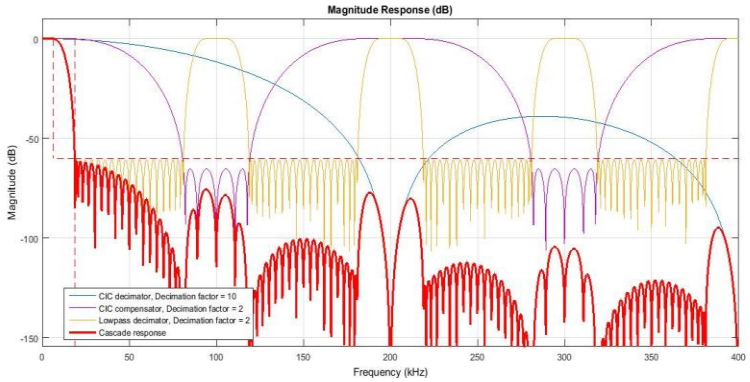

Figure 6. The Response of each Individual Filter Stage and of the Overall Cascade of DDC

4. The Design of DUC Using MBD

A Digital Up-Converter (DUC) [8] is a key component of digital front-end (DFE) circuits for RF systems in communications, sensing, and imaging. The function of the DUC is to translate one or more channels of data from baseband to a passband signal comprising modulated carriers at a set of one or more specified radio or intermediate frequencies (RF or IF). It achieves this by performing: interpolation to increase the sample rate, filtering to provide spectral shaping and rejection of interpolation images, and mixing to shift the signal spectrum to the desired carrier frequencies. The sample rate at the input to the DUC is relatively low; for example, the symbol rate of a digital communications system, while the output is a much higher rate, generally the input sample rate to a Digital-to-Analog Converter (DAC), which converts the digital samples to an analog waveform for further analog processing and frequency conversion.

The DUC consists of a cascade of three interpolation filters and an oscillator that up converts the interpolated signal to a specified passband frequency. The DUC implements the interpolation filter using three filter stages. A block diagram of the DUC is shown in Figure 7.

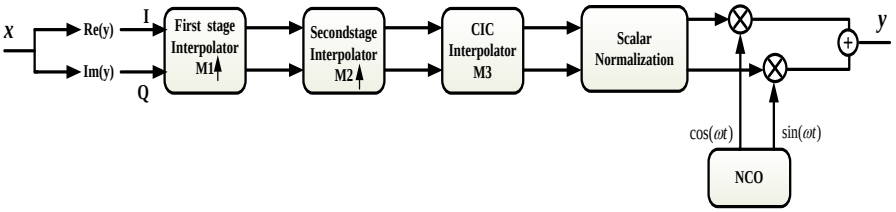

Figure 7. Block Diagram of DUC

When the DUC designs the filters internally, the first stage consists of a halfband, or a lowpass filter, the second stage consists of a CIC compensator, and the third stage consists of a CIC interpolation filter. The DUC object allows you to specify several characteristics that define the response of the cascade for the three filters [9], including passband and stopband frequencies, passband ripple, and stopband attenuation.

The transmitted signal is sampled from 50 KHz to 2 MHz. This yields an interpolation factor of 40. The DUC object automatically factors the interpolation value so that the first filter stage interpolates by 2, the second filter stage interpolates by 2, and the CIC filter interpolates by 10. Set the passband ripple to a small value of 0.05 dB to avoid distortion of the signal. Set the stopband attenuation to 60 dB. the cascade response of the decimation filters of DUC is shown in Figure8, and the response of each individual filter stage and of the overall cascade of DUC is shown in Figure 9.

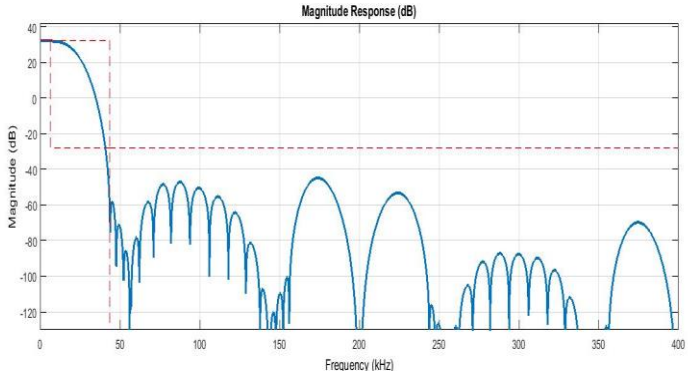

Figure 8. The Cascade Response of the Decimation Filters of DUC

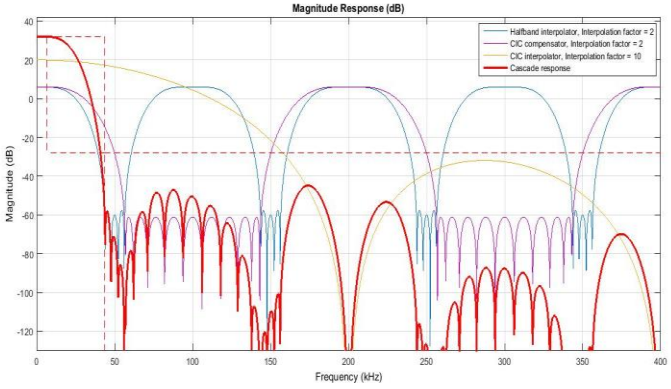

Figure 9. The Response of each Individual Filter Stage and of the Overall Cascade of DUC

5. Design Example Using DDC and DUC

This example shows how to use the digital up converter (DUC) and digital down converter (DDC) System objects to design a Family Radio Service (FRS) transmitter and receiver. The whole system is shown in Figure 10. These objects provide tools to design interpolation decimation filters and simplify the steps required to implement the up/down conversion process.

FRS is an improved walkie talkie FM radio system authorized in the United States since 1996. This personal radio service uses channelized frequencies in the ultra-high frequency (UHF) band [10]. The 8 KHz speech is first resampled to 50KHz. The DUC at the transmitter up converts the signal from 50 KHz to 2 MHz and shifts the signal to an IF frequency of 455 KHz. The receiver has an analog front end that brings the received signal to an IF frequency of 455 KHz. The signal is then sampled at a rate of 2 MHz. The DDC at the receiver brings the signal back to baseband with a sample rate of 50 KHz.

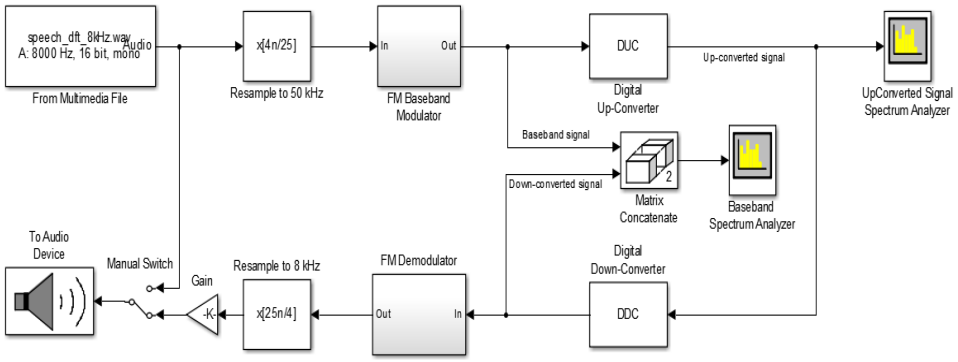

Figure10. The System Using DDC and DUC

In the Up-Converter signal spectrum analysis module, the IF signal can be observed. As shown in Figure 11, baseband signal has been transformed after DUC, the spectrum of baseband signal has been moved to IF of 455 KHZ. In the Baseband Spectrum Analyze module, the spectrum of baseband signal and the down-converter signal can be observed. As shown in Figure 12, the spectrum of the two signals are basically same. Therefore, FRS can be modeled using the DDC and DUC blocks.

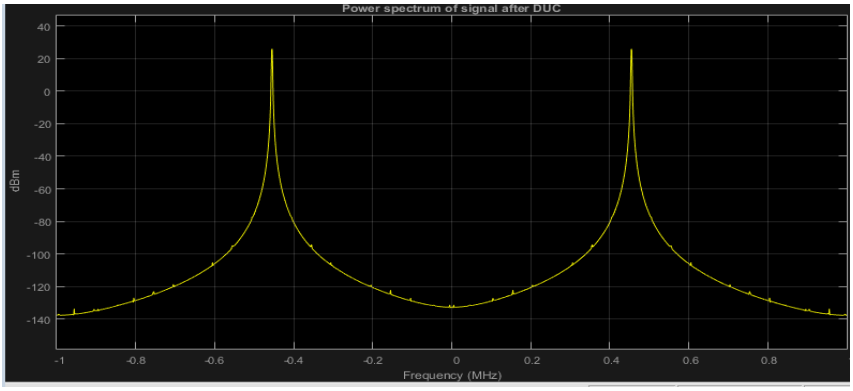

Figure 11. The Spectrum of Up-Converter Signal

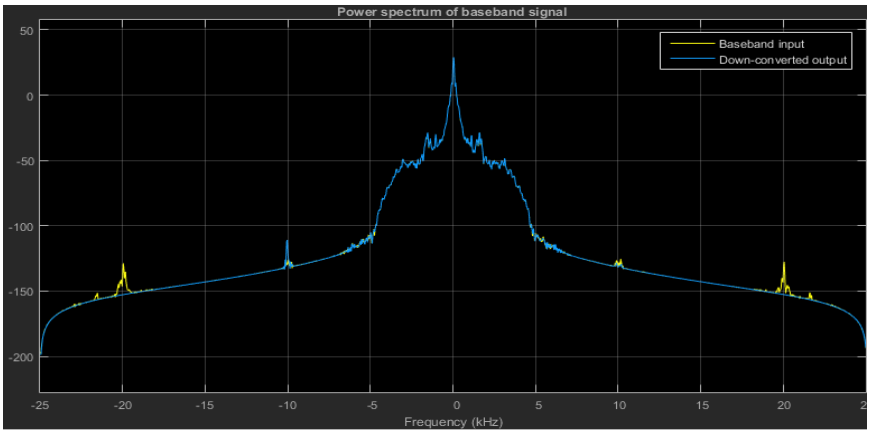

Figure 12. The Spectrum of Baseband Signal and Down-Converter Signal

6. Conclusion

A codesign strategy for DDC and DUC of SDR with MBD is presented in this paper. The design approach is supported by a parameterized model that provides optimized building blocks for a wide variety of modules, and an automatic synthesis tool for rapid description and implementation DDC and DUC of SDR systems. Combining these elements with a model-based design flow supported by different CAD tools running in the MATLAB environment eases the concurrent synthesis and verification of hardware and software components in every design stage. The described methodology allows accelerating the design process of SDR systems. This reduction in development time can be used to optimize a particular solution, as well as to compare different solutions in order to obtain the best tradeoff between cost and performance.

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