International Journal of Multimedia and Ubiquitous Engineering
Vol.11, No.12 (2016), pp.307-318
http://dx.doi.org/10.14257/ijmue.2016.11.12.28

Design of Low Hardware Complexity Multiplexer Using NAND Gates on Quantum-Dot Cellular Automata

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Abstract

This paper presents a 2-to-1 multiplexer based on quantum-dot cellular automata(QCA) with low hardware complexity. A QCA is the computing with cellular automata composed of arrays of quantum-dot devices. We propose a novel 2-to-1 multiplexer using three NAND gates in QCA. We focus on reducing a hardware complexity and minimizing a wasted cell. In order to the implementation of the 2-to-1 multiplexer, we use a new equation using De Morgan's law. Our new architecture also can increase the speed with clock phase.

Keywords*: Nanotechnology, Quantum-dot cellular automata, Majority gate, NAND gate, Multiplexer*

1. Introduction

Since Gordon Moore said that number of transistors on integrated circuits doubles approximately every two years, the reduction of feature sizes and the increase of processing power have been successfully achieved by very large scale integration(VLSI) technology. The microprocessor is one of typical examples, based on VLSI technology, and it is being actively studied in order to increase the integration, performance, efficiency and to minimize the feature sizes. Although many techniques were proposed in order to increase the integration, the development of VLSI technology has reached its peak due to the fundamental physical limits of CMOS technology [1-3]. CMOS technology is reaching its limit beyond which further downscaling in feature size is impossible. High leakage current, high power density levels and high lithography cost crop up with further dimension scaling.

That said, CMOS does have many features that will cause both industry and academia to pursue scaling for the foreseeable future. The robustness of individual devices, relatively high fabrication yields, and existing infrastructure are just some of the characteristics that any new technology will need to eventually mimic. Additionally, with regard to interconnect, although wire delays and pitches may eventually limit scaling, the multiple layers of interconnect associated with CMOS have allowed designers to cross signals and wire up different parts of a circuit with relative ease. Although providing similar functionality has not been the most pressing focus for emerging nanoscale devices, many should still be able to promise at least one additional circuit "layer" for crossings (as efficient methods are essential to continue scaling at the system level). For example, systems of nanowires and nanotubes are orthogonal to each other and can leverage CMOS-like vias to cross signals [4].

Presently, at the transition stage from microelectronic technology to nanotechnology, the basic computer elements essentially vary. Besides, the application area of computers extends. Computers process large volumes of decimal information in financial,

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ISSN: 1975-0080 IJMUE

commercial, Internet-based, and automatic control applications, which cannot tolerate errors from converting between decimal and binary formats. One of the emerging nanotechnologies, the Quantum-dot Cellular Automata(QCA), is considered as a viable alternative to meet the energy efficient design target beyond the limit of existing CMOS technology [5-7].

A QCA is the computing with cellular automata composed of arrays of quantum-dot devices, and basic concepts of it were introduced by Tougaw and Lent in 1993 [5]. The unique feature is that logic states are not stored in voltage levels as in conventional electronics, but they are represented by a cell. A cell is a nano-scale device capable of encoding data by two-electron configuration. The cells must be aligned precisely at nano-scales to provide correct functionality, thus, the proper testing of these devices for manufacturing defects and misalignment plays a major role for quality of circuits [8].

A Multiplexer is an important element in many various QCA circuits, such as the implementation of an FPGA and QCA random access memory arrays. The multiplexer is a combinational circuit which permits picking one output amid numerous inputs. It transfers one of the inputs to the output at a time, so it is also known as Data selector. This type of operation facilitates to share one costly device for more than one application in a system [9].

In this paper, we propose a new design of 2 to 1 multiplexer using NAND gate in QCA. The proposed 2 to 1 multiplexer has been compared to three previous designs in number of cells, terms of area, speed and complexity. In this paper is organized as follows: In Section 2, the background of QCA and multiplexer structures is described briefly. Section 3 shows the previous multiplexer and Section 4 we propose a new multiplexer design and comparison with simulation and conclusions are presented in Section 5.

2. Related Work

2.1. QCA Basic

The QCA scheme is based on a cell which contains four quantum dots and two free electrons, as shown in Figure 1. The quantum dots are shown as the open circles which represent the confining electronic potential, and each cell is occupied by two electrons. The electrons are allowed to jump between the individual quantum dots in a cell by the mechanism of quantum mechanical tunneling. Tunnelling is possible on the nanometer scale when the electronic wavefunction sufficiently `leaks' out of the confining potential of each dot, and the rate of these jumps may be controlled during fabrication by the physical separation between neighbouring dots [10-11]. Normally two electrons are placed diagonally. If cells are located like a Figure 1(a), we call it a polarization of P= +1 and binary 1, while Figure 1(b) are P=-1 and binary 0.

The wires constructed using the two types of cells are shown in Figure 2(a) and Figure 2(b). When an input is applied to the input cell, the binary information propagates from left to the right due to the coulomb repulsion between the electrons of neighboring cells. When all cells in the wire settle down to their ground states, they have the same polarization. Figure 2(b) shows an inverter chain. When all cells settle down each cell in the wire has a different polarization from its neighbors in the wire array. This chain is formed by aligning the quantum dots to be at 45 degrees. The value in an inverter chain changes from '1' to '0' and vice versa as it moves along the wire. [12-13]. Figure 2(c) shows an arrangement of cells that acts as an inverter. The signal comes in from the left on a binary wire and splits into two parallel wires which are offset from the original. Because the incoming wire extends one cell beyond the beginning of the offset wires, aligning effects dominate at the branch point [14]. Figure 2(c) is a robust inverter and

Figure 2(d) is a simple inverter. A robust inverter is a stable state compared to simple inverter. A Simple inverter is better than robust inverter in number of cells.

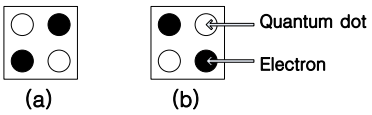


Figure 1. QCA cell: (a) P=+1(Binary 1), (b) P=-1(Binary 0)

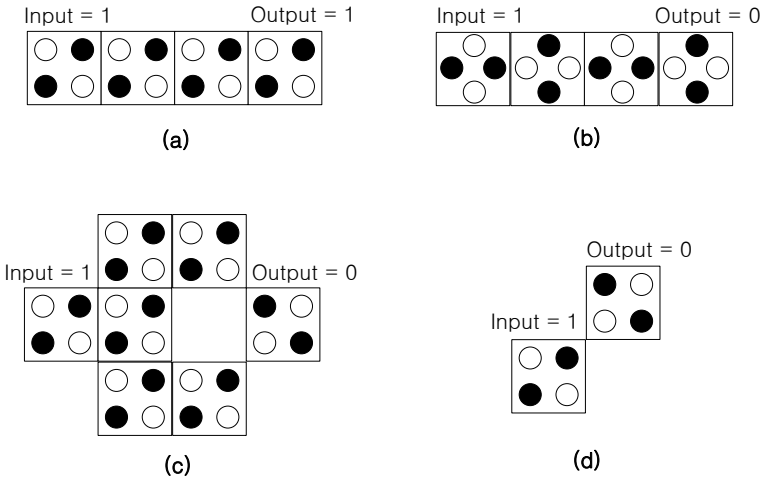


Figure 2. QCA Basic Structures: (a) QCA Wire, (b) Inverter Chain, (c) Robust Inverter, (d) Simple Inverter

In a traditional integrated circuit, the crossing of two wires is achieved by physically passing one wire over the other with an insulator placed between them. Such a nonplanar crossing would also work for two QCA wires, but the cellular nature of such wires allows us to cross them using an entirely coplanar arrangement of cells. Such a coplanar crossing is impossible in conventional circuits which code information using currents and voltages. Coplanar wire crossing is one of the most interesting features of QCA; it allows for the physical intersection of horizontal and vertical QCA wires on the same plane, while retaining logic independence in their values; the vertical wire is implemented by rotating the QCA-cells at 45 degrees *i.e*. by means of an inverter chain. Figure 3 show a coplanar wire crossing in QCA [14].

A majority gate in QCA takes three inputs and implements the majority function of three Boolean variables A, B and C. This function is expressed using the following logic equation (1).

$$M(A, B, C) = AB + BC + AC \quad (1)$$

The AND function can be implemented by setting one value (A, B, or C) in equation (1) to a logical 0. Similarly, the OR function can be implemented by setting one value (A, B, or C) in equation (1) to a logical 1. This results in the equations (2) and (3) [15]. Figure 4 show a QCA majority logic gate.

$$M(A, B, 0) = AB + B(0) + A(0) = AB \quad (2)$$

$$M(A, B, 1) = AB + B(1) + A(1) = A + B \quad (3)$$

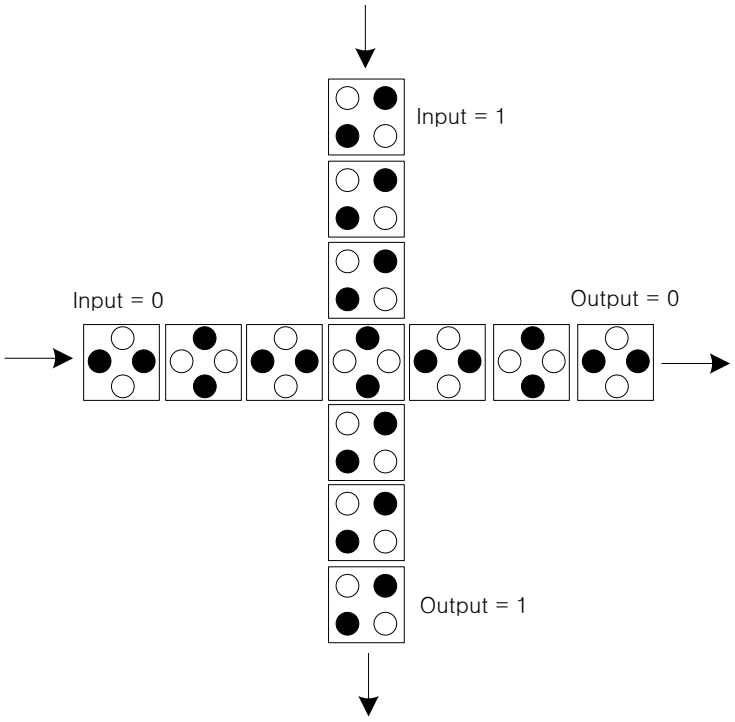


Figure 3. QCA Coplanar Wire-Crossing

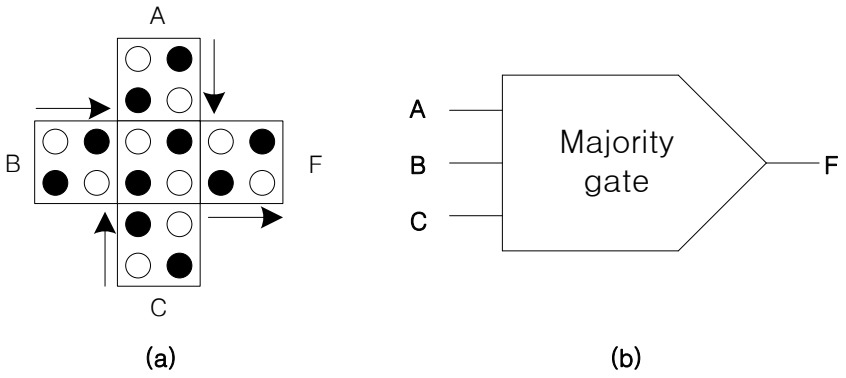


Figure 4. QCA Majority Logic Gate: (a) Using QCA Cells, (b) Majority Gate Diagram

Clocking (by application of an appropriate voltage to a cell) leads to adjustment of tunneling barriers between quantum dots for transfer of electrons between the dots. Each QCA cell is clocked using a four-phase clocking scheme as shown in Figure 5 [16]. The four clock phases are switch, hold, release and relax are utilized in the four clock signals. In the switch phase, the cells begin to compute the value; the cells are unpolarized and have low potential barriers which begin to raise. In the hold phase, the value is held and the barriers are held high. In the release phase, the barriers are lowered and lastly, in the relax phase, the barriers remain lowered where the cells remain unpolarized. The phases allow for a reliable signal transmission and also functional gain which is of paramount importance in computational systems [17-18].

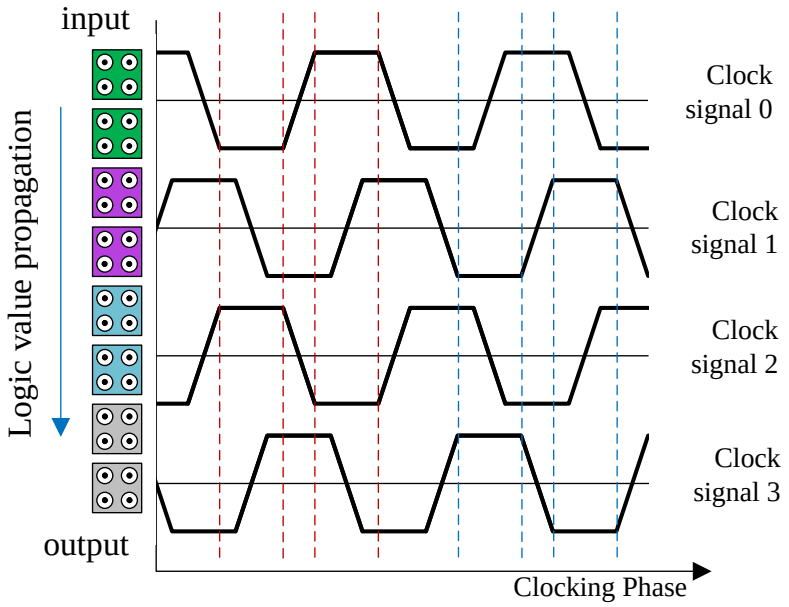
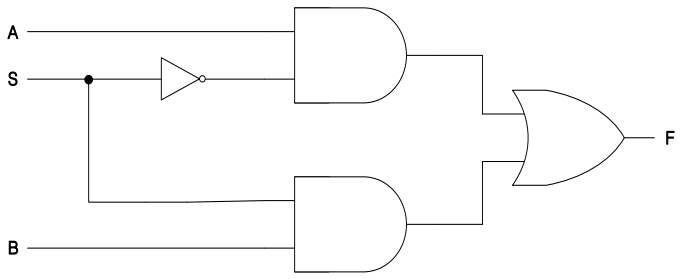


Figure 5. QCA Clock Phases

2.2. Multiplexer

A multiplexer is a combinational circuit that selects binary information from one of many input lines and directs the information to a single output line. Multiplexers have a considerable role in the digital systems which allow to select one of the input's flows for transmitting to the output. Whereas all the logic functions can be built by multiplexers, implementation of multi-input multiplexer in the one layer is a remarkable subject. The main building block of QCA circuits is majority gate and consequently the other logic circuits are implemented based on majority gate [19]. The functionality of multiplexer is shown in equation (4). A and B are the two inputs and S is used to select one between the two inputs. A multiplexer is illustrated diagram and using three majority gates in Figure 6. Table 1 shows the truth table of 2-to-1 multiplexer introduced in Figure 6 [20].

$$F = AS' + BS \tag{4}$$



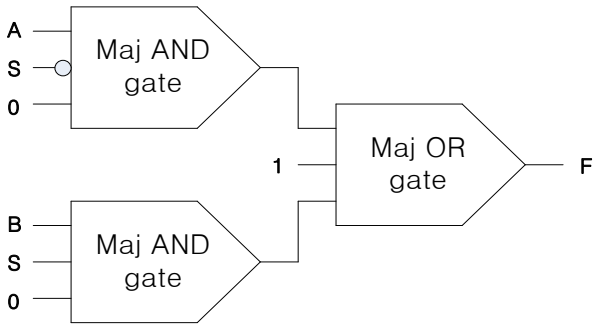


Figure 6. Multiplexer Diagram

Table 1. Truth Table for 2-to-1 Multiplexer

S	A	B	F
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

3. Previous Design

Many multiplexers have been proposed in various ways. Figure 7, Figure 8 and Figure 9 show a different way to construct 2-to-1 multiplexer and simulation result [21-23]. Mardiris's multiplexer [21] use two majority AND gates, one majority OR gate and two simple inverter. In addition, this multiplexer has been constructed using coplanar wire-crossing scheme. This structure consists of 67 cells and covers an area of 81,648nm^2. Mukhopadhyay's multiplexer [22] also use the same gates and wire-crossing implementation but they use different inverter. They use a robust inverter, so they are more stable state compared to using simple inverter.

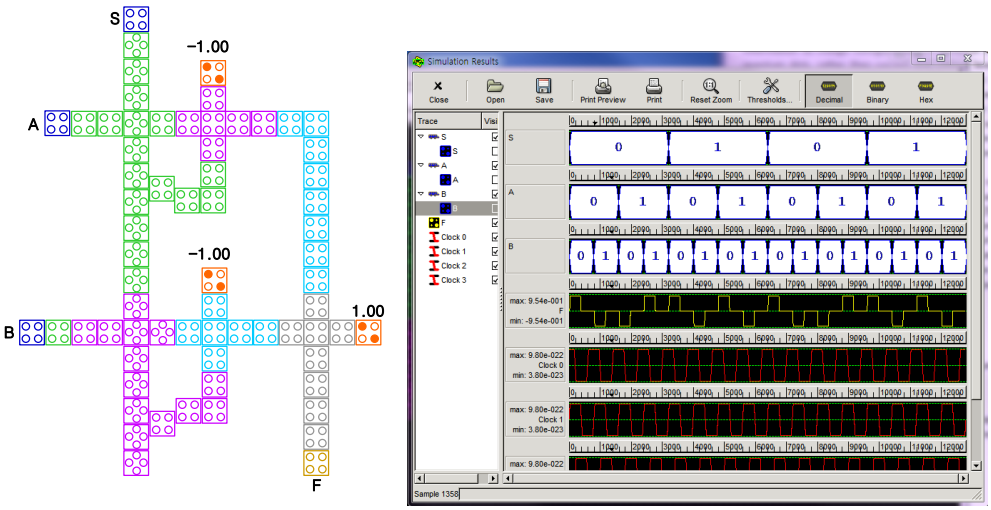


Figure 7. Layout of 2 to 1 Multiplexer and Simulation Result by Mukhopadhyay [21]

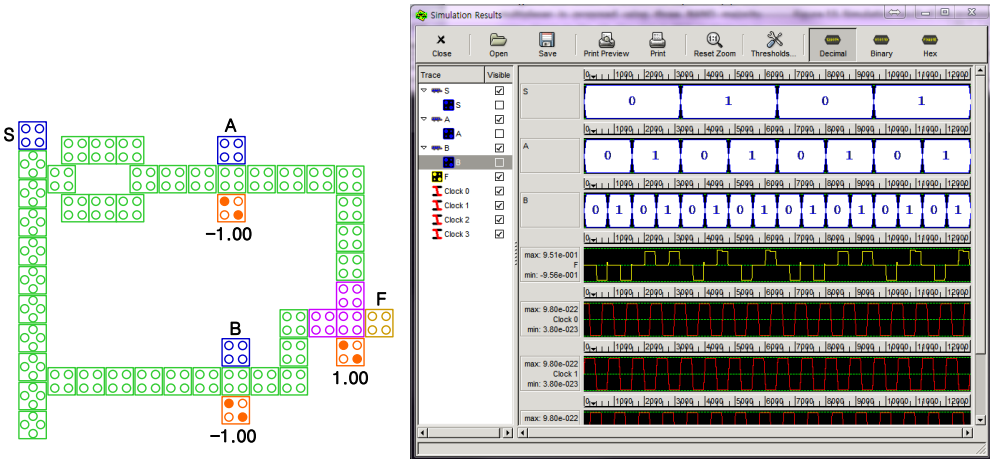


Figure 8. Layout of 2 to 1 Multiplexer and Simulation Result by Hashemi [22]

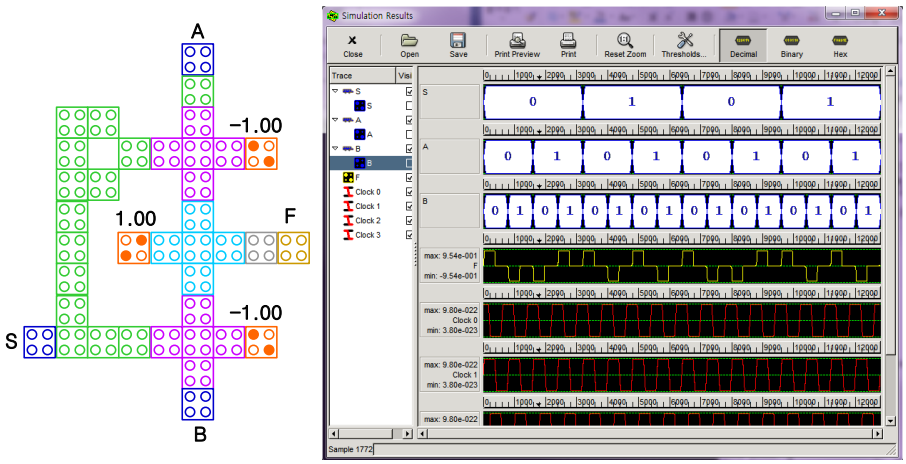


Figure 9. Layout of 2 to 1 Multiplexer and Simulation Result by Mardiris [23]

This structure consists of 49 cells and covers an area of 46,332nm^2. They all use a coplanar wire crossing scheme. Hashemi's multiplexer [23] do not use any wire crossing scheme. The design use two majority AND gates, one majority OR gate and a robust inverter. This structure is composed of 38 cells and requires an area of 37,908nm^2.

Simulation results are shown in each Figure. As you see the result, they have all right results but different signal strength. In Figure 9 and Figure 9, the signals indicate from -9.54e-001 to 9.54e-001 while Figure 8 shows -9.51e-001 to 9.56e-001. In other words, the multiplexer shown in Figure 7 and Figure 9 have strong signals compared to the multiplexer in Figure 8. Since the circuit shown in Figure 9 is more compact and simple and uses robust inverter but still use many cells and area.

4. Proposed Design and Analysis

In this paper we propose 2-to-1 multiplexer in QCA. In order to low hardware complexity, we use another equation using De Morgan's law which is shown in equation (5). When the control signal S is 0, then input A comes out and when the control signal S is 1, then input B comes out. Table 2 shows the truth table of proposed 2-to-1 multiplexer. Our multiplexer diagram is proposed using three NAND majority gates shown in Figure 10 [20].

$$F = (A + S')' + (B + S)' \tag{5}$$

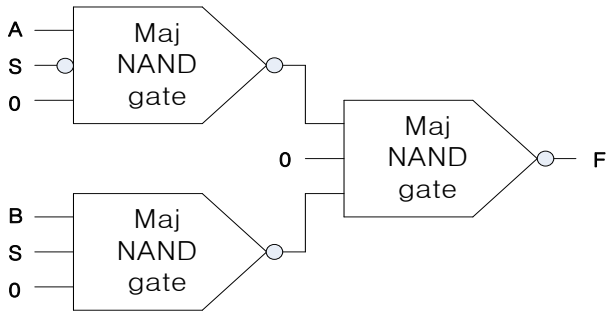


Figure 10. Proposed 2 to 1 Multiplexer Diagram

Table 2. Truth Table for Proposed 2-to-1 Multiplexer

S	A	B	F
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

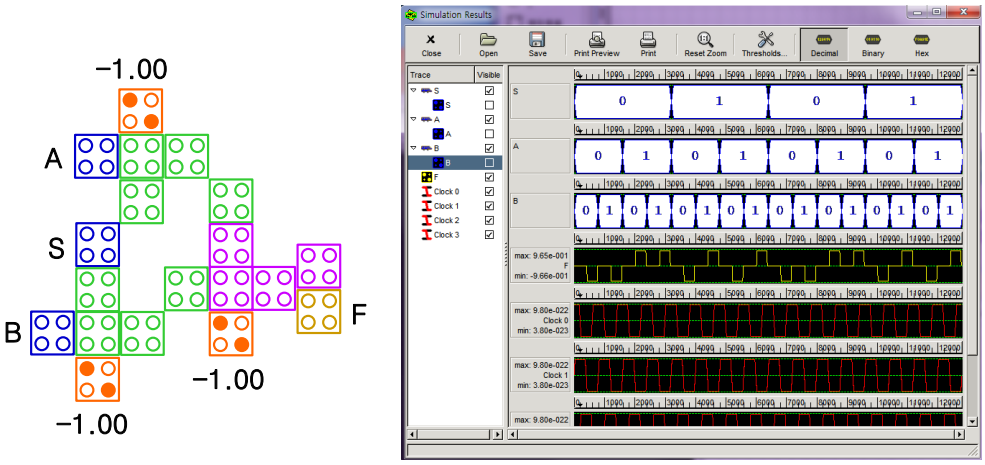


Figure 11. Layout of Proposed 2 to 1 Multiplexer and Simulation Result

The NAND gates are implemented by three input majority gate with inverters. Our proposed 2-to-1 QCA multiplexer is shown in Figure 11. The design uses three majority AND gates and three inverters. We use two simple inverters to minimize the number of cell and one robust inverter to maximize a signal strength. We also add one cell in up of the output cell for maximize a signal strength. We only use 19 cells over an area of 15,876nm^2. Our multiplexer has been designed using QCADesigner.

The proposed multiplexer is simulated using QCA designer tool and is efficient in terms of cell count and area. Our design has focused on not only hardware complexity but also time complexity. As you see in Table 3, we observe that cell count, total area and clock phase are advanced more than previous design. In comparison, our design has 80.5%, 65.7% and 58.1% improvement in the total area compared to previous structures. We have also used proper clock phases so that we have a strong signal with a compact structure. Our design's signal strength is 9.65e-001, so our multiplexer have a strong signal better than other structures. Also, we can implement a multiplexer by only NAND gates. A NAND gate is smaller, area-wise and faster than other circuits. As a result, the proposed design is better than the previous structures. Plus our structure needs only 2 clock phases to get the final result.

5. Conclusion

In this paper, we proposed 2-to-1 multiplexer based on QCA with low hardware complexity by minimizing unnecessary cells and total area. We have also used only two clock phases to get the final result. We have used both robust and simple inverters so that we could keep the strong signal in spite of a simple structure. We expect that our structure will be efficiently used as a component structure for constructing bigger circuits.

Table 3. Comparison of 2 to 1 Multiplexer

	Mardiris *et al.* [21]	Mukhopadhyay *et al.* [22]	Hashemi *et al.* [23]	Ours
Number of cell	67	49	38	19
Total area (nm^2)	81,648	46,332	37,908	15,876

Clock phase	4	2	4	2
Signal strength(max)	9.54e-001	9.51e-001	9.54e-001	9.65e-001
Used gate	AND, OR	AND, OR	AND, OR	NAND

Acknowledgments

This work was supported by the National Research Foundation of Korea(NRF) grant funded by the Korea government(MSIP) (NO. NRF-2015R1A2A1A15055749).

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