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Memory Cell Designs with QCA Implementations: A Review

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Abstract

Quantum-dot-cellular-automata is a potential technology for low power and high density memory designs. In this paper a comprehensive review of parallel and serial QCA memory-cell designs are presented. It is shown that a loop-based serial memory-cell design is better in terms of latency, clocking and timing, hardware requirement.

Keywords*: Memory Architecture, Quantum-Dot –Cellular-Automata (QCA)*

1. Introduction

CMOS circuit designs are scaling down from 6nm to 7nm in area but one cannot continue to follow Moore's Law because the transistor size is now reaching to its physical limits. New techniques like Quantum-Dot-Cellular-Automata which uses the position of electrons confined with-in a QCA cell to represent the logic state of a memory cell is being utilized. The two types of Quantum based memories are Parallel memory and serial RAM memory. These QCA memories are based upon memory-in-motion paradigm [1] *i.e*. memory logic should keep in motion by using QCA cells.

Parallel memory architecture design in QCA offers low latency at the cost of reduced density [2]. Parallel memory utilizes one-bit per memory cell like the traditional CMOS Random Access Memory (RAM) design, but in QCA such memory design offers repetition of the Write-Read circuitry for each RAM-cell or a memory bit. It increases the hardware in terms of number of QCA cells, clocking zones and control cells [3]. This structure offers fast operations at the cost of reduced density.

Unlike Parallel Memory Design, the serial memory architecture utilizes one memory cell for storing multiple bits. This structure efficiently utilizes the sharing of Read/Write circuitry between the bits [5]. Such structure has the advantage of less hardware requirement and high density memory design. Hence the serial memory architecture consumes less area, simpler design *i.e*. high density [6] but at the cost of low operating speed.

QCA memory which utilizes the advantages of both parallel as well as serial memory design [12] can be designed called Hybrid memory [22-23].The Author of paper [14] presented a storage design which is based on memory in motion paradigm.

This Paper organizes as follows: In Section II parallel memory cell design with line based approach is described. Section III provides the introduction to serial memory cell design. Section IV briefs the Surveyed Memory-Cell designs where previous structures of RAM cell designs are presented. Finally the conclusion is drawn in Section V.

2. Parallel Memory Architecture

Parallel QCA RAM-cell architecture utilizes the sharing of various zones of clock between the QCA memory cells in a column. The basic architecture of parallel memory-cell design is Line-based in which the bits are stored in straight line of QCA cells by moving the bits in back-forth direction as shown in Figure 1.The three columns shown in Figure 1 represents three clocking zones. In QCA designer software.

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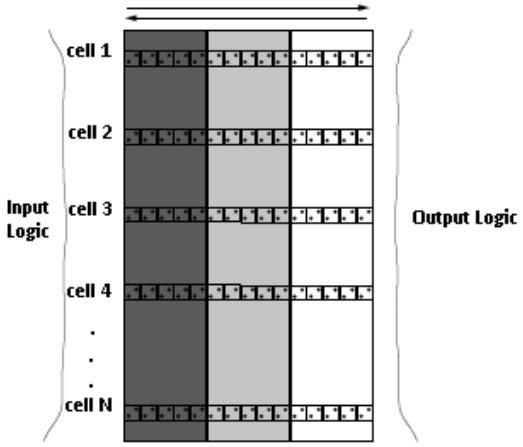

Figure 1. Line-Based Design in Parallel Memory Architecture [1]

By default four clocking zones are available. By utilizing these four clocking zones efficient memory-cell design can.

Figure 2. Conventional Four –Phase Clock Zones of Parallel Memory-Cell Design

Be achieved. These four clocking zones are: Relax Switch, Hold and Release as shown in Figure 2.

Figure 2 is representing Quasi Adiabatic operation of a QCA cell which utilizes four zones of clock cycles. The condition that the bit is stored in a QCA Line is that it should be in a Hold phase of a clock Signal. Hence the clocking zones for parallel memory design are shared column-wise.

A. Parallel QCA Memory-Cell Design

A parallel QCA memory cell design with Read/Write logic is shown in Figure 3.It's QCA implementation is presented in Figure 4.

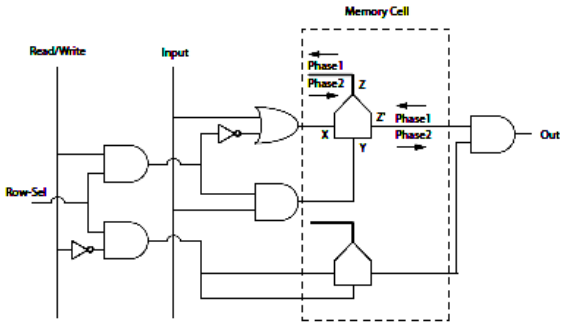

Figure 3. Line Based QCA RAM Cell Design with Input and Output Logic Circuitry [1]

Line Based parallel QCA RAM-cell design offers bi-directional flow of data by moving the data back-forth *i.e*. processing-in-wire concept is utilized. Hence parallel memory-cell operation offers faster operation at the cost of reduced density.

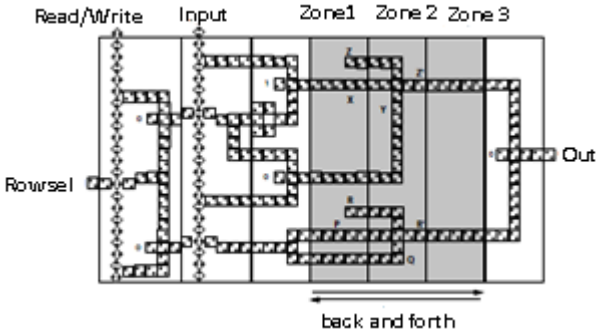

Figure 5. QCA Implementation of Line Based QCA RAM Cell Design Using Input-Output Control Logic Circuit [1]

B. Clocking and Timing

The design shown in Figure 3 requires total of three clocks which results in adiabatic switching is presented in Figure 6.Three zones of clock cycles [1] are used in which zone 2 clocks Signal has four equal Time-slots; whereas zone 1 and zone 3 have unequal clock time- slots as shown in Figure 5.

3. Serial Memory Architecture

A serial memory design is a loop based, which utilizes memory-in-motion paradigm with in a QCA loop. The memory design is Tile based meaning that the arrangement

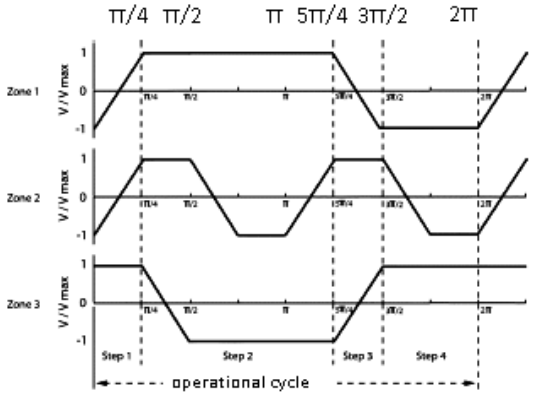

Figure 6. Three Clocking Zones [1]

QCA cells are in the form of QCA blocks. The QCA memory loop can be formed by connecting two horizontal lines of QCA cells from both ends which creates a loop[7]. These memory loops can be stacked so as to create highly dense as well as compact architecture.

A. Serial QCA Memory-Cell Design

The design shown in Figure 8 is a Loop based *i.e*. the loop in a memory-tile can store multiple bits at a time depending upon the number of clocking zone or clocking cycle. Corresponding clocking and timing scheme is shown in Figure 9.

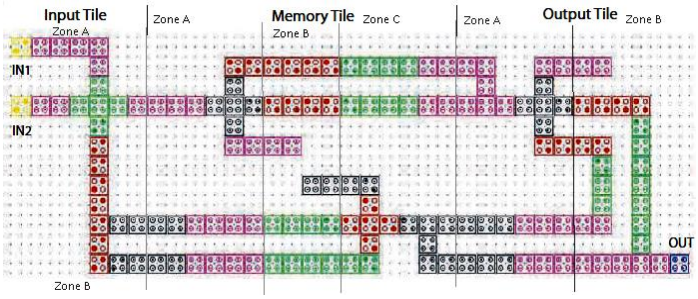

Figure 8. QCA Implementation of Loop Based QCA RAM Cell Design with Input-Output Control Logic Circuitry [7]

B. Clocking and Timing

Input-output tiles are in two clock cycle zones *i.e*. hold phase and switch phase where as the memory tile is in three clocking zones *i.e*. hold, relax and switch phases.

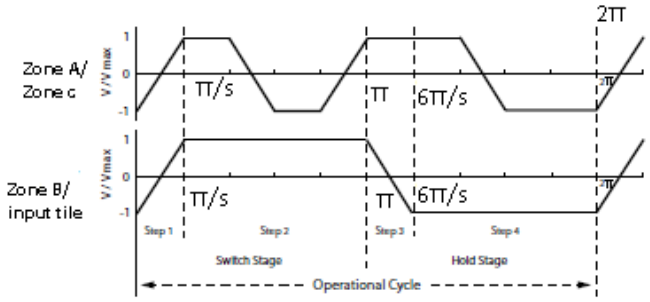

Figure 9. Clocking Zones for Serial Memory Design [7]

4. Surveyed Design

Taskin B *et al.* (2008) proposed a line based memory-cell design using six loic gates as shown in Figure 10.The design in based on Majority voter [2] which utilizes dual phase clocking scheme.

Gosh M. *et al.* (2015) designed a parallel memory cell Mux - based on 2 dot 1 QCA cell arrangement. The results show 86.11% accuracy with minimum number of QCA cells [3]. The design shown in Figure 12 is utilized for making n-bit memory architecture. Mux based parallel memory design using QCA cell is also presented in [13].

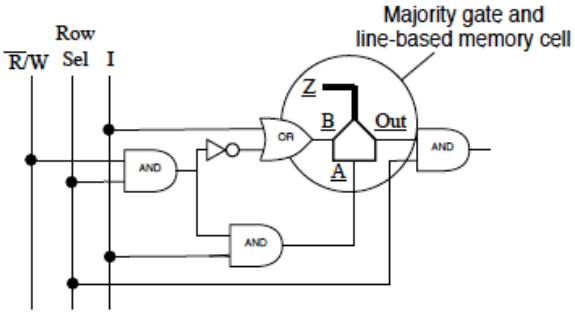

Figure 10. Line Based Memory-Cell Design [2]

QCA Implementation of Figure 10 is shown in Figure 11.

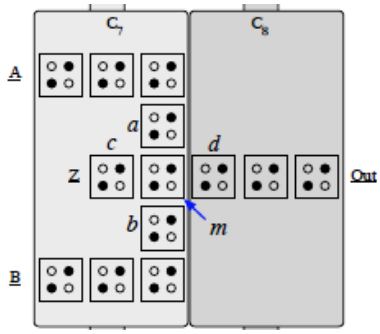

Figure 11. QCA Implementation of Figure 10 [2]

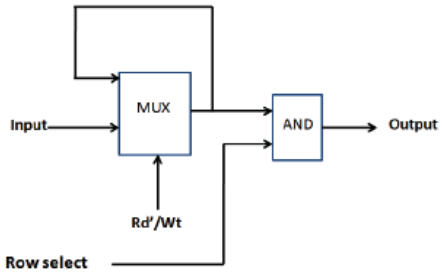

Figure 12. Mux Based Parallel 2 Dot 1 RAM-cell [3]

Walus K. *et al.* described a loop based RAM-cell design based on basic logic gates. Whenever the Write/Read logic pin is active high the data can be stored in a memory loop as shown in Figure 14.The proposed QCA design based on D-latch is much more complex because it contains 158 number of QCA cells as shown in Figure 15.

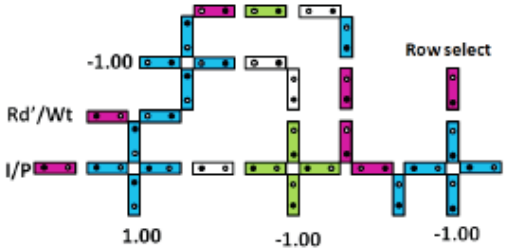

Figure 13. QCA Implementation [3] of Figure 12

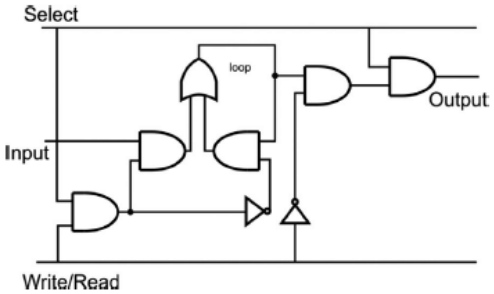

Figure 14. Schematic of Conventional RAM Cell [4]

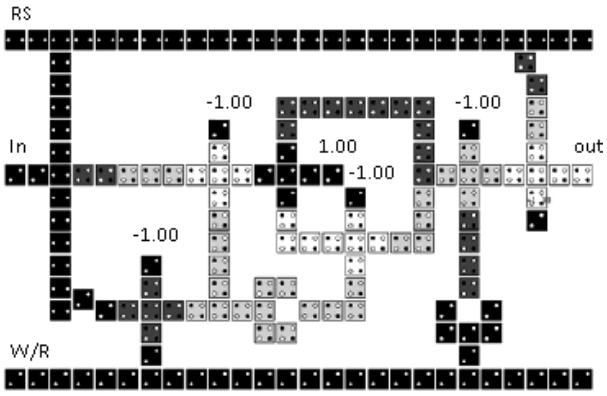

Figure 15. QCA Memory-cell Layout [4] of Figure 14

Dehkordi, M.A. *et al.* (2011) presented a SR flip flop based memory design [9] where data bits are stored in the RAM cell loop. The design utilizes less number of QCA cells with very small wasted area as shown in Figure 16 and its QCA implementation in Figure 17.

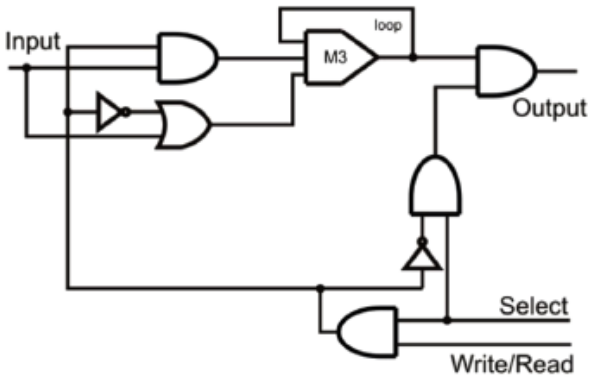

Figure 16. Majority Voter Based RAM Cell [9]

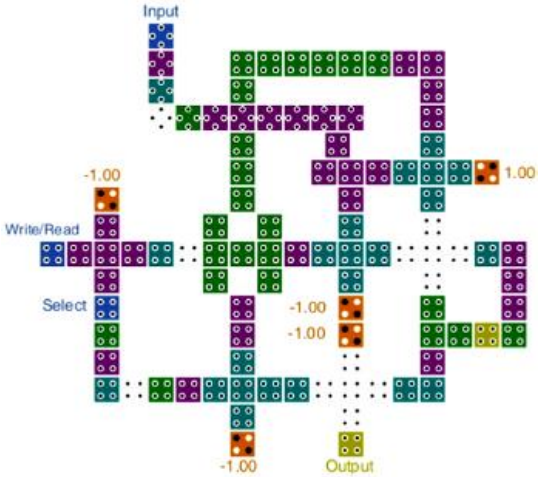

Figure 17. QCA Implementation [9] of Figure 17

Hashemi, S. *et al.* (2012) proposes a RAM cell with the Ability of SET-RESET feature utilizes only eight basic Gates without any coplanar wire crossings the design Occupies $0.13\mu m^2$ [10] is Shown in Figure 18 and Figure 19 shows its QCA implementation.

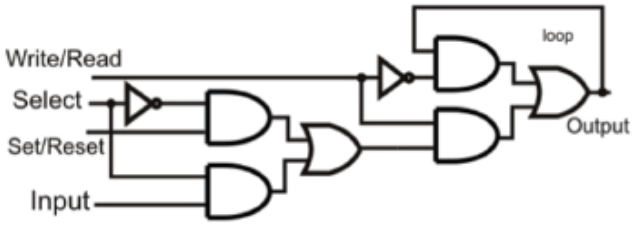

Figure 18. RAM Cell Structure [10]

Dehkordi, M.A. *et al.* (2011) presented a second memory – cell design with less number of gates as compared to the previous design shown in Figure 16, the second design shown in Figure 20 utilizes six logic gates. Hence reduces the complexity in terms of area of 0.07μm^2 with input to

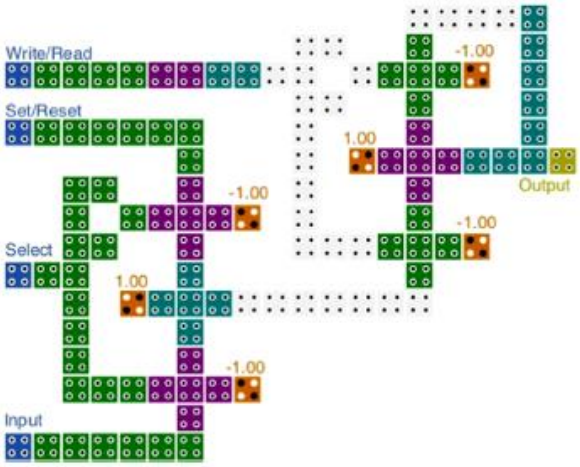

Figure 19. QCA Implementation [10] of Figure 18

Output delay of 2 clock cycles.QCA equivalent circuit is shown in Figure 21.

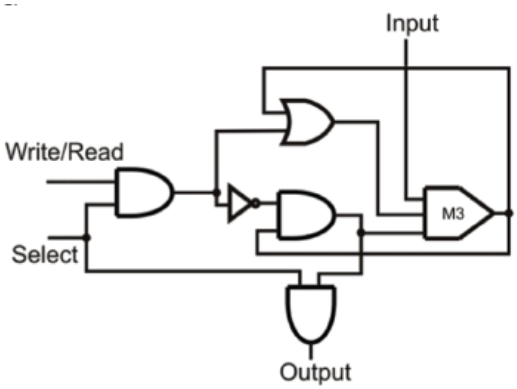

Figure 20. Second Memory-cell Design [9]

Angizi, S. *et al.* (2015) designed a five input majority-voter based memory-call design with 88 QCA cells, five logic gates and area of 0.08μm^2.The proposed design is very efficient, the number of clock cycles utilized by the design is 1.7.The Schematic circuit is shown in Figure 22 where as its QCA equivalent design is given in Figure 23.

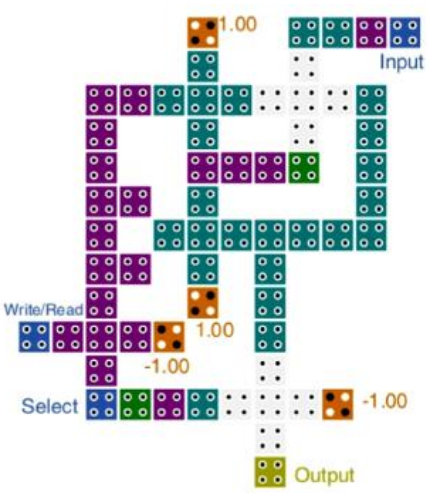

Figure 21. QCA Equivalent Design [9] of Figure 20

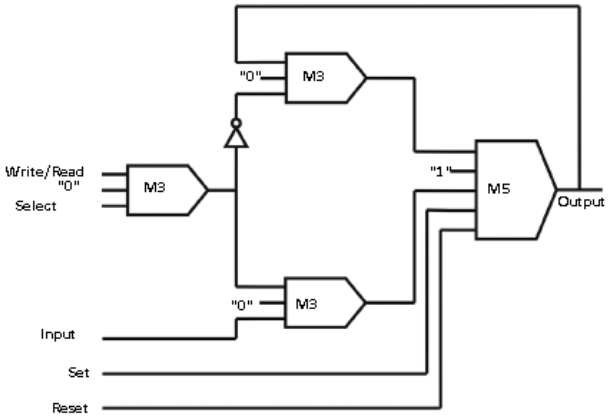

Figure22. Memory-cell Design with Majority-Voters [11]

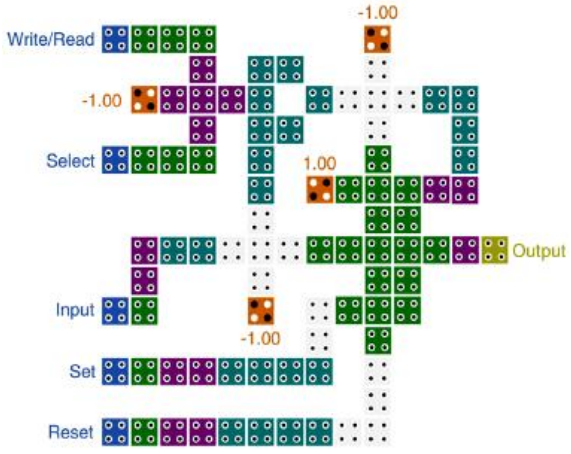

Figure 23. QCA Circuit of [11] Figure 22

5. Conclusion

Reconfiguration of memory circuits using Quantum Dot Cellular Automata will further improve the design in terms of power efficiency, read and write latency, area as well as cost. Table 1 presents a comparison of line based and loop based memory cell design.

Metrix	Parallel RAM cell design	Serial RAM cell design
Memory Density	Less density	More Density
No. of QCA cells required	More	Less
CMOS circuit complexity	High	Low
Write/Read circuit	Duplicating for each bit	Sharing of bits in a loop
Latency	Low	High

In parallel memory design, if clock signal duration will be different, we need time-to-space transformation by duplicating the circuit multiple times so as to form iterative logic array. In serial memory design, the clock time duration for all the four zones of semi-adiabatic switching must be different. Therefore more than one clock are required for serial memory design. An improved design which can take the advantage of both parallel as well as serial memory architecture can be designed which must be more efficient in terms of no. of clock cycles, read and write latency, cell counts and wasted area over the existing designs presented in this paper.

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