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A Novel Low Power and Low Voltage Bulk-Input Four-Quadrant Analog Multiplier in Voltage Mode

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Abstract

This paper presents a new CMOS four-quadrant low voltage and low power analog multiplier circuit in voltage mode. In the proposed analog multiplier, transistors are biased in weak inversion by driving them at bulk terminals. The proposed design has fully differential ended output. Input signal ranges are ±40mV and all transistors have the equal sizes. Simulation results have been presented by HSPICE simulator in 0.18µm standard CMOS technology to confirm the operation of the circuit. The results show that the proposed analog multiplier has several advantages in comparison with other analog multipliers.

Keywords: *analog multiplier, voltage mode, bulk-input CMOS circuits, four-quadrant, weak inversion*

1. Introduction

Analog multipliers are coming into account as essential and necessary circuit elements. Multiplier is a device having two analog inputs and one output. Output signal is the multiplied result of the inputs [1]. There is many different types of multipliers related to their input mode (currents [1-4] or voltages [5-8] or a mixture of them [9-10]) and the region of the operation (saturation [11-12, 4], linear [13, 5] and weak inversion [2, 7-8, 14]). Analog multiplication can be applied in many applications such as adaptive filters, frequency doublers, equalizer, modulators, automatic gain controlling, artificial neural networks [5, 15-17], image processing, medical treatments [9], in sensor applications [10] and fuzzy logic controllers. These days, the electronic society is faced with orders in relation to low power dissipations [3, 17].

Primary circuits were reported first in Gilbert works using BJT transistors [18]. Moreover, many works have been proposed including different types of four-quadrant multiplier circuits for low power applications even digital [19]. There are many modes for managing an analog multiplier according to multiplier types. In all these works a practical way for obtaining a low power dissipation topology is to use MOSFETs in weak inversion layer [2, 7-8, 14]. Another way is to drive them in bulk terminals [14]. As a result, we need an efficient structure for analog multiplier. Figure 1 shows a simple diagram of multiplication.

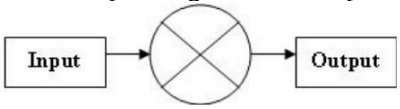

Figure 1. A Simple Diagram of Multiplication

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The main reason for choosing this structure is answering many desires that were not acceptable and available in many ones such as [12]. In [12], the most noticeable factor is the power consumption which is 32µW. However, this is considerable. The main reason for achieving these high levels power consumption is utilizing more transistors. For the same reason papers [2,4,20] and [21] have high power consumption.

The authors of [12] proposed a low power CMOS analog multiplier using 13 transistors. All of them have been driven in the linear region using 0.35μm CMOS technology. In [12], W/L is 0.8µm/0.35µm, input signals are X=0.5V, Y=1.5V and supply voltage is 1.5V, which is ten times bigger than V_{DD} in this design and finally the power consumption is 32µW. The power consumption in this paper is also high.

Gravati *et al.* [2] proposed a novel current mode very low power analog CMOS four-quadrant multiplier. The Gravati *et al.* analog multiplier [2] consist of 14 transistors. Moreover, they using 0.35µm technology. MOSFETs are in weak inversion region with 2V supply voltage and 250nA bias current. The maximum power consumption reported by Gravati *et al.* [2] is 5.5µW. Although the transistors work in weak inversion, but it is not in a very low power structure. It may have been caused due to large number of transistors and high level V_{DD} and I_{BIAS}.

Beyraghi *et al.* [4] proposed a current mode four-quadrant analog multiplier designed in 0.35µm CMOS Technology using 20 saturated transistors. The utilized supply voltage is ±1.5V and input current range is ±10µA. Aspect ratio of transistors are in different size. The reported power dissipation in [4] is 475µW. The main reasons for this power consumption could be large numbers of MOSFETs and high amount of supply voltage. Although the process number and driving region are also noticeable.

In [20], there is a design of four-quadrant analog multiplier consist of a multiplier cell. It has 12 transistors working in saturation. CMOS Technology is 0.5µm with W=1µm and L=2µm. The input range is 200mV for both inputs, supply voltage is 2.5V and bias current is 10nA. The power dissipation is not mentioned, but it is certainly clear that it is a high value, because of using high input ranges and many number of MOSFETs.

Popa [21] scrutinized two current mode multiplier topologies including 17 and 23 transistors. The process is 0.18µm CMOS technology with 1.2V supply voltage and 300µA range for inputs in saturation region. The simulation results for both circuits show the power consumption of 60µW and 75µW, respectively. The author has claimed the circuits use the small value of minimal supply voltage and the power consumption is extremely low, however it could be even lower.

In this paper, a CMOS low power four-quadrant analog multiplier has been presented with only 8 MOSFETs. The transistors are biased in weak inversion using 0.18µm CMOS Technology. Supply voltage is 0.15V and bias current equals to 10nA. The input ranges are ±40mV. We use differential inputs and we also have differential outputs. As effective inversion layer in pMOS devices increases by negative potential of n-type bulk with respect to p-type source, there would be an exponential relationship between drain to source current and bulk to source voltage. The proposed multiplier is simulated in HSPICE. The simulation results show that the power consumption in the proposed analog multiplier is 444.5pW.

The rest of this paper is organized as follows: Section 2 described circuit explanation. Section 3 presents the mismatch of the proposed multiplier. Simulation results are presented in Section 4. Finally, the paper is concluded in section 5.

2. Explanation of the Proposed Circuit

With respect to the operation of a MOS device in weak inversion, relative equations are as follows:

$$I_{DS} = I_{D0} e^{\frac{-V_{gs}}{\eta U_T}} e^{\frac{-(\eta-1)V_{bs}}{\eta U_T}} \left[1 - e^{\frac{-V_{ds}}{\eta U_T}}\right] \quad (1)$$

Eq. 1 is the drain to source current of MOS (ignoring the early effects VDS<<VE) [22, 23], where $I_{D0} = I_s e^{\frac{V_{TH}}{\eta U_T}}, I_s = 2\eta\beta U_T^2, U_T = \frac{KT}{q}\eta$ is the sub-threshold slope factor and is between 1 and 2 [22, 24], $\beta = \mu C_{ox}\frac{W}{L}V_E$, and V_E is the early voltage that is nearly 10 V.

As explained above, the devices must operate in weak inversion, below V_{TH}, and bulk has voltage, then V_{sb} has a considerable value [11], which is computed as follows:

$$V_{TH} = V_{TH0} + \gamma(\sqrt{|V_{SB} + \phi_0|} - \sqrt{|\phi_0|}) \quad (2)$$

In this equation $V_{TH} = V_{TH0}$ where $V_{sb} = 0$, $\phi_0 = 2\phi_F + \nabla\phi$, $\nabla\phi = 6U_T$, and γ is the body effect parameter that depends on the process and defines as follow: $\gamma = \frac{-\sqrt{2q\,\epsilon_{si}\,N_D}}{C'_{OX}}$.

The exponential function in this topology defines as a current mirror which is biased in bulk terminals and is shown in Figure 2.

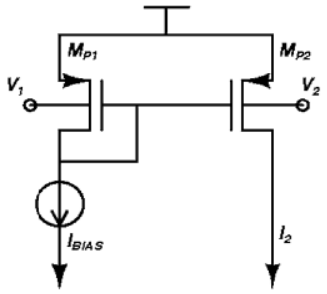

Figure 2. Exponential Circuit

The current equation for this circuit based on Eq. 1 can be written as follows:

$$I_{Ds1} = I_{D0} e^{\frac{-V_{gs1}}{\eta U_T}} e^{\frac{-(\eta-1)V_{bs1}}{\eta U_T}} \quad (3)$$

$$I_{Ds2} = I_{D0} e^{\frac{-V_{gs2}}{\eta U_T}} e^{\frac{-(\eta-1)V_{bs2}}{\eta U_T}} \quad (4)$$

$$I_{Ds2} = I_{BIAS} e^{\frac{-(\eta-1)(V_{bs2}-V_{bs1})}{\eta U_T}} \quad (5)$$

Where V_{sb2}, V_{sb1} are very small ($|V_{sb2}|, |V_{sb1}| \ll \frac{\eta U_T}{(\eta-1)}$, with $\eta = 1.2$, so $\frac{\eta U_T}{(\eta-1)} = 155mv$), the equations are as follows, which result in more dynamic range in comparison to multipliers with gate inputs.

$$I_{Ds2} = I_{BIAS} e^{\frac{-(\eta-1)V_{bs2}}{\eta U_T}} e^{\frac{(\eta-1)V_{bs1}}{\eta U_T}} \quad (6)$$

According to Taylor's series:

$$I_{Ds2} = I_{BIAS}[1 - (\frac{(\eta-1)V_{bs2}}{\eta U_T}) + \frac{1}{2!}\left(\frac{(\eta-1)V_{bs2}}{\eta U_T}\right)^2 - \cdots] \times [1 + (\frac{(\eta-1)V_{bs2}}{\eta U_T}) + \frac{1}{2!}\left(\frac{(\eta-1)V_{bs2}}{\eta U_T}\right)^2 + \cdots] \quad (7)$$

We can consider these two equations as equal ones if $|(\frac{(\eta-1)V_{bs2,1}}{\eta U_T})| \ll 1$.

For presenting four-quadrant multiplier, we need four circuits as shown in Figure 2. Figure 3 shows a four-quadrant multiplier architecture. It should be noted that $|V_{in2}|, |V_{in1}| \ll \frac{\eta U_T}{(\eta-1)}$.

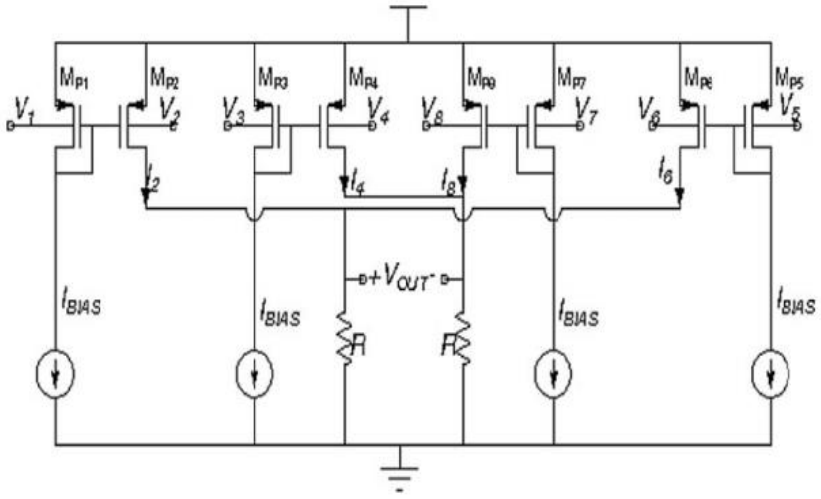

Figure 3. The Proposed Multiplier Topology

In Figure 3, assume V_{bs} of all eight pMOS devices are $V_1, V_2, V_3, V_4, V_5, V_6, V_7$ and V_8. The input voltages are $V_1 = V_7 = V_b + V_{in1}$, $V_2 = V_4 = V_b - V_{in2}$, $V_3 = V_5 = V_b - V_{in1}$, $and\ V_6 = V_8 = V_b + V_{in2}$.

So, the currents in each branch is as follows:

$$I_{Ds2} = I_{BIAS} e^{\frac{-(\eta-1)(V_2-V_1)}{\eta U_T}} = I_{BIAS} e^{\frac{(\eta-1)(V_{in2}+V_{in1})}{\eta U_T}} \quad (8)$$

In Eq. 8 we ignore the higher order terms to approach Eq. 9:

$$\cong I_{BIAS}[1 + (\frac{(\eta-1)V_{in2}}{\eta U_T}) + \frac{1}{2!}\left(\frac{(\eta-1)V_{in2}}{\eta U_T}\right)^2] \times [1 + (\frac{(\eta-1)V_{in1}}{\eta U_T}) + \frac{1}{2!}\left(\frac{(\eta-1)V_{in1}}{\eta U_T}\right)^2] \quad (9)$$

In the same way $I_{Ds4}, I_{Ds6}, I_{Ds8}$ defines as below:

$$I_{Ds4} = I_{BIAS}e^{\frac{-(\eta-1)(V_4-V_3)}{\eta U_T}} = I_{BIAS}e^{\frac{(\eta-1)(V_{in2}-V_{in1})}{\eta U_T}} \cong I_{BIAS}[1+(\frac{(\eta-1)V_{in2}}{\eta U_T})+ \frac{1}{2!}\left(\frac{(\eta-1)V_{in2}}{\eta U_T}\right)^2] \times [1-\left(\frac{(\eta-1)V_{in1}}{\eta U_T}\right)+\frac{1}{2!}\left(\frac{(\eta-1)V_{in1}}{\eta U_T}\right)^2] \quad (10)$$

$$\cong I_{BIAS}[1-(\frac{(\eta-1)V_{in2}}{\eta U_T})+\frac{1}{2!}\left(\frac{(\eta-1)V_{in2}}{\eta U_T}\right)^2] \times [1-(\frac{(\eta-1)V_{in1}}{\eta U_T})+\frac{1}{2!}\left(\frac{(\eta-1)V_{in1}}{\eta U_T}\right)^2] \quad (11)$$

$$I_{Ds4} = I_{BIAS}e^{\frac{-(\eta-1)(V_8-V_7)}{\eta U_T}} = I_{BIAS}e^{\frac{(\eta-1)(V_{in2}-V_{in1})}{\eta U_T}} \cong I_{BIAS}[1-(\frac{(\eta-1)V_{in2}}{\eta U_T})+\frac{1}{2!}\left(\frac{(\eta-1)V_{in2}}{\eta U_T}\right)^2] \times [1+ \left(\frac{(\eta-1)V_{in1}}{\eta U_T}\right)+\frac{1}{2!}\left(\frac{(\eta-1)V_{in1}}{\eta U_T}\right)^2 \quad (12)$$

In this topology for multiplication I_{out} defines as $I_{out} = (I_{Ds2}+I_{Ds2})-(I_{Ds4}+I_{Ds8})$ and output voltage is as follows:

$$V_{out} = I_{out} \times R = [(I_{DS2}+I_{DS6})-(I_{DS4}-I_{DS8})]R \quad (13)$$

So the output is as follows:

$$I_{out} \cong 4\left[\frac{(\eta-1)}{\eta U_T}\right]^2 V_{in2}V_{in1} \quad (14)$$

As explained above inputs are differential named V_{in1} and V_{in2}. In first quadrant V_1 is V_{in1} and V_2 is V_{in2}. In other three quadrants V_3, V_5 and V_7 are equal to V_{in1} and V_4, V_6 and V_8 are equal to V_{in2}, respectively.

3. Mismatch of the Proposed Multiplier

There would be some kind of mismatches between the devices because of the fabrication process, which is calculated by regarding to variations of process parameters and also the mismatch in the bias voltages or currents. The drain current may cause a mismatch due to I_{D0} including β mismatch (in weak inversion its effects can be neglected [24, 25]). Another factor, can be caused by V_{TH} that varies the current and the η due to bulk to source voltage, V_{BS}. For these mismatches we can consider a term as $I_{D0}(1+\Delta I_{D01})$ and bias mismatch can be considered as $I_{BIAS}+\Delta I_{BIAS}$. For each device in current mirror we assume another mismatch caused by V_{Ds} in output currents $(I_{DS2}, I_{DS4}, I_{DS6}, I_{DS8})$ which introduces the factor δ_{ij} where i and j refers to transistor pairs. So Eq. 1 can be rewrite as below:

$$I_{DS2} = I_{BIAS} \times \xi_{2,1} \times e^{-\frac{(\eta-1)V_{bs2,1}}{\eta U_T}} \times \delta_{2,1} \quad (15)$$

Where $\xi_{2,1} = \frac{(1+\Delta I_{D02})}{(1+\Delta I_{D01})}$ shows I_{D0} mismatch between M_{P1} and M_{P2} that their variations are , ΔI_{D02}, respectively, $V_{bs2,1} = V_{bs2} - V_{bs1}$ and $\delta_{2,1} = \left[1-e^{-\frac{V_{ds2}}{\eta U_T}}\right]/[1-e^{-\frac{V_{ds1}}{\eta U_T}}]$ is due to V_{ds} between the two pairs. As the inputs are applied to bulk terminals so $V_{bs} = V_{in}$ and it is better to have only a parameter for mismatch factors like ρ so finally the Eq. 15 rewrites as:

$$I_{DS2} = \rho_2 \times I_{BIAS} \times e^{\frac{(\eta-1)(V_{in2}+V_{in1})}{\eta U_T}} \quad (16)$$

And $\rho_2 = \xi_{2,1} \times \delta_{2,1}$. Like this expression will be considered for other current equations, then we have:

$$I_{DS4} = \rho_4 \times I_{BIAS} \times e^{\frac{(\eta-1)(V_{in2}-V_{in1})}{\eta U_T}} \quad (17)$$

$$I_{DS6} = \rho_6 \times I_{Bias} \times e^{\frac{-(\eta-1)(V_{in2}+V_{in1})}{\eta U_T}} \quad (18)$$

$$I_{DS8} = \rho_8 \times I_{Bias} \times e^{\frac{-(\eta-1)(V_{in2}-V_{in1})}{\eta U_T}} \quad (19)$$

With respect to Eq. 13 the summations are:

$$I_{DS2} + I_{DS6} = I_{Bias}(\rho + \Delta\rho_{2,6})\left[e^{\frac{(\eta-1)(V_{in2}+V_{in1})}{\eta U_T}} - e^{\frac{-(\eta-1)(V_{in2}+V_{in1})}{\eta U_T}}\right] \quad (20)$$

And

$$I_{DS4} - I_{DS8} = I_{Bias}(\rho + \Delta\rho_{4,8})\left[e^{\frac{(\eta-1)(V_{in2}-V_{in1})}{\eta U_T}} - e^{\frac{-(\eta-1)(V_{in2}-V_{in1})}{\eta U_T}}\right] \quad (21)$$

So final current equation presents as follows:

$$I_{out} \cong I_{Bias} \times \rho \times 4\left[\frac{(\eta-1)}{\eta U_T}\right]^2 V_{in2}V_{in1} + \lambda I_{Bias} \quad (22)$$

Where λ explains the mismatch due to multiplied part with $\Delta\rho$. The Eq. 22 shows the speculated expression for the mismatch process.

4. Simulation Results

For taking the performance of the proposed multiplier, we have used 0.18μm CMOS technology in threshold voltage of -0.443 v, two identical resistant 1MΩ, 0.15V supply voltage, 10nA I_{BIAS} (to bias the transistors in weak inversion), equal size of the transistors (W/L, 45 μm/2 μm) and bias voltage V_b is 100mV. For DC characteristics Vin1 and Vin2 vary from -100 to 100mV. Figure 4 shows the DC simulations I_{out}-$V_{in\ diff}$. Moreover, Differential input signals are shown in Figure 5. Table 1 shows the characteristic of the proposed multiplier. In Table 2, the results of the proposed analog multiplier are compared with other analog multipliers.

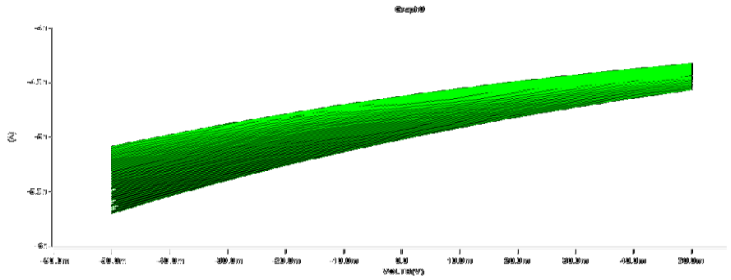

Figure 4. DC Characteristic I_{out}-$V_{in\ diff}$

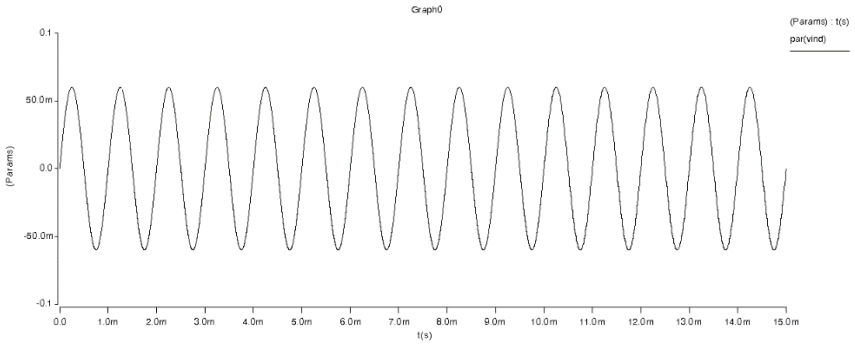

Figure 5. Differential Input Signals

Transient response of the proposed analog multiplier circuit is shown in Figure 6, when two sinusoidal signals of 40mV and 30mV, in 10 and 100 KHz are applied to the inputs.

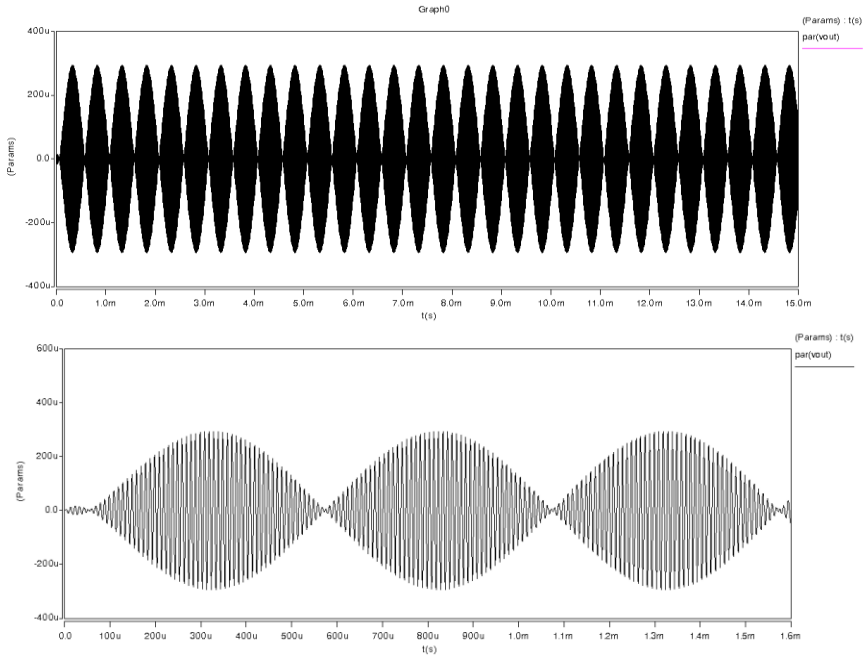

Figure 6. Transient Response of the Proposed Multiplier

Table 1. Results of this Work

Parameters	Result
V_{DD}	0.15 [V]
V_b	100 [mV]
I_{BIAS}	10 [nA]
Input dynamic range	Vin1 30 [mV], Vin2 40 [mV]
POWER	444.5 [pW]
Process used	0.18 [μm] CMOS

Table 2. Comparison of Performance

Parameters	This paper	[15]	[25]	[6]
Process	0.18 [μm]	0.35 [μm]	0.18 [μm]	0.35 [μm]
VDD	0.15 [V]	3.3 [V]	0.5 [V]	1.5 [V]
Vb	100 [mV]	NA	400 [mV]	NA
IBIAS	10 [nA]	10 [μA]	300 [nA]	NA
Input range	±40 [mV]	±NA]	±80 [mV]	±120 [mV]
Power	444.5 [pW]	0.34 [mW]	714.3 [nW]	6.7 [μW]

Table 2 performs a comparison between this paper and 3 other works. The circuit has used 0.18μm CMOS Technology. Based on our simulation results which are shown in Table 2, all parameters in this work are lower than the other ones. So the power consumption obviously will be in a lower range too. Power consumption are 0.34mW, 6.7μW and 714.3nW for [15], [6] and [25] respectively, but 444.5pW relates to this work.

5. Conclusion

A CMOS four-quadrant voltage mode analog multiplier circuit is presented which operates in weak inversion by driving it at bulk terminals. It is suitable for low power and low voltage applications as its power dissipation is 444.5pw. However the mismatch reduces its speed and output voltage range is very low. Circuit is designed in 0.18μm and the performance was simulated using HSPICE.

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