International Journal of Multimedia and Ubiquitous Engineering
Vol.10, No.9 (2015), pp.255-262
http://dx.doi.org/10.14257/ijmue.2015.10.9.26

Design of ATA Interface Hard Disk Memory Card Used in Video Image Data

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Abstract

In order to realize the current requirements of video image data memory card such as low power consumption, high storage density, high reading/writing speed, and enhancing the storage medium compatibility with improving the storage capacity and stability at the same time, we suggested a design of Video image data memory card using ATA interface hard-disk, and we use modularized design in this program, consists four parts: the image data buffer module, ATA logic module, ATA interface module, host communication module. Wherein the image data buffer module selects the CPLD plus external FIFO to complete makes the system only need to modify the CPLD program while working together with different external devices, which can improve the reliability and maintainability of the memory card that we designed. The functions of ATA logic module and ATA interface module are realized based on FPGA. The host communication module is completed by the AVR chips with TUSB6250 chip, ensuring the memory card has the advantages of low power consumption, internal short circuit protection and so on. In this paper, the proposed memory card scheme has the superiority such as lower cost, better compatibility, easy to expand, especially suitable for huge amounts of data in video store.

Keywords: *Video image data ATA interface Data memory card FPGA*

1. Introduction

At present, the video surveillance technology is developing toward the direction of digital, high definition, intelligent, network. As to the desire to improve the image quality requirements, the increase of video monitoring circuit, and other factors, the video surveillance system will need higher request in system capacity, security, and storage devices have become a key factor in the future development of video surveillance systems. The direction of data storage technology development is to improve the storage capacity and stability, enhanced compatibility of storage media to meet the application process for low power consumption, high reliability, high storage density, high reading/writing speed.

ATA (Advanced Technology Attachment) interface is developed by Compaq, Western Digital and other companies together in 1986, and is a interface using a 40-pin cable to connect with the main board. Through continuous development from birth, ATA protocol produced a total of 7 versions. ATA-7 is the latest version of the current ATA interface, whose interface rate is up to 133M/s, also known as ATA133, is the first ATA hard disk in interface speed over 100MB/s. At present, only the Maxtor Corporation uses ATA133 standard to produce a series of hard disk [1-2].

Most of the current domestic surveillance storage format uses a simplified H.264 or MPEG4 format, when the image quality is the CIF format level, the hard disk consumption rate is about 100M/road/hour.According to each data memory car\d corresponding to a piece of hard disk by some calculations, using basic megapixels

ISSN: 1975-0080 IJMUE

camera with 720P collected as a standard, normal video about an hour requires of hard drive capacity for 4G ~ 8G, video monitoring data through data compression also require storage space 3G per hour. One road video saved 30 days required capacity 3 GB * 24 * 30 = 2160GB (about 2Tb).

Image storage amount is mainly related to the resolution, for example, in the VGA (640*480) resolution, the data flow per second is: 640*480*30=9216000= 9 MB, when transferred to a computer by the USB port it is about 7Mb / sec. This system uses array CCD, which is frequently used as the image acquisition terminal, as an example for the calculation. The camera's line cycle or frame cycle will vary different work conditions, but the pixel clock cycle will not change, and in the design the data transfer rate is calculate according to the pixel clock cycle. The calculated data transmission rate is actually burst transmission rate, and continuous transmission rate is smaller than this value, and the burst transfer rate affects the size of the buffer.

At present, the development direction of current data storage technology is to reduce power consumption, improve reliability, increase storage density, improve reading/writing speed, at the same time to increase the storage capacity and stability and enhance the compatibility of the storage medium. High-end storage systems such as the SAN system, is mainly to meet the needs of large users of financial, telecommunications and other storage systems, while NAS and DAS storage systems can't meet the using demand of small image data acquisition system because of high cost. Therefore, the technology based on hard disk storage at the lowest price for mass storage requirements provides a feasible solution. This paper uses FPGA to realize the design scheme of ATA interface hard disk storage card, and the scheme can be used can be used to store vast amounts of video data [3].

2. Design Scheme of Memory Card

Data memory card includes image data buffer module, ATA logic module, ATA interface module, USB module. As the core control device of the system, it complete the equipment self-checking and the communication with the host. The data acquisition card uses the PIO (mainly for the transmission of commands, defining the label and writing file information) to communicate with ATA hard disk, when the system is expanded, the added image storage card memory card is detected and governed by the earliest memory one, and different memory cards communicate each other by I^2C. The design uses a rapid mode whose bus transfer rate reaches 400kbit/s, to meet the system self-checking and the transmission of control commands between different sectors [4-5].

The design scheme of data memory card is shown in Figure 1, using modularized design. It consists four parts: the image data buffer module, ATA logic module, ATA interface module, host communication module.

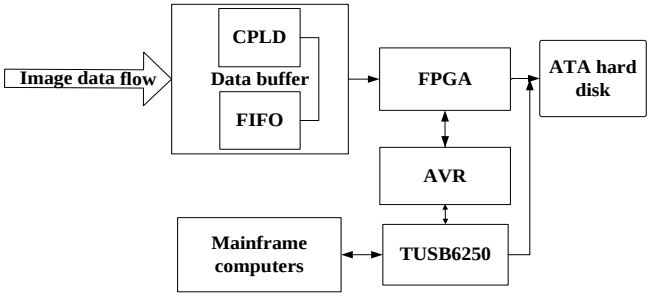

Figure 1. Composition of Image Data Memory Card

3. The Data Buffer Module

In this design, the data buffer module needs to solve the problems of the data splicing and the hard drive transmission delay in monitoring camera interface. FIFO (first in first out) chip is usually used to cache data, and accommodate the asynchronous signal frequency or phase difference. In the embedded system development, although the FIFO module is often integrated in the main control chip, but the programmable logic devices including internal mass storage resources are very expensive, considering the general problem of equipment, therefore, we use a combination of CPLD plus external FIFO to accomplish this function, so that you only need to modify the CPLD program when the system work together with the different external devices, which reflects the unity of design principle and improves the reliability and maintainability. The design of external FIFO circuit is shown in Figure 2, image data is written by the CPLD, and read by the FPGA, which realize data buffer between the different controllers.

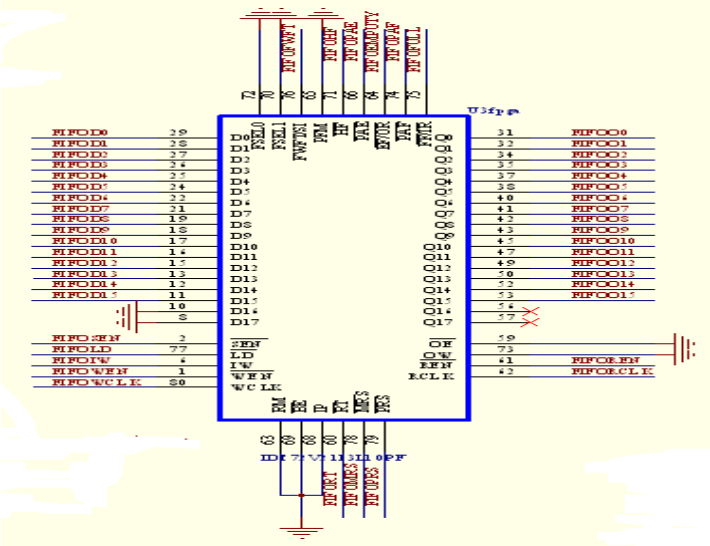

Figure 2. External FIFO Circuit

The design of CPLD circuit is shown in Figure 3, the data buffer module of data memory card adopts CPLD of XC95144XL type, and its main features are:

- 5 ns pin-to-pin logic delays
- System frequency up to 178 MHz
- 144 macrocells with 3,200 usable gates: each macrocell can work in power-saving mode
- up to 144 user I / O pins ,
- ISP in-system programmable technology: Endurance exceeding 10,000 program/erase cycles

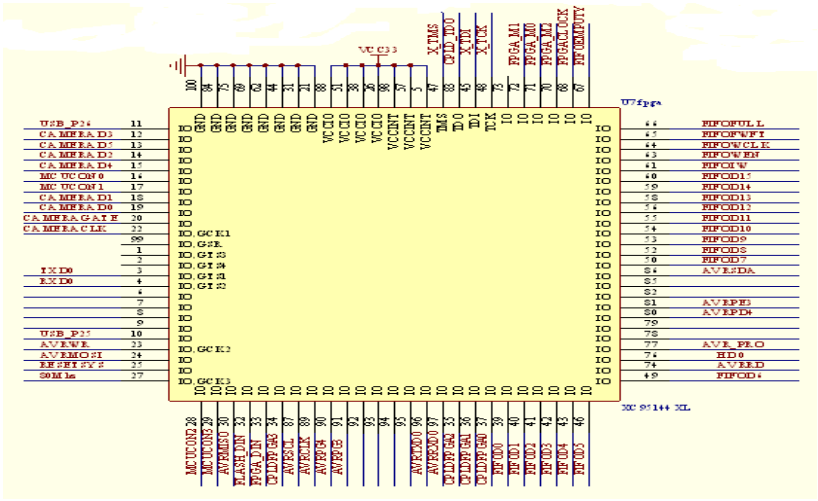

Figure 3. CPLD Circuit

Due to the flexibility of programmable logic devices, CPLD can integrate a variety of input image data operations to improve the efficiency of hard disk storage, including a data combination method as shown in Figure 4.

In order to guarantee the strict timing relationships of image data, we need to latch processing first, and use four bit 4 shift register respectively according to different cameras, considering the temporal relations, the output of the shift register is launched by 16 bit data register, and then written to the FIFO [6].

4. ATA Interface Logic Module

4.1. Working Principle and Circuit of ATA Interface Logic Module

The function of ATA interface logic module is to implement the conversion of the control signal and data from main controller into the ATA standard time sequence, send the data to the ATA bus, sample the ATA bus signal simultaneously, and after synchronization, caching, the signal is transmitted into the internal controller modules and establish the ATA data transmission channel, and control the reading/writing timing of hard dist which is complicated by the FPGA [7].

ATA interface in the system is connected to the onboard FPGA, and FPGA carries interface logic control on the hard disk, providing reading/writing timing, and CRC check. ATA data channel is composed of CRC checksum and data buffer, the selection of data is determined by the ATA interface logic. FIFO reading interface logic and ATA interface logic is driven by control signal from AVR controller and the clock signal, and is capable to form ATA interface error information into the status word to send to the AVR controller.

As the role of a central controller, AVR controller completes the bottom scheduling task of various equipments including the hard disk detection, electronic identification and hard disk controlling. I^2C communication between various data storage card is also established by the AVR controller.

In the ATA interface modules, AVR controller detects the status of hard dist, and provides FPGA with the PIO mode command of hard disk to control the state of reading and writing to the disk. Meanwhile AVR controller also provides the FPGA with FIFO read timing , and CPLD write timing to complete the rigorous combination of FIFO asynchronous reading and writing. At the same time in the host computer communication module, AVR control chip also plays a central role in the control, which will be described in the host communication module session. ATA interface circuit is shown in Figure 4 [8].

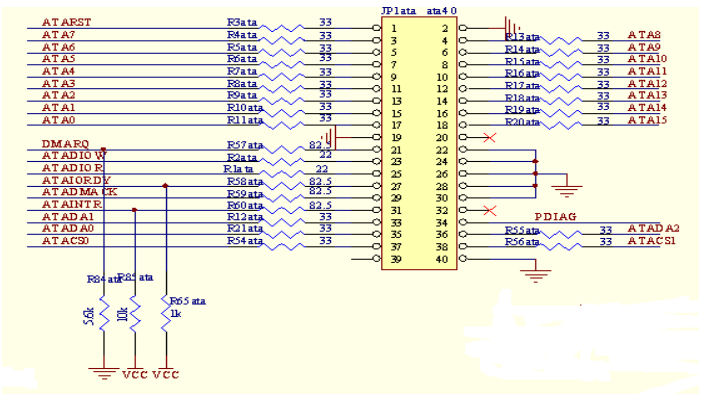

Figure 4. ATA Interface Circuit

4.2. FPGA Design of Data Memory Card

In the design ATA logic module FPGA reads data from the data buffer module FIFO and build it on ATA hard disk data channels. ATA data channel is composed of CRC checksum and data buffer (create two data buffer within the FPGA), and data selection is determined by the ATA interface logic, FPGA generate UDMA timing logic.

4.2.1. Structure and Function of the FPGA

The FPGA is Field Programmable Gate Array (FPGA), it is subsequent development product of the programmable logic devices such as the PAL and EPLD. It is rich in logical units, and overcome the problem of limited number of the original programmable gate device. As a half custom of integrated circuit products in application-specific circuits, it also solves the problem of the inflexible application of the custom circuit.

The FPGA chip is based on look-up table technology, but its concept and performance is beyond the limitation of original technology, general also is integrated the common function of hardcore module, such as block RAM, clock management and DSP.

The FPGA chip is mainly composed of six parts: the I/O unit, the basic logic unit, clock management, internal RAM, wiring resources, inline function module and embedded special hardcore.

On the FPGA programming development, we use the programming tool in the development of EDA environment. With the programming language, the design of the internally hardware circuit of the FPGA chip is described. The design process of the FPGA is as follows: first of all, the function of the circuit is designed. Then the design process, the design of integrated process and the implementation process are finished. After the completion of the above several works, the overall layout of and wiring of the circuit are carried. Finally, the device is programmed.

In the development process of FPGA, every step is need for validation. The main means of validation include the time series analysis, simulation and upper debugging, *etc*. In order to verify the correctness of the design, find problems as early as possible to ensure the smooth progress of the follow-up design. We will verify each step in the above several kinds of work at the same time.

The FPGA hardware design logic schematics of ATA logic can be seen in Figure 5.

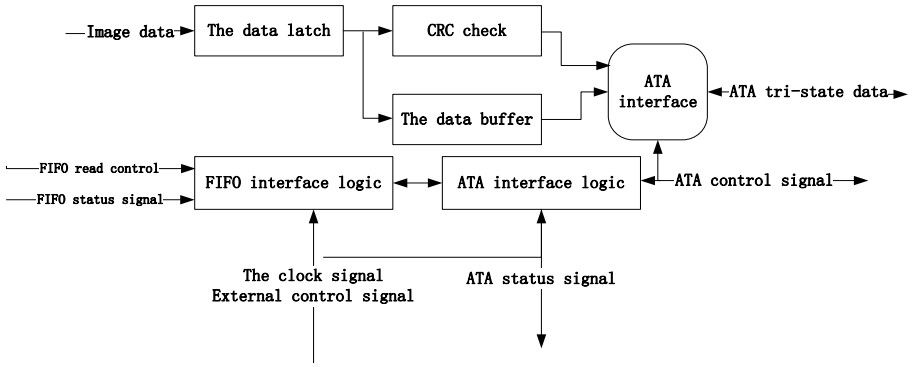

Figure 5. FPGA Hardware Design Logic Schematics of ATA Logic

4.2.2. FPGA Design of Data Memory Card

The ATA interface logic module defines the system register combination according to the ATA-6 protocol standard, and the interface signal on the basis of the ATA physical interface function. It keeps communication with the control module of ATA hard disk, and receives instruction and associated parameters sent from the host, then transmits them to the control module of ATA hard disk effectively and timely. It also can feedback status information from hard disk storage process to the status register in time, waiting for the master query. ATA interface logic module is implemented using VHDL language. The FPGA implementation of ATA logic module circuit is shown in Figure 6 [9].

In the part of standard interface we define the standard of the ATA interface signals. These signals have: address CS0, CS1, DA, data bus signal DD, reading/writing control signal DIOW, DMACK, DIOR, DMARQ, *etc*. According to different signal addressing of interface address we design the registers, DIOR and DIOW signals is used to control the direction of ATA hard disk reading/writing.

When the system is powered on, FPGA internal register group are initialized firstly. When the reset signal is detected by the main control chip FPGA at the same time, ATA hard disk operates the reset operation. After the end above two processes, the FPGA is idle. In the idle state, FPGA waits for the host command. When the main control chip detects the command from the host, the FPGA begin to command register writing command. When the master write these commands into a set of registers, the main control chip FPGA will host BSY bits, and begin to communicate with ATA hard disk, forward command register in the register to ATA hard disk, and judge that these commands is a data command or countless. According to the indifference commands, FPGA enters the appropriate command process.

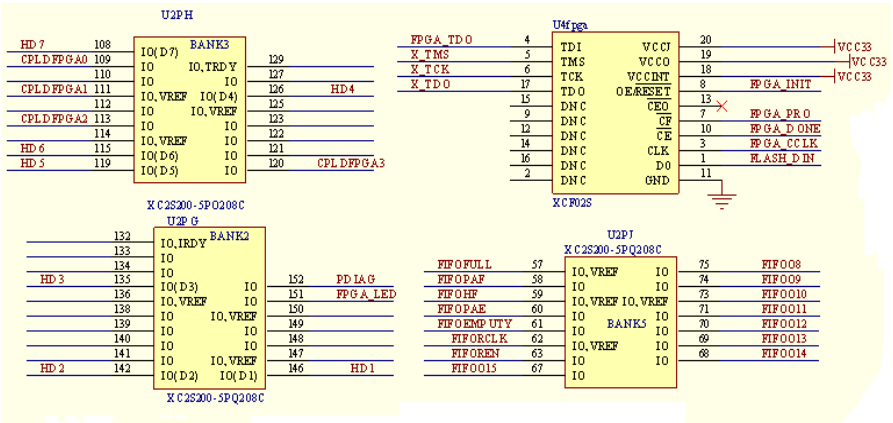

Figure 6. ATA Logic Module Circuit in FPGA

5. Host Communication Module

The host communication module is mainly used to complete the function of data transfer and human–computer interaction, namely to be able to read the data stored in the hard disk and send it to the host through the USB data interface, in order to handle the human-computer interaction function of data. This module is composed of AVR chip with the TUSB6250 chip to complete. The circuit design is shown in Figure 7.

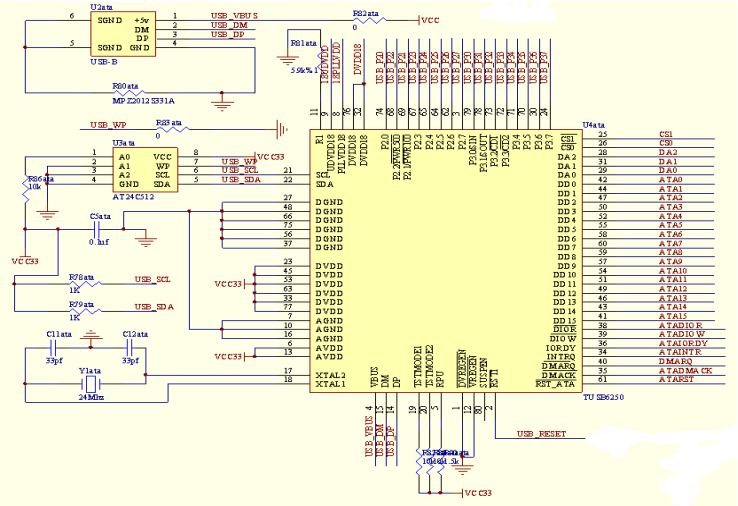

Figure7. Circuit of Communication Module

The TUSB6250 is designed by Texas Instruments to be a solution of a USB 2.0 to ATA/ATAPI bridge with low-power and high-speed. It is simple to use with no external components and low power consumption, and it has internal short circuit protection. Because of its internal integration with ATA hard disk interface, so we select the TUSB6250 to complete the communication with PC [10].

The TUSB6250 on the data acquisition card also acts as a master device of the whole equipment, the host computer accesses ATA hard drive via USB, and TUSB6250 is used as the data read-back channel of main hard dist, which supports USB2.0 high speed (480Mbps) mode. At this point, the TUSB6250 and FPGA together share ATA hard disk, and ATA hard disk works in UDMA66 mode.

6. Conclusion

We design the data memory card in video surveillance system in detail, and describe the relevant standard of ATA interface, the characteristics of the programmable logic devices, the concrete development process, and each module inside the data acquisition card, using CPLD and external FIFO to complete Combination of bytes before the data is written to the hard disk to achieve the image data buffer. The FPGA is also used to realize two kinds of working mode for ATA hard disk of PIO and UDMA, and we can use USB2.0 interface to realize the image data to read back.

Acknowledgment

The authors would like to thank for the developers of the shearlet toolbox and wavelet toolbox. This work is supported by Jilin Province Science and Technology Department (No. 201215107) and Jilin Province Education Department (No. 2013264).

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