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OPT-VCG: A Novel Proposal for 3D SoC Test Optimization

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Abstract

As an emerging technology for on-chip interconnect scaling in vertical direction in semiconductor industry, through-silicon-via (TSV) demonstrates its advantages and has been adopted for 3D SoC implementation. Optimal test architecture and test scheduling are significant for stacked 3D SoC design. However existing design methods cannot achieve both optimal test time and individual rationality. In this paper, game theory based 3D SoC test architecture optimization and test scheduling method is proposed under constraints of the available number of TSVs for test time minimization and rational test band width allocation. VCG algorithm is brought to 3D SoC design. Three kinds of stacked SoCs are built using ITC'02 SoC test benchmarks, and experimental results on them show the advantages of the proposed method over prior work.

Keywords: *through-silicon-via (TSV), 3D SoC, test optimization, test scheduling, game theory, VCG*

1. Introduction

The rapid development of DSM technology paves a way for semiconductor industry to manufacture high performance and low cost electronic devices. As a solution to SoCs interconnect scaling, to integrate of different circuit modules in vertical direction, through-silicon-via (TSV) emerges as the most popular technology for stacked IC and achieves competitive advantages, thus making it possible to substitute traditional 2D SoC with 3D SoC. It is predicted that 3D SoC will take the lead for complicated SoC design in the following decade. 3D SoC meets the requirements of system performance, heterogeneous structure, small footprint and costs *etc.,* [1]. However TSV-centered 3D SoC brings about new challenges for EDA technology such test structure optimization and test scheduling [2].

Embedded cores are widely used in 3D SoC for shortened product development cycle and enhanced development efficiency. Nevertheless, embedded cores cannot be accessed through I/O of SoC by nature, thus requiring special access mechanism. And Test Access Mechanism (TAM) for 3D SoC is much more complicated than that for 2D, *e.g.,* 3D TAM should support testing individual dies as well as testing partial and complete stacked SoC.

Therefore TAM should be incorporated on the dies for data transportation between cores and stack I/O pins. Test stimuli (test response) from (to) test resource (test sink) are delivered via TAM. Test wrapper serves as infrastructure for TAM during the process of data transportation. Therefore the design for test wrapper optimization and test scheduling has impact on the quality of test and determines test time and test costs for 3D SoC.

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2. Related Works

Recent research work about 3D SoC includes heuristics of test wrapper design for cores [3], whereas test access mechanism is not mentioned. In [4], ILP model is proposed for test structure design. These methods didn't consider constraints related to 3D SoC test such as the number of TSVs, and the assumption made for test costs reduction is not feasible: TAM can start and end at any layer [5].

3D SoC can be implemented using soft dies, hard dies or firm dies. For a given hard die, the test structure on it is fixed, thus test time is known. The only structure the designers can control is 3D TAM. For firm dies, the test pins and available maximized number of TSVs for the bottom die are known. The 2D TAM structure including the total number of cores under test (CUT), and test vectors and test band width are given, the designers need to make an optimum design and test scheduling method, band width for serial/parallel conversion for test length minimization under constraints of TSVs without exceeding the allowed upper bound. Soft dies are far more complicated than the other two, in order for test time minimization, extra variable and constraints should be taken into account. However this limits the number of dies that can be incorporated in the model in return. For the previous three types of SoC, Noia applies Linear Planning optimum solution, and test length is reduced greatly, and it is found out that increase in the number of test pins leads to test time reduction by increasing the usage rate for test pins [6]. Noia proves that for large complicated stacked SoC, the test time for dies on lower layers is relatively less, which is self-evident, because the cores from all levels have to transport test data via the test pins on the lowest level, the closer it is from the bottom layer, the less test time it takes.

3D SoC test comprises of pre-bound test and post-bound test. For pre-bound test, each die is tested separately, while for the latter, the stacked 3D SoC system is tested as a whole.

In [7], Li Jiang proposes a layout-driven test-architecture design and optimization technique under constraint of pin-count for pre-bond test of 3D SoC. The proposed test-architecture reduces the routing cost for test-access mechanisms, and thermal aware test scheduling algorithm is proposed to eliminate hot spots during manufacturing test.

In [8], die level test wrapper and related 3D test structure is proposed for pre-bound and post-bound test. This approach is practical, however test scheduling is not considered. This paper does not consider pre-bound test, the readers are referred to [9] for TAM optimization for pre-bound and post-bound test for test time minimization.

For stacked IC, the test pins are set on the lowest level close to package for post-bound test, while TSV influences the test band width when accessing cores of higher level. TSVs account for the area on chip, and are mainly used for functional interconnection including power/ground routing, clock routing *etc.,* Hence it is necessary design test access infrastructure to make full use of the few TSVs.

This paper explores test structure optimization for stacked SoC, especially made from soft dies and hard dies and tempts to study the effects of the number of available test pins, TSVs, the sequence of testing CUT on TAM optimization and test scheduling.

3. Problem Definition

3.1. Test Architecture for Stacked SoC

Supposing that test bus model is taken for TAM design. Generally speaking, 3D SoC can be embedded 2-8 dies [6]. And dies on the lowest level connect I/O directly. Dies from other levels need to transfer data via TAM from dies of all the lower levels through I/O of the lowest levels. In order to test all the cores from all the dies in the whole stacked SoC, TAM

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must guarantee any part of 3D SoC can be tested through pins of the lowest level. The total number of test pins and TSVs influences test time. Considering a SoC with three layers of dies, *e.g.,* D_0, D_1 and D_2. Let test time for them be 300, 600 and 800 clock cycles respectively. The total number of test pins on the lowest layer is 110 clock cycles, and the corresponding test band width for D_0, D_1 and D_2 is 30, 25 and 20 accordingly. Here only stacked SoC made of soft dies is taken for an example. Dies of three layers construct stacked SoC shown as Figure 1.

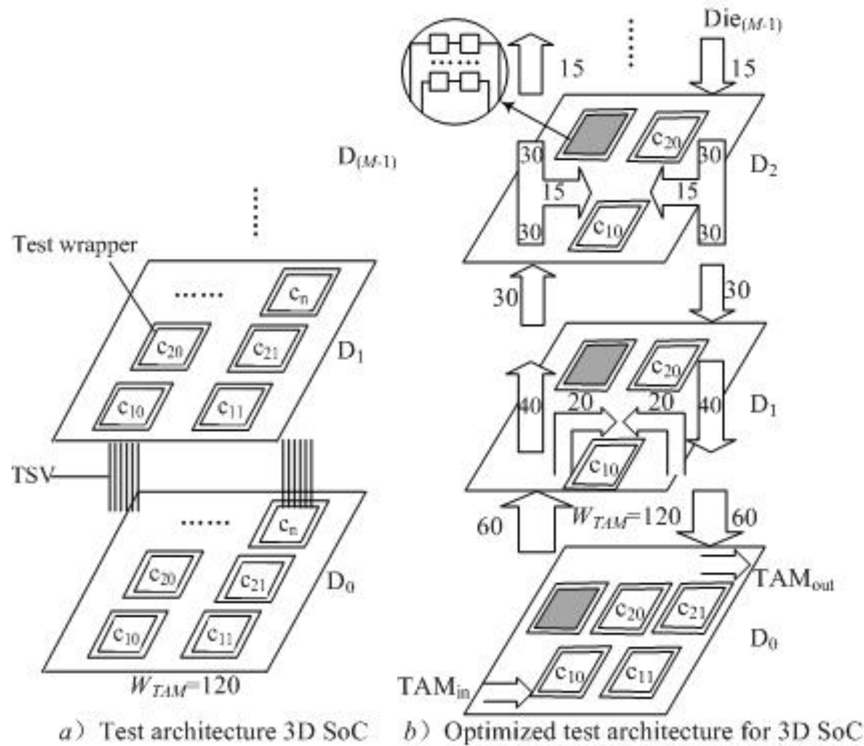

Figure 1. Illustration for 3D SoC Test Architecture of Soft Dies

In Figure a), Die D_0 is at the lowest layer, and the number of test pins is 120, dies of other layers connect next layers via TSV and finally exchange data through the port of I/O on the lowest layer. The test pins for them are 80, 40, 30 respectively.

It can be seen from Figure 1 b) that test band width for D_0 is 40 (test pins required is 80), test band width for D_1 is 20 (test pins 40), and D_1 is tested in parallel with D_0, each die uses its own test band width and TSVs, while test band width for D_2 is 15 (30 test pins), D_2 is tested in serial with Die_1, they share test band width and TSVs. It can be inferred that total test time for this stacked SoC is 1400 clock cycles (max {300,600} + 800).

3.2. Test Architecture Optimization for 3D SoC

Figure 2 shows 3D SoC with 5 CUTs, each CUT is surrounded by test wrappers for testability. Test wrapper is a testable logic which connects TAM and CUT. Each embedded core consists of a couple of function I/O and internal scan chains. The number of test wrapper scan chains equals the test band width.

The stacked SoC has two layers, three cores are mounted in $Layer_0$, and the other two cores are embedded into $layer_1$. Assuming that $2w$ channels are available, hence test band width is

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w. During the process of test, test data from ATE is transported to CUT via TAM with band width being *w*, when test finishes, test response is collected via another *w* channels via TAM. For a given test access architecture, the available number of TSVs is known. The objective of TAM design is minimizing test application time, and allocating test band width to different TAM.

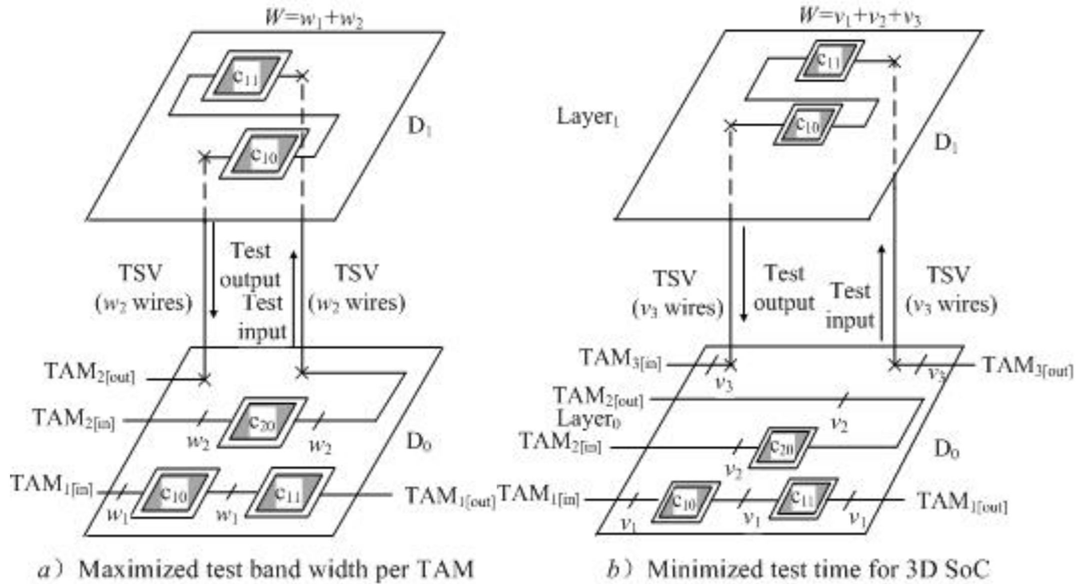

Figure 2 Illustration for Test Architecture Optimization

Figure 2 shows two different designs for the two-layered stacked SoCs. In Figure 2*a*), test band width is $W=w_1+w_2$, c_{10} and c_{11} in layer1 have to be tested via TSV, subject to test constraints $2w_2 \le n$ (n denotes the number of available TSVs), while for Figure 2*b*), CUT c_{10} and c_{11} use specific test channel subject to test constraints $2v_3 \le n$. It can be inferred that in 2*a*), test band width for each TAM is maximum, however all the CUTs have to be tested sequentially via the same test channel, in 2*b*), two cores in $layer_1$ share the specific test channel thus saving test time. In practice, designers aim at determining a scheme and allocating test band width to test channel rationally under constraints of the number of available TSVs for test time optimization.

4. 3D SoC Test Optimization Model

4.1. Problem Formulation

Originally game theory was proposed by von Neumann and Nash [10], Game theory is a study of conflict and cooperation between rational decision-makers. A game has the following elements: players, information, actions and payoffs, where the actions are available to each player at each decision point. If some strategies are employed to the game, and no player can profit by unilaterally changing its strategy, then equilibrium to the game can be achieved.

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4.2. 3D SoC Test Architecture Optimization

4.2.1. 3D SoC Band Width Allocation

For a given 3D SoC, the target is allocating test band width to each TAM for test architecture optimization. Increasing test band width purely will reduce test application time at the expense of increase in test pins. They both are contradictive, while game theory can help to find the equilibrium. Allocate the same test band width to each die at first, and then increase or decrease the number of test pins for corresponding 2D SoC and 3D SoC under constraints of test band width as well as the number of TSVs in order to find a win-win result, *e.g.,* the number of test pins maximized, when no less test application time can be obtained ever, or the Nash Equilibrium point can be found which does not satisfy test constraints.

4.2.2. 3D SoC Test Scheduling

This paper explores 3D SoC of five levels made of hard dies and soft dies shown as Figure 3. As mentioned before, for 3D SoC made of hard dies, the test architecture and test time for each die are known, and the only thing that the designer can do is to determine which die can be tested with some die in parallel for test time minimization.

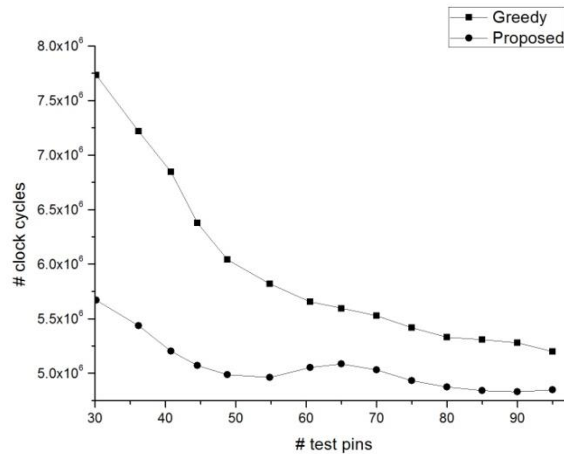

Figure 3. Test Time Comparisons on 3D SoC2 of Hard Die

Game theory can help to obtain such a point resulting in test time increase in some individual die and the total test time is minimized on the whole. For the latter, the number of modules on each die from 3D SoC, scan chains, the length of scan chain and the available test pins and the test band width are given.

3D SoC test architecture can be taken as a game, while the two elements: test time and test band are the two players, using game theory to find equilibrium between them is our target. In this paper, VCG algorithm [10] of game theory is introduced for equilibrium between test bandwidth and test time.

For a given 3D SoC, its total payoff is the function of user's test band width and test time:

$3DSoC=U_i-\Sigma_i Cost_i$

Where U_i is the service efficiency that node *i* gets, $Cost_i$ is the service costs for node *j*. An ideal band width allocation algorithm should satisfy the following two requirements:

1) System optimum: 3DSoC system efficiency

2) Individual rationality: the 3DSoC system can achieve equilibrium under constraints of individual rationality.

Optimum operator provides a certain band width, and each individual entity selects an allocation scheme to minimize its test time and test band width under constraints of the upper bound for the number of TSVs.

Let the costs for band width w allocation be $C(w)$, the payoffs for die i when achieves band w_i be $U_i(w_i)$, vector w^* be the scheme that optimum solution corresponds, $|w|$ the total test band width. Optimum operator determines the allocation scheme for test bandwidth according to a certain strategy. The scheme should maximize$\sum_i\{U_i(w_i)-C|w^*|\}$ while subject to:

1) $\max(\sum_i w_i)\leq W$

2) $\max(\sum_i w_i)\leq TSV_{max}$

Where W denotes the total band *width*, and TSV_{max} the available number of TSVs, die i has t_i TSVs, with band width being w_i, 3DSoC has M dies.

4.3. Algorithm for 3D SoC Test Optimization Based on Game Theory

To justify the bargaining model used to obtain the Nash Equilibrium solution for 3D SoC test optimization, a general assumption is taken about the condition under which the game is to be played. Either player is supposed to be completely informed on the structure of the game and the payoff function of his partner in addition to its own payoff function. The players are supposed to be able to make rational strategy.

***Algorithm** 3DSoCTestOpt*

Input: Actions $\{A_1, A_2\}$, payoffs $\{P_1, P_2\}$, strategies $\{S_1, S_2\}$, $T_{tolermargin}$, $W_{tolermargin}$

Output: a win-win Nash Equilibrium solution

Step 1: Each player selects a mixed strategy that it has to when they cannot reach an agreement, *e.g.*, their requirements are incompatible.

Step 2: each player informs the other of their common threats.

Step 3: each player acts independently without telling the other and makes decisions according to its own requirements. The two parts won't cooperate unless they can benefit from it.

Step 4: if neither of the two players can find the Pareto optimum that meets demand of both sides, and better outcome can only be obtained unilaterally, then execute the threat, go to step 3.

Step 5: if a Nash Equilibrium point is found, and interests of both sides are satisfied, and more requirements only lead to worse outcome, return the results, the algorithm ends, otherwise go to step 3.

4.4. Nash Equilibrium

Nash equilibrium captures a steady state of the play of a strategic game in which each player holds the correct expectation about the other players' behavior and acts rationally. The existence of Nash Equilibrium for 3D SoC test architecture optimization and test scheduling is equivalent to that for fixed point. According to Brouwer fixed point theorem, neither of the two players can get the maximized or minimized value simultaneously. Therefore the existence of Nash Equilibrium of such problem is demonstrated.

5. Experimental Results

Handcrafted benchmarks for 3D SoCs are built using ITC'02 d695, f2126, p22810, p34292 and p93791. In 3D SoC1, the complexity of benchmark grows from bottom to top *e.g.*,

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p93791, p34292, p22810, f2126, and d695, while for 3D SoC2, the benchmarks are d695, f2126, p22810, p34292 and p93791, 3D SoC3 takes the compromise, *i.e.,* f2126, p22810, p93791, p34932 and d695, the most complicated benchmark is put in the middle in facility of comparison.

In Table 1-4, TSVmax denotes the allowed maximized number of TSVs, and Wpin the number of test pins. "||"means parallel test of both dies before and after "||", ","serial test of both dies before and after ",". In Table 1 and 2, column 3 and 4 are the test scheduling results for the proposed method and Greedy algorithm respectively. The fifth column is the percentage of test length difference when shift from serial test to parallel test for 3D SoC2. Table 3 shows the test scheduling for three kinds of 3D SoCs.

Table 1. Experimental Results Comparison on 3D SoC2 of Hard Die between Proposed Method and Greedy Algorithm

TSV_{max}	W_{pin}	Test schedule		△(%)
		Proposed	Greedy	
160	30	0,1,2,3,4	0,1,2,3,4	0
160	35	0,1,2,3||4	0,1,2,3||4	0
160	40	0,1,2||3,4	0,1,2||3,4	0
160	45	0||2,1||4,3	0,1||3,2,4	6.5
160	50	0||3,1||2,4	0||3,1||2,4	0
160	55	0||1,2,3||4	0||1,2||3,4	0
160	60	0||1,2||3||4	0||1,2||3,4	4.2
160	65	0||1,2||3||4	0||1,2||3,4	4.2
160	70	0||1||3,2||4	0||1||4,2||3	0
160	75	0||1||3,2||4	0||1||4,2||3	2
160	80	0||1||2,3||4	0||1||4,2||3	2
160	85	0||1||3,2||4	0||1||4,2||3	2
160	90	0||1||3,2||4	0||1||4,2||3	2
160	95	0||1,2||4,3	0||1||4,2||3	36
160	100	0||1||2||4,3	0||1||2||3,4	0

Table 2. Experimental Results on n on 3D SoC2 of Soft Die between Proposed Method and Greedy Algorithm

TSV_{max}	W_{pin}	Test schedule		△(%)
		Proposed	Greedy	
150	30	0||1||2,3,4	0||1, 2,3||4	68.1
150	35	0||1||2,3,4	0||2, 1||3,4	79.5
150	40	0||1||2,3,4	0||2, 1||3,4	83.4
150	45	0||1||2,3,4	0||1||2,3||4	92.3
150	50	0||1||2,3,4	0||1||2,3||4	97.8
150	55	0||1||2||3,4	0||1||2||3,4	109.6
150	60	0||1,2||3||4	0||1||2||3,4	105.2
150	65	0||1,2||3||4	0||1||2||3,4	108.4
150	70	0||1,2||3||4	0||1||2||3,4	116.2
150	75	0||1,2||3||4	0||1||2||3,4	127.3
150	80	0||1,2||3||4	0||1||2||3,4	136.7
150	85	0||1||2||3||4	0||1||2||3,4	127.4
150	90	0||1||2||3||4	0||1||2||3,4	129.1
150	95	0||1||2||3||4	0||1||2||3,4	133.5

Table 3. Experimental Results for Test Scheduling of Proposed Method on Three 3D SoCs of Hard Die

TSV_{max}	W_{pin}	Test schedule		
		3D SoC1	3D SoC2	3D SoC3

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<table>
<tr><td>160</td><td>30</td><td>0,1,2,3,4</td><td>0||1||2,3,4</td><td>0,1,2,3,4</td></tr>
<tr><td>160</td><td>35</td><td>0,1,2,3||4</td><td>0||1||2,3,4</td><td>0||2,1,3,4</td></tr>
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<tr><td>160</td><td>95</td><td>0||1,2||4,3</td><td>0||1||2||3||4</td><td>0||1||2,3||4</td></tr>
<tr><td>160</td><td>100</td><td>0||1||2||3,4</td><td>0||1||2,3||4</td><td>0||1||2,3||4</td></tr>
<tr><td>160</td><td>105</td><td>0||1||2||4,3</td><td>0||1||2,3||4</td><td>0||1||2,3||4</td></tr>
</table>

Table 4. Test Time Reduction of Proposed Method Over Greedy Algorithm on Three 3D SoCs of Hard Die

TSV_{max}	W_{pin}	△(%)		
		3D SoC1	3D SoC2	3D SoC3
160	30	0	0	0
160	35	6.76	6.76	6.76
160	40	18.34	8.34	8.34
160	45	37.86	37.86	37.86
160	50	26.92	26.92	26.92
160	55	42.88	42.88	42.88
160	60	44.44	53.30	67.35
160	65	44.44	67.35	67.35
160	70	44.91	67.35	67.35
160	75	45.32	67.35	67.35
160	80	56.58	67.35	67.35
160	85	56.58	67.35	67.35
160	90	56.58	67.35	67.35
160	95	56.58	67.35	67.35
160	100	67.34	67.35	67.35
160	105	87.13	87.13	87.13

It can be inferred from Table 1 that for 3D SoC2 of hard dies, test time difference is no big when shifting serial test to parallel test, the difference ranges from 0-4.2%, and while in Table 2, the difference ranges from 68.1-136.7%, the reduction rate increases sharply. Therefore the proposed method be haves well especially for 3D SoC2 of soft dies. The maximum test time reduction reaches up to 136.7%. That makes sense because 3D SoC2 of soft dies provides the designers more freedom with fewer constraints, thus obtaining better performance.

Table 4 shows the percentage of test length reduction between the proposed method and Greedy algorithm.

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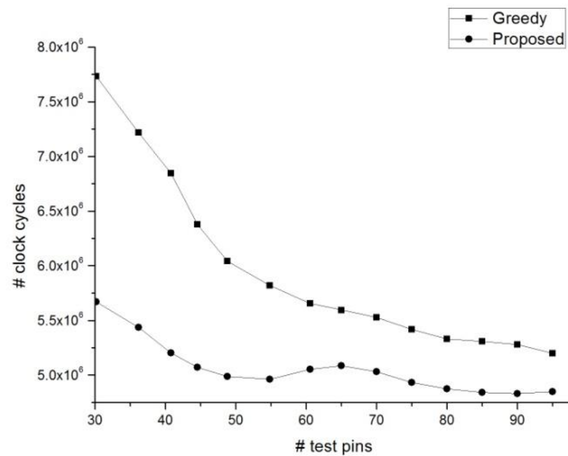

Figure 3. Test Time Comparisons on 3D SoC2 of Hard Die

Figure 3 shows test time for the proposed method and Greedy algorithm on 3D SoC2 of hard die. Obviously with the increase of test pins, test application time for both approaches decreases sharply and turns slowly when test pins reaches 60.

It can be seen that the proposed method performs better than Greedy algorithm. And test application time for both methods is minimized when the test band width (test pins) is maximum. The proposed method gets slight increase in test time when test pins rise to 55 and get the peak at 60.

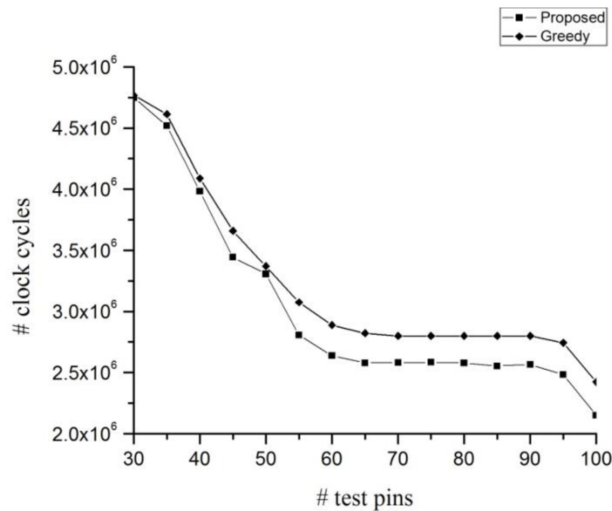

Figure 4. Test Time Comparisons on 3D SoC2 of Soft Die

While in Figure 4, the experiment is implemented on 3D SoC2 of soft die, the test time difference between the proposed and Greedy algorithm is subtle, however with the number of test pins increases, the proposed method got sharper reduction in test time than Greedy algorithm, with the exception of the case, they both take the same test time when the number of test pins reaches up to 50.

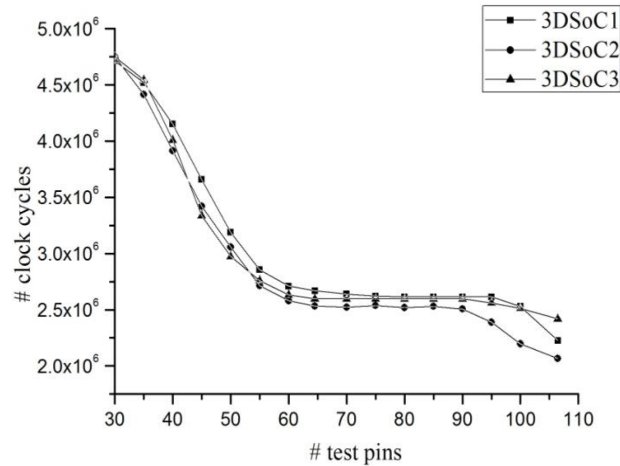

Figure 5. Test Time Comparisons between Serial and Parallel Test on 3D SoCs of Hard Die

Figure 5 shows the test time comparison on 3D SoCs when shifting from serial test to parallel test.

6. Conclusion

This paper proposes a novel approach to 3D SoC test architecture optimization and test scheduling under constraints of the number of TSVs and band width. Two-person cooperative game theory is applied for multi-objective modeling to get win-win outcome for the two players in the game. After multiple rounds of game, the benefits of both sides don't change by either side change its own strategy unilaterally, and then Nash Equilibrium point are obtained, and the double objectives of test application time minimization, TAM architecture optimization are obtained accordingly. Experimental results on handcrafted 3D SoC from five different benchmarks show the advantages of the proposed method over the previous methods, and optimal TAM design is obtained, test time is minimized.

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