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Implementation of Arithmetic Logic Unit Using FINFET

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Abstract

Today to complete the extra and difficult task the demand of refining ability of a processor is increasing step by step which resulted in the more fabrication of components fabricated on a single chip as the Moore Law. But with accumulative in a module the noise rises. The ALU is a one of the most important functional units in any CPU. The ALU is a core of any system or any processor as well as the core module of the central processing unit CPU. Since mostly all the simple operations are executed by the support of ALU only. As the name ALU denotes arithmetic logic unit, therefore it is used to execute the arithmetic and logical task in a digital bit. So the ALU can be defined as the combination unit which is used to implement its logical and arithmetic function units. The determination of this paper is to implement the Arithmetic Logic Unit (ALU) by a FinFet technique in 45nm. The work accomplished by ALU is Logic Action (OR, AND and EXOR) and Arithmetic action (ADDER). This result is before certain to the multiplexer and the result obtained is dependent on the input selector line. This result obtained is considered is in the term of average power and noise and paralleled with the dissimilar input value. The application takes domicile in a tool cadence virtuoso. In this paper is to present a modified low power ALU using Fin type field-effect transistors (FinFETs) technique and to compare that with the GDI technique at 45nm.

Keywords*: ALU (Arithmetic Logic Unit), CADENCE VIRTUOSO (tool), FINFET, GDI TECHNIQUE (gate diffusion input)*

1. Introduction

The main section of the processor is an arithmetic logic unit, An Arithmetic logic unit is very important part of the central unit processor (CPU). ALU is convoluted by implementing the operations of arithmetic and logical nature. There are possible only with the help of the ALU. An ALU is the also integrated packages, in this package comes the arithmetic and logic circuitry. For the entirely combinations like to consist of gate used the logic circuitry. An ALU is a tremendously multipurpose and suitable device since it is varieties obtainable in single chip's ability for performance many dissimilar logical and arithmetic task. Arithmetic Logic Unit (ALU) is a precarious module of a microprocessor and is the essential section of central processing unit. It is moreover the extreme easy going and advantageous part of processor as it consumes peak of the power of a processor. ALU is used to execute function which contains the addition, subtraction, OR, NAND and XOR function. With the escalation in number of functions, the speediness of an ALU is abridged so at the design level nearby is needed to rise the speediness of a processor by the appropriate choice of ALU function dependent upon use and kind of circuit to be implemented and designed. Present exists numerous method is present for the power lessening of ALU in which FinFet is as well the one of them. Fin type field-effect transistors (FinFETs) short gate method is the technique decreases the number of

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transistors in the circuit due to which power lesser. At present in the current computer processor are based on GPU (graphical processing unit).

1.1. Arithmetic Logic Unit

The Arithmetic Logical Unit is that the important scheme within the digital system style. Associate degree Arithmetic logic Unit (ALU) is associate degree integral a part of a computer processor. It's a combination logic unit that performs its arithmetic and logic operations. ALUs of assorted bit-widths are of times needed in terribly large-scale integrated circuits (VLSI) from processors to application specific integrated circuits (ASICs). ALU is obtaining smaller and additional advanced these days to alter the event of an additional powerful however smaller PC.

The demand for low power and; high speed process has been increasing as results of increasing pc and signal processing applications. Higher turnout arithmetic operations are necessary to realize the required performance in several time period signal and image processing applications. The key arithmetic operations in such applications are multiplication, addition, division and subtraction.

Present be there many low power techniques where gift lately within which FinFET is additionally one amongst them. At the current time a FinFET and GDI are the furthermost usually used technique for the alteration of power because it shrinks the change of output. Additionally, a GDI technique is employed to cut back the amount of semiconductor unit of the reduction in space of chip. The foremost usually cell associate exceedingly in a very GDI technique is an electrical converter cell that is made by the mix of one PMOS and NMOS. Here one input is provided to the gate terminal of each and so output is taken out.

The below is provided the fundamental gated shaped by the assistance of GDI technique.

2. FinFET Technique

The FinFET has been inflated to select up the issues sweet-faced by MOSFET. It's mostly a mufti box workplace Field Effect semiconductor that has been scaled additionally

Of MOSFET. It's for the foremost half properties redolent to a semiconductor, anyhow has some advantages of CMOS. As you chop back saw the behind figures, a thousand and one drain and a thousand and one source, we tend to give a notice additionally appraise every pair of dealer and coming back to some extent are often planned as a successful semiconductor hereafter increasing the now of transistors in one

FinFET.

MOSFET has some manufacturing plant created issues like

i) Short channel chattels personal and ii) Corner result Corner. Effects has the following problem:

a) An improvement of the run avant-garde at the parameters of the cautious space consider tacky trench isolation
b) Run improvement is very lucky, if the box workplace conduct or wraps all over the move during a circle of the watchful space
c) Corner finish ends up in a not diligent switching-off of the STI MOS semiconductor units and worsens the transistor Performance.

So to come back the exhausting nut to crack baby-faced by timid MOSFET, FinFET came into approach to life and to work the transistors additional Efficient. Wider FinFET devices are off the rack utilizing multiple are the terrible image of fins encircled by the person and drain. Freelance

Gating of the FinFET’s does a takeoff gates permit pertinent reduction in the current run.

2.2. GDI Technique

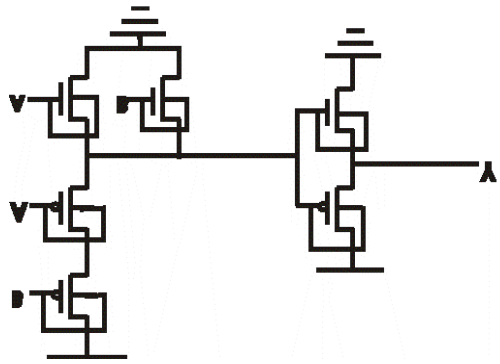
The GDI cell resembles a CMOS convertor structure. In Associate in Nursing extremely CMOS convertor the provision of the PMOS is connected to VDD and additionally the provision of NMOS is grounded. But in Associate in Nursing extremely GDI cell this might not primarily occur. There are some necessary variations between the two. The three inputs in GDI are namely-

1) G- common inputs to the gate of NMOS and PMOS
2) N- input to the source/drain of NMOS
3) P- input to the source/drain of PMOS

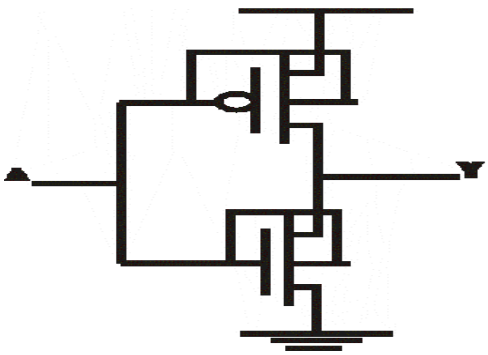
Bulks of every NMOS and PMOS area unit connected to N or P (respectively) that is it's at random biased not like in CMOS convertor. Moreover, the foremost necessary distinction between CMOS and GDI is that in GDI N, P and G terminals can be given a supply 'VDD' or is grounded or is supplied with signal relying upon the circuit to be designed and so effectively minimizing the amount of transistors used just in case of most logic circuits (eg. AND, OR, XOR, MUX, *etc*.). As a result of the allotment of supply and ground to PMOS and NMOS is not mounted simply just in case of GDI, therefore, disadvantage of low voltage swing arises of GDI that might be a drawback and so finds issue just in case of implementation of analog circuits.

3. Logic Gates Using FinFet –

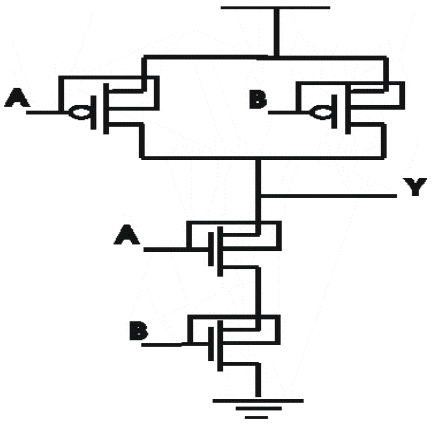
These are some basic logic gates derived by use of FinFET.



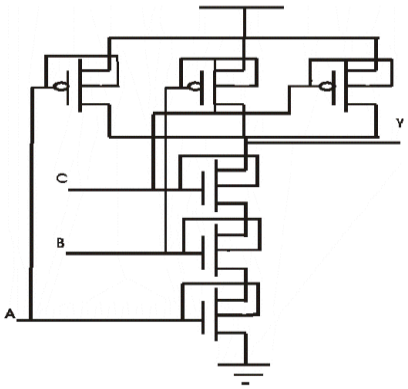
(a) OR GATE



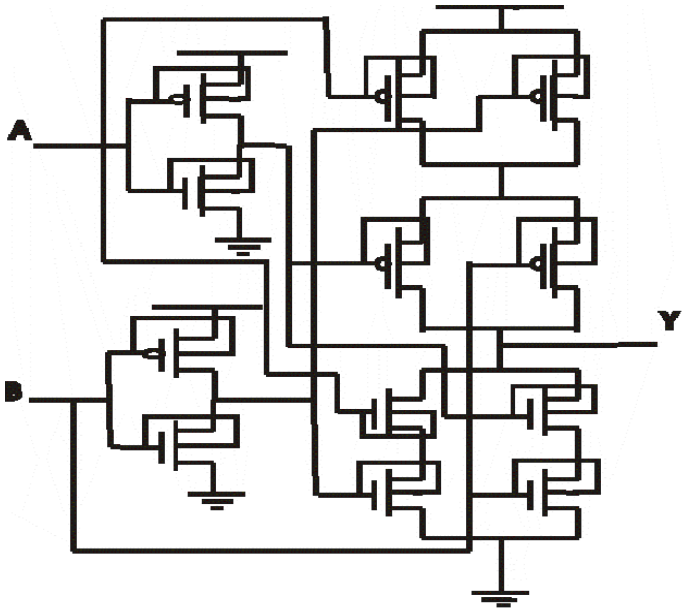
(b)NOT GATE



(c)2 INPUT AND GATE



(d)3 INPUT AND GATE

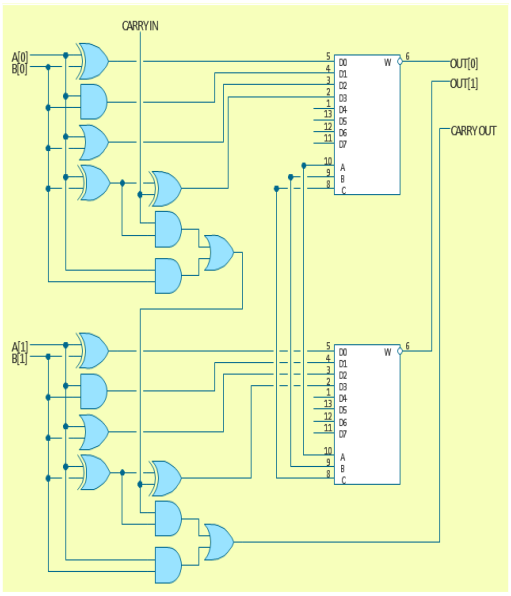


(e) XOR GATE

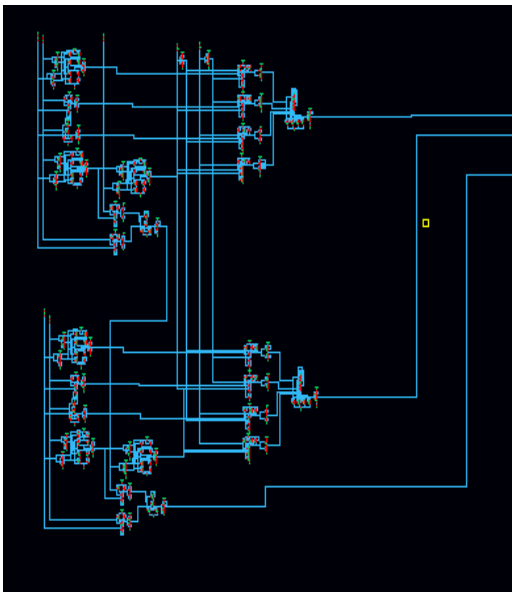
Logic Gates (A) Or Gate (B) Not Gate (C) 2 Input Nand Gate (D) 3 Input Nand Gate (E) Xor Gate

4. Simulation and Result

In this section, we show the simulation and results related to the technique. We are finding some parameters with the help of tool cadence virtuoso. Circuit diagram and schematic diagram shown as.

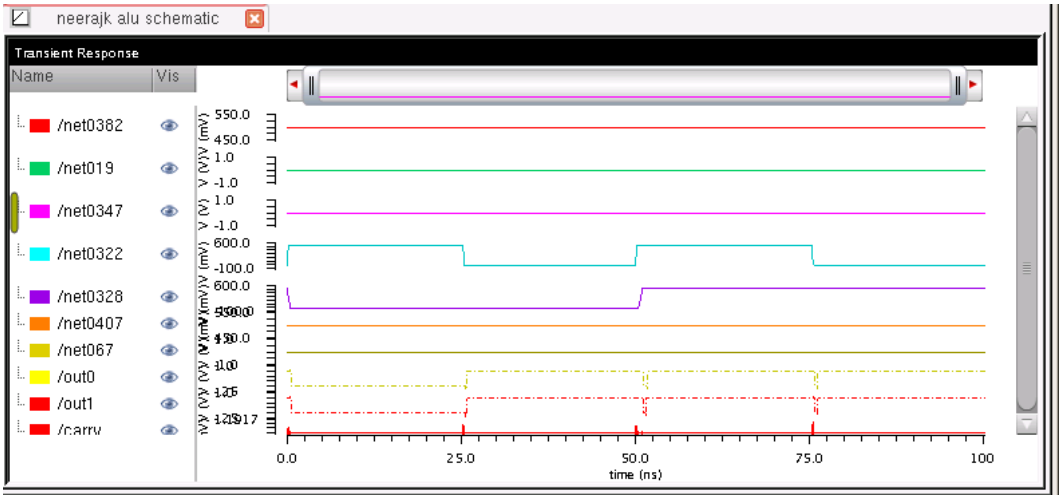


Circuit Diagram of Arithmetic Logic Unit .



Schematic Diagram of Arithmetic Logic Unit

4.1. Waveform of ALU Using FinFET



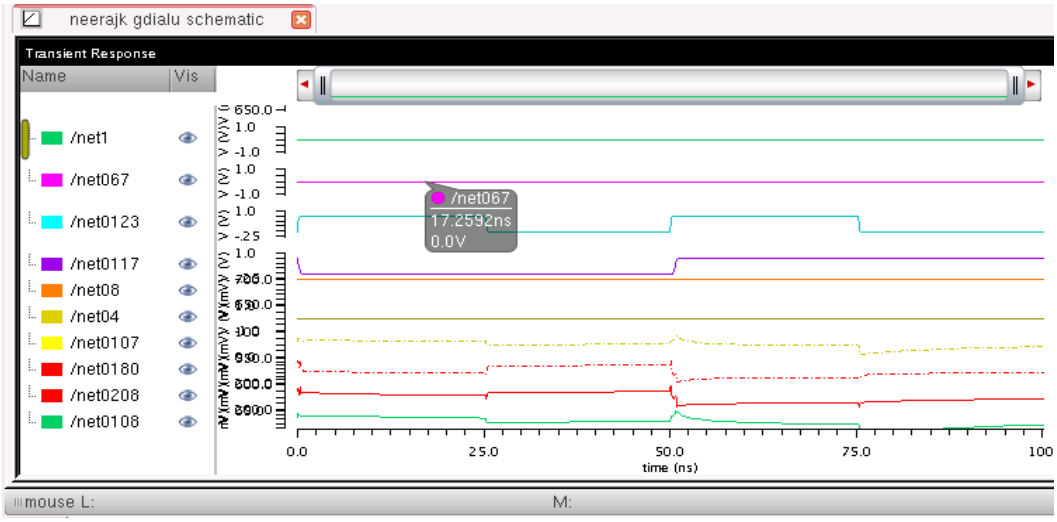
Waveform of Arithmetic Logic Unit Using FinFET

4.2. Parameters

Table for Transient and Noise Analysis using FinFET Technique-

Parameters / Input value	0.5v	0.6v	0.7v
Transient analysis	$24.78e^{-6}$	$26.45e^{-6}$	$31.55e^{-6}$
Noise analysis	$8.38269e^{-15}$	$8.384889e^{-15}$	$8.38441e^{-15}$

Waveform of ALU Using GDI



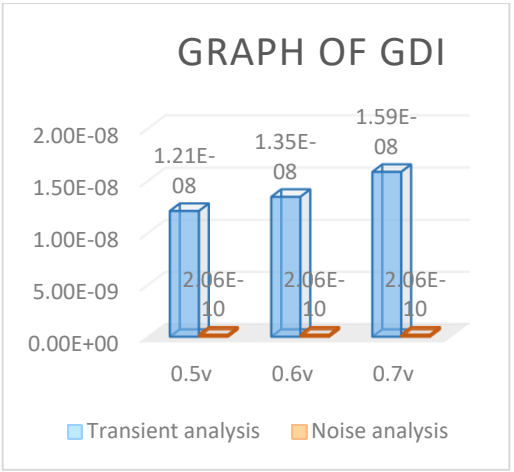
Waveform of Arithmetic Logic Unit Using GDI

4.3. Parameters

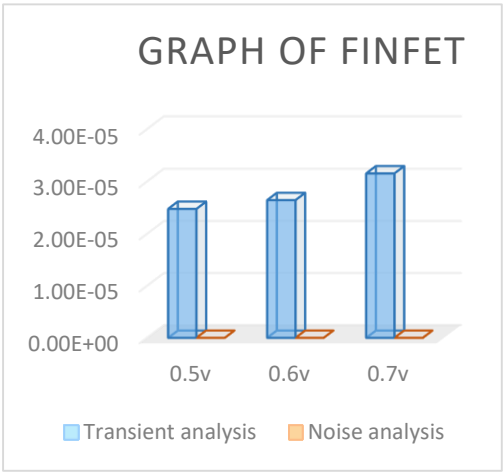
Table for Transient and Noise Analysis Using GDI Technique-

Parameters / Input value	0.5v	0.6v	0.7v
Transient analysis	$12.11e^{-9}$	$13.46e^{-9}$	$15.85e^{-9}$
Noise analysis	$2.06054e^{-10}$	$2.06079e^{-10}$	$2.06083e^{-10}$

4.4. Graphs-



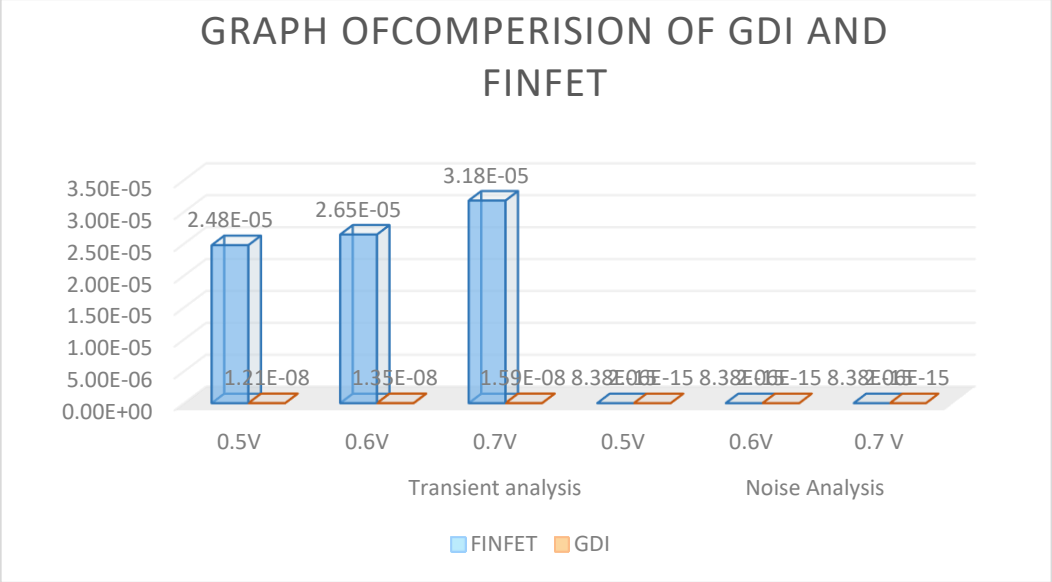
GRAPH OF GDI



Comparision of GDI and Finfet-

Table of Comparision of GDI and FINFET

Parameter	Input Value	FINFET	GDI
Transient analysis	0.5V	$24.78e^{-6}$	$12.11e^{-9}$
	0.6V	$26.45e^{-6}$	$13.46e^{-9}$
	0.7V	$31.78e^{-6}$	$15.85e^{-9}$
Noise Analysis	0.5V	$8.38269e^{-15}$	$2.06054e^{-15}$
	0.6V	$8.38489e^{-15}$	$2.06079e^{-15}$
	0.7 V	$8.38441e^{-15}$	$2.06083e^{-15}$



Graph of Comparison of GDI and FINFET

5. Conclusion

In this paper, we are comparing two low power techniques. We have to find that the GDI technique is better in term of transient and power analysis. But there is FINFET technique is better in term of noise analysis. In this era and upcoming era of digital electronic both low power technique is used in large amount. It is often seen that enormous range of functions is often enforced exploitation the essential GDI cell. MUX style is that the most advanced style which will be enforced with GDI, which requires solely two transistors, which needs 8-12 transistors with the traditional CMOS or FinFET style. Several functions are often enforced with efficiency by GDI by suggesting that of semiconductor count. Logic gates are enforced in SG, FinFET offers faster-switching speed and reduces the run current. Implementation of adder circuit and storage device victimization FinFET due to its high performance.

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