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# Low Power Reconfiguration of Approximate Arithmetic Units Using Verilog HDL

Nithin Nagabasavanna[1] and Nagaraju Chowdaiah[2]

*[1]M.Tech Scholar, [2]Profressor, BGS Institute of Technology, Karnataka, India*
*nithinnithu10@gmail.com, nagaraj.bgs@gmail.com*

***Abstract***

*Approximate computing is the theme that a system can let applications trade off accuracy for efficiency. It involves any technique where the system intentionally let on incorrectness to the application layer in order for conserving some resource. Floating point numbers i.e. approximate real number arithmetic to save space and time over arbitrary precession numerical representation. Approximate (APP) Computing is a technique of computation which ripostes less accuracy in results instead of an accurate output, which is enough for the desired application. The proposed work gives the basic allies on approximate computing based on arithmetic units using Verilog HDL. In dual mode operation, full adders and its types of adders resemble minimizing the power consumption and overall delay. Results show the great power saving efficiency and the 37mV and overall delay of 15.519ns.*

***Keywords****: VLSI, Approximate circuits, approximate computing, design of low power, Verilog*

## 1. Introduction

Degree of approximation defines the efficient role in the stadium of low power technologies. Many implications have been made in order to reduce the power consumption. This will help in various processors compressors and signal processing systems to work in power efficient mode. Various techniques can be used to perform approximate computing. The main intention of scaling CMOC into the nano scaling is to decrease the area constraints but in parallel it decreases the yields [1]. Error tolerance came into picture in order to reversing the trend in virtual manner by developing new methodologies for chips that are used in many endeavor say, audio, video, gaming, visual graphics also in wireless communication. In these techniques error occurred within thresholds are deemed acceptable [2]. Due to these technologies the reconfiguration data can be implemented to overall benefits.

Field-programmable gate arrays are tremendously used as the computing platform in the fast and efficiency of energy execution of recognition mining and search applications. Approximate computing is one trust worthy method for attaining energy efficiency [3]. Compared with most foregoing works on inexact computing which target approximate processors and blocks of arithmetic. So, re-designing technique mainly focuses on reducing delay of data path modules to improve parametric yield [4]. In particular, multiple approaches and applying them to improve yield of a wide range of adder architectures by exploiting error tolerance in these applications is came into existence. Experiment results show that even for small thresholds on error severity, one can obtain significant improvements in manufacturing yield.

However, many proposed hardware architecture is based on the manipulating the input or manipulating the bound operations which fails to give expected output at certain conditions and the operations has to be compromised. In several cases output quality degraded severely. In some power saving techniques by approximation technology fails

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due to lack of considerations of Degree of Approximation (DA) while designing [5]. This leads to the unexpected output and further compromising the result.

Earlier adder sub-tractor blocks are very high power conservative modes in approach. The delay constraint is also severe in the early approach. While considering the overall result, the power and delay increases gradually and the efficiency decreases. Therefore to overcome the drawbacks dual mode approach id proposed in this work.

## 2. Design Implementation

Proposed work gives the contributions made specifically in followings

1. First and foremost this work throws all specified information regarding One bit DMFA (Dual Mode Full Adder) Cell
2. Eight bit reconfigurable RCA (Ripple Carry Adder) flat
3. Eight bit reconfigurable CLA (Carry Look Ahead Adder) flat
4. DMCLB1 (Dual mode Carry Propagation Block 1) and DMCLB2 (Dual mode Carry Propagation Block 2)
5. DMPGB1 (Dual mode Carry Generation Block 1) and DMPGB2 (Dual mode Carry Generation Block 1)
6. This process will be continued in all the aspects of accurate and approximate features.

The experimental result shows the drastic reduction of the power and timing endeavors

### 2.1. One bit DMFA Cell

One bit DMFA cell is the reconfiguration of the general arithmetic unit in dual modes of operation in which each adder can wield in Accurate / Approximate-mode of operation by keying the control of signal that is APP signal that drives the modes of operation.

If the value is given one it is working in the mode accurate and if the value given by the user it is working in the mode approximation. This, proposed adders/subtractor is called as Reconfigurable-Adder Subtractor Blocks (RABs). The Proposed Dual Mode Full Adder is shown in Figure 1. The first time designed architecture gives the result that is similar to the basic operation of adder and in reused in the power en caption and the total duration of delay in working in the dual turns. This creates a new path in the arithmetize units designing in the new way of power consecrations.

 

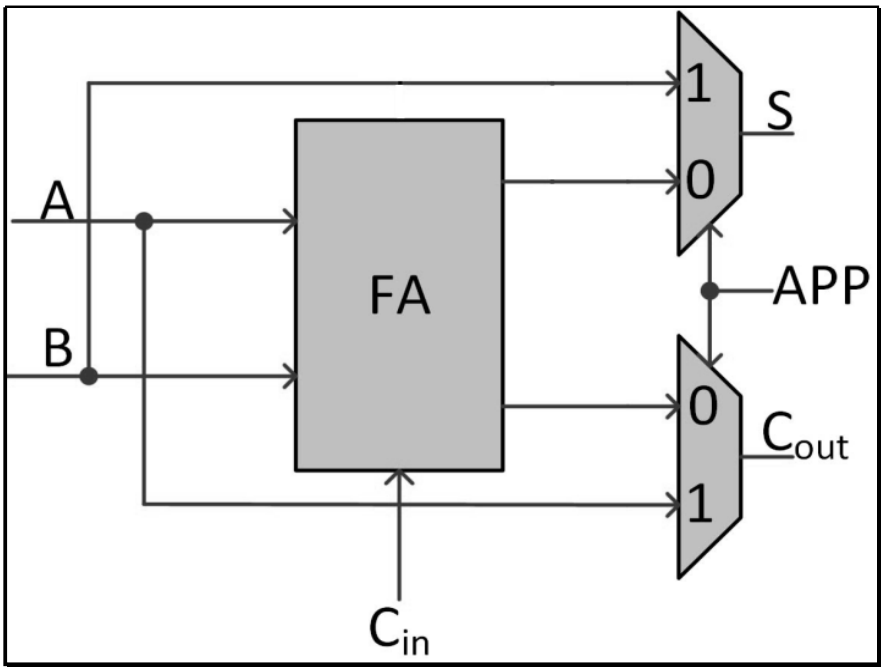


**Figure 1. One Bit Dual Mode Full Adder Cell**

The figure 1 shows the operation of one bit DMFA. Based on the approximate signal the operation of the full adder is decided whether to work in which unique mode. The output result shows the tremendous approach in result of power saving and less delay. This is the main approach in dual mode of operation. Keeping this as base various adders can be implemented.

### 2.2. Eight-Bit Reconfigurable RCA Flat

The eight bit reconfiguration of the adder ripple carry is as shown in figure 2. It is connected parallel one after the other in refer to the basic design but in enhanced part the basic design is modified nu concaving the mux and the driving point as decoder . Here we used a mux of 2.1 and 3.8 decoder.

Each mux carries the previous carry to the next confiscation adder and the decider provides the carry in. The decoder also helps in operation of the dual mode. It selects the Accurate and Approximate mode automatically. In one bit user can force to operate in two modes but in eight bit operation cannot be forced so it automated by the decoder. In the operation mux selects the output produced by the recurring full adder. Results gives the enormous saving of power and efficiency compared to the normal FA. By this designing technique the area can be overhead but the rest of the concerns desecrates.

In the eight bit operation for each and every cycle of operation we can't give values for APP. Therefore decoder comes to play. This reduces the overall delay in the circuit optimization. Decoder automatically approximates the operation to work either in two modes. For the eight bit operation 3:8 decoder is placed as shown in above figure.

The implementation of the dual mode RCA compared to the normal RCA induces the large amount in power saving and the lesser delay in operation and just a slight increase in the area because of introduction of the decoder in the circuit implementation.

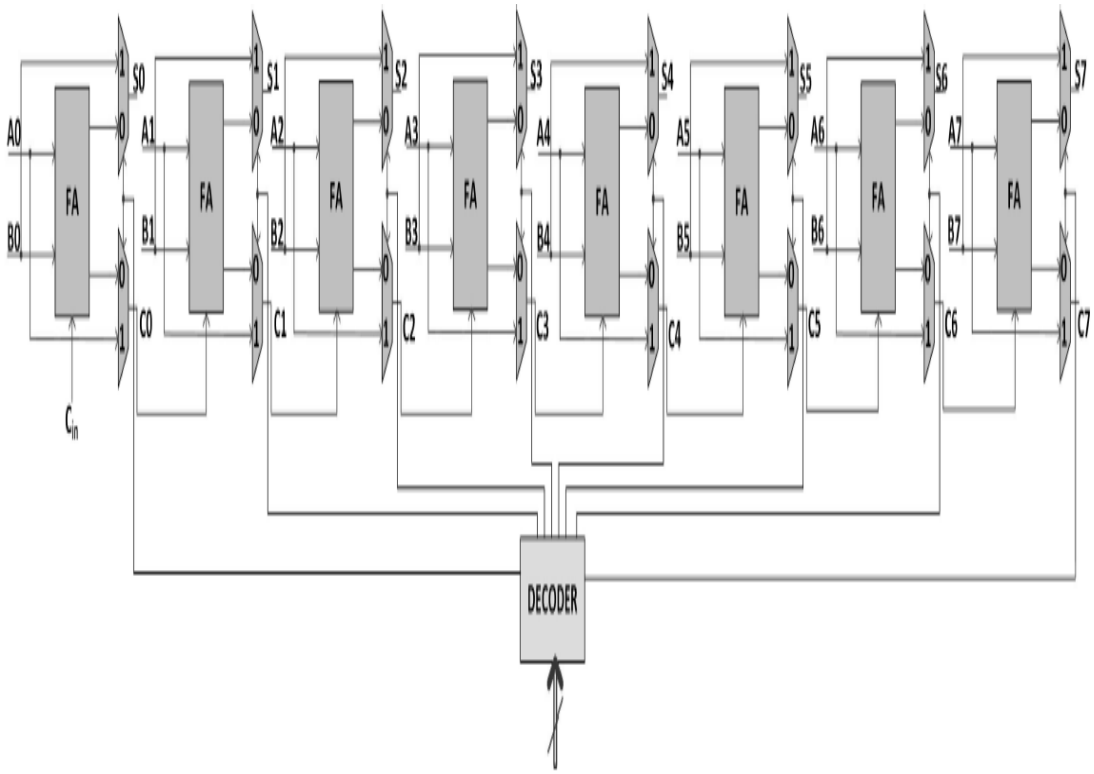


**Figure 2. Eight-Bit Reconfigurable RCA block**

### 2.3. Eight Bit Reconfigurable CLA (Carry Look Ahead Adder) Flat

Before designing the reconfiguration of dual mode CLA the basic key note to be analyzed is there is a presence of the generation and propagation operation in this adder. The redesigned of the adder base to the normal adder is as illustrated in figure 3. The presence of the carry generation and carry propagation analysis makes the design interesting and important. In this operation mux is not used and instead of mux dual modes of generation and propagation of carries are used.

The working operation is done level by level mode. At first the lower levels is calculated and the respective results is passed to the next level. Then the final carry generated id passed to the top level and the calculations is made, here decoder approximately selects the modes of operation to which have to work in either modes.

In Carry Look Ahead blocks there are two main constraints to give importance *i.e.*, Carry Propagation and Carry generation blocks. In dual mode implementation also there should be given importance for the propagation and generation blocks. The above figure gives the detailed implementation of the CLA block based on carry propagation and generation architectures. Output of the designed circuit is processed by the row wise operation and analysis. At first DMCLB 1, 2 and DMPGB 1 is processed and output is passed to DMPGB 1. In parallel first and second row operation is done and output is passed to the next corresponding row. Finally top row is synthesized to obtain reconfigurable CLA. Decoder plays a main role in CLA block operation and it acts as a Cin for the respective next block carrying the previous Cout.

 

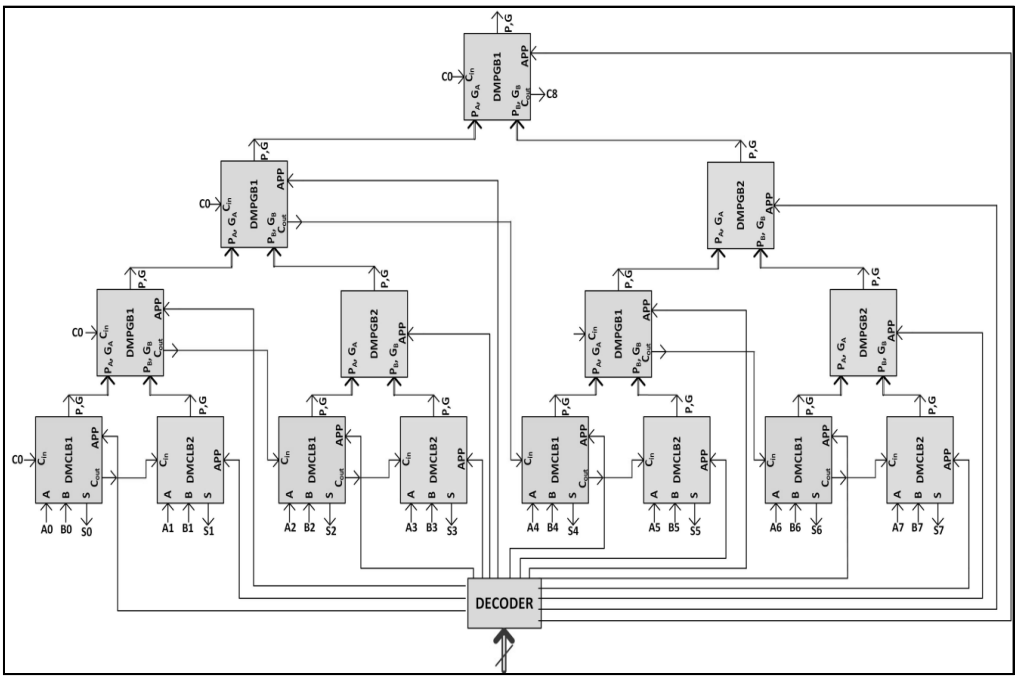


**Figure 3. Eight-Bit Reconfigurable CLA block**

Output of the designed circuit is processed by the row wise operation and analysis. At first Dual mode carry generation block (DMCLB) as shown in Figure 4 and Dual mode carry propagation block (DMPGB) as shown in Figure 5 is processed and output is passed to next level dual mode CLB & PGB blocks. In parallel first and second row operation is done and output is passed to the next corresponding row. Finally top row is synthesized to obtain reconfigurable CLA. Decoder plays a main role in CLA block operation and it acts as a Cin for the respective next block carrying the previous Cout.

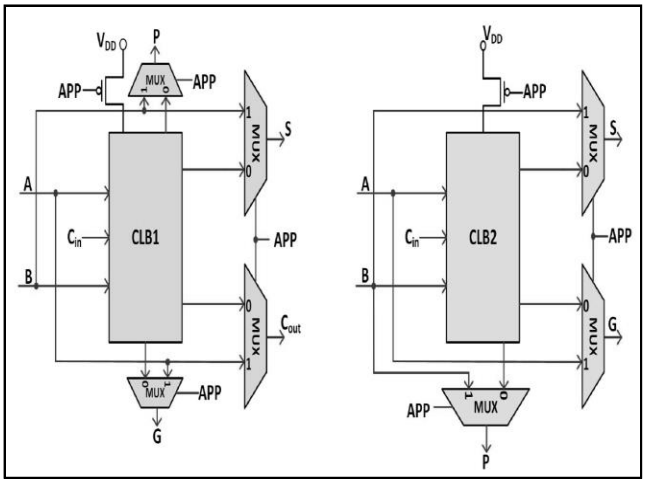


**Figure 4. Representation of Dual Mode Carry Generate Blocks**

Below equations are used in designing the dual mode carry generate blocks in approximate mode with respect to Figure 4

For DMCLB1:

$$P=B \quad \text{….2.1}$$
$$G=A \quad \text{….2.2}$$
$$S=B \quad \text{….2.3}$$

Cout = A ….2.4

For DMCLB2:

P=B ….2.5

G=A ….2.6

S=B ….2.7

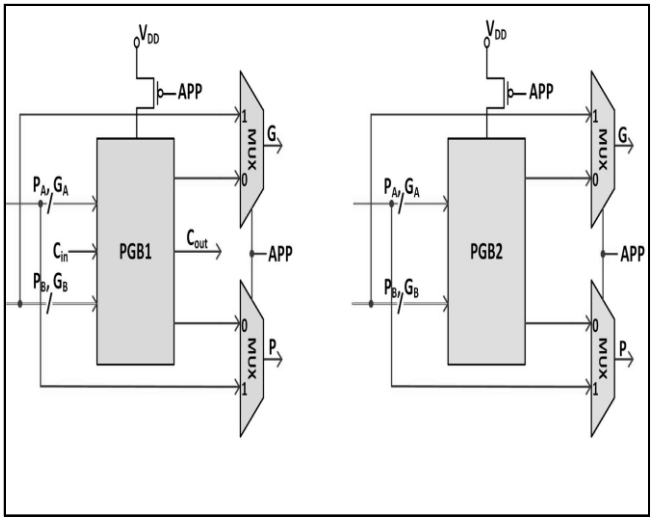


**Figure 5. Representation of Dual Mode Carry Propagate Blocks**

Below equations are used in designing the dual mode carry propagate blocks in approximate mode with respect to figure 5.

For DMPGB1:

$P=P_A$ ….2.8

$G=G_B$ …. 2.9

Cout = G+PCin …2.10

For DMPGB2:

$P=P_A$ ….2.11

$G=G_B$ ….2.12

Equations discussed are utilized in verilog computing of dual mode operations. In modern computation technique, approximation computation methodology can be applicable to the various domains. One predefined observation to be made is that, it is suited for the systems or applications which are error tolerant. Approximate computing has took its own palace in multimedia processing, signal processing, machine learning, scientific computing an all basic arithmetic computing can be approximated by this methodology. The goal is to enable efficient inference to baseline approach. The fields of computation in approximate manner ensures more concern in technology in previous stages of year mainly the domain of image- processing applications, compression technology in videos and also in various VLSI domains

## 3. Experimental Results

This overall scenario is verified by using the software Xilinx and modlesim. The power analysis and the delay is drastically reduces as compared to the previous endeavors The area increase is negligible compared to power analysis constraints in future applications this methodology can also be extended to various fields. In the normal operation the power consumptions of the 43mv but in the proposed analysis the power value is reduces to the 37mv and delay operation is also reduces to 17.423 ns to 15.519ns. For the convenience the simulation results are also discussed in the further sections.

 

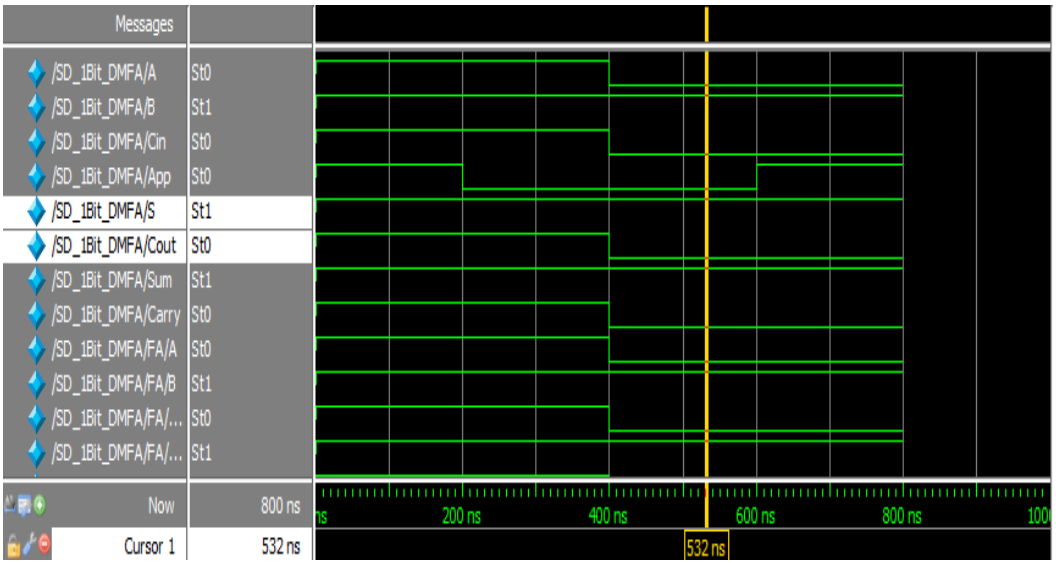


**Figure 6. Simulation Result of One Bit DMFA**

**Description:** The simulation result is obtained to base to Figure 1, in the simulation result, DMFA is working in dual mode of operation. When APP is set to 1 it is working in accurate mode and in next session it is set to 0 so it is working in approximation mode. Table 2 generalizes the output in accurate mode and approximate mode. As seen there is only a change in last column of the output in 1 bit addition operation. So it does not cause any impact in overall output and it is can be negligible. By this this techniques can be applied to error tolerant applications and the gain of the power saving can be achieved with less delay constraints.

**Table 2. Analysis of 1 Bit Full Adder in Accurate and Approximate Mode**

| A | B | Accurate mode | Approximate mode |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 |

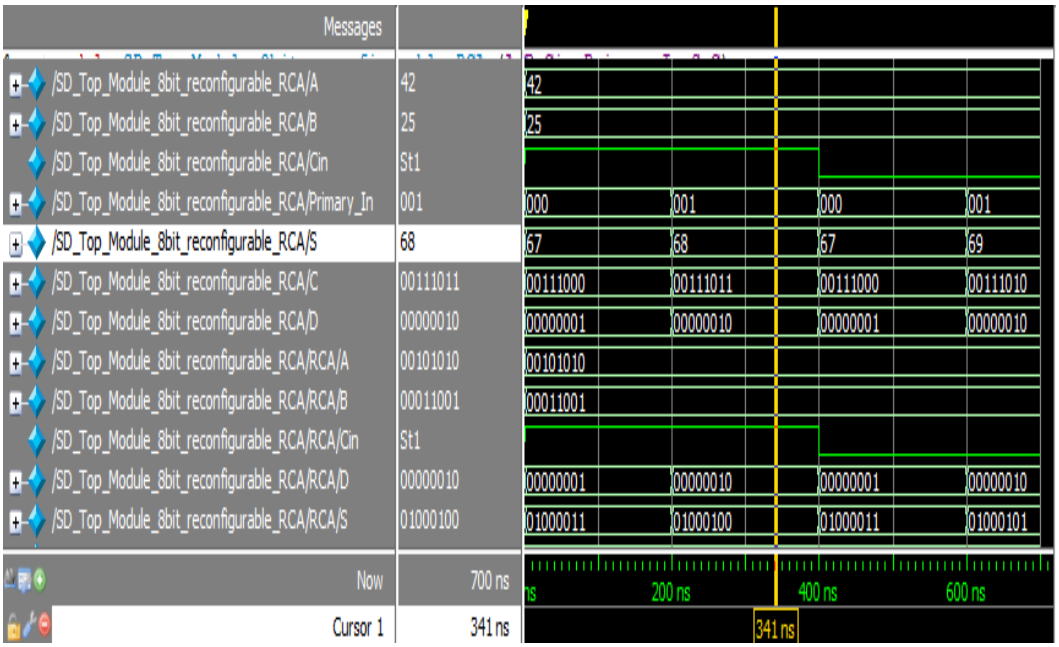


**Figure 7. Simulation Result of 8bit Reconfigurable RCA Block Working in Accurate Mode as well as Approximate Mode**

**Description:** The simulation result is obtained to base to the dual mode operations of the RCA in Figure 2. The Figure 7 is the simulation result obtained in operation of Dual mode RCA. The addition operation shown in Figure as 42 plus 25 which gives 67, but the actual result should be 68. So the module is working in approximate mode as well. The difference is 1 bit so it is negligible and it does not impact on output and it is tolerable.

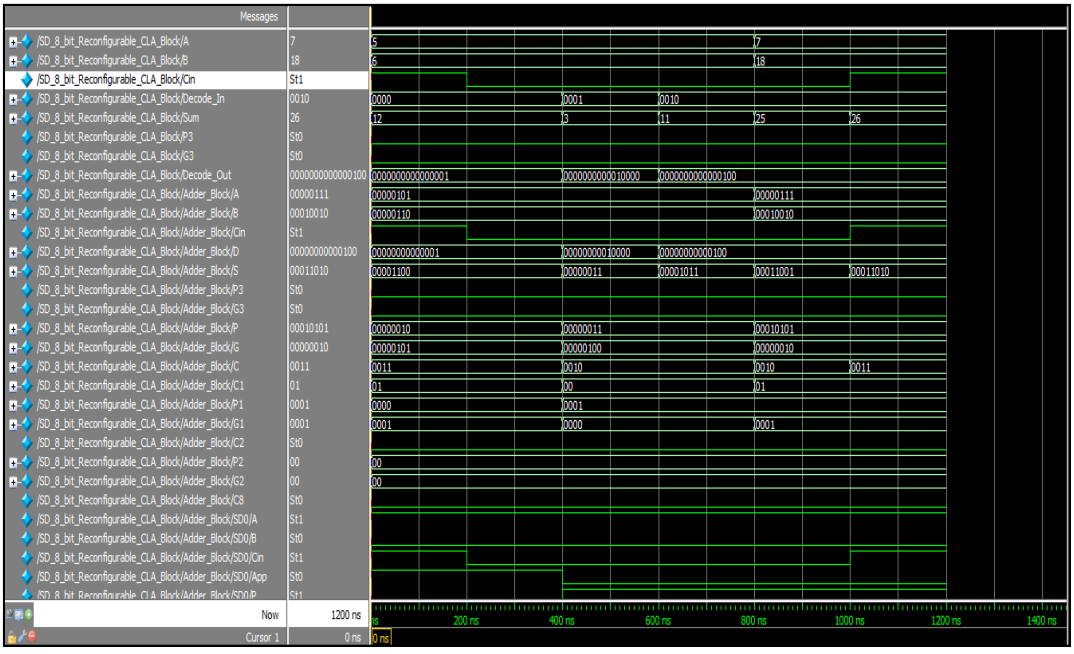


**Figure 8. Simulation Result of 8bit Reconfigurable CLA Block Working in Accurate Mode As well As Approximate Mode.**

**Description:** The simulation result is obtained in Figure 8 is base to the dual mode operations of the CLA in Figure 3. The addition operation taken in this scenario is operation 7 plus 18 gives the exact result of 25, so it is operating in accurate mode. In third cycle of operation same scenario 7 plus 18 which give 26, but the actual result should be 25. So the module is working in approximate mode as well. The difference is 1 bit so it is negligible and it does not impact on output. By these scenarios the verification of dual mode operation in accurate and approximate mode is done.

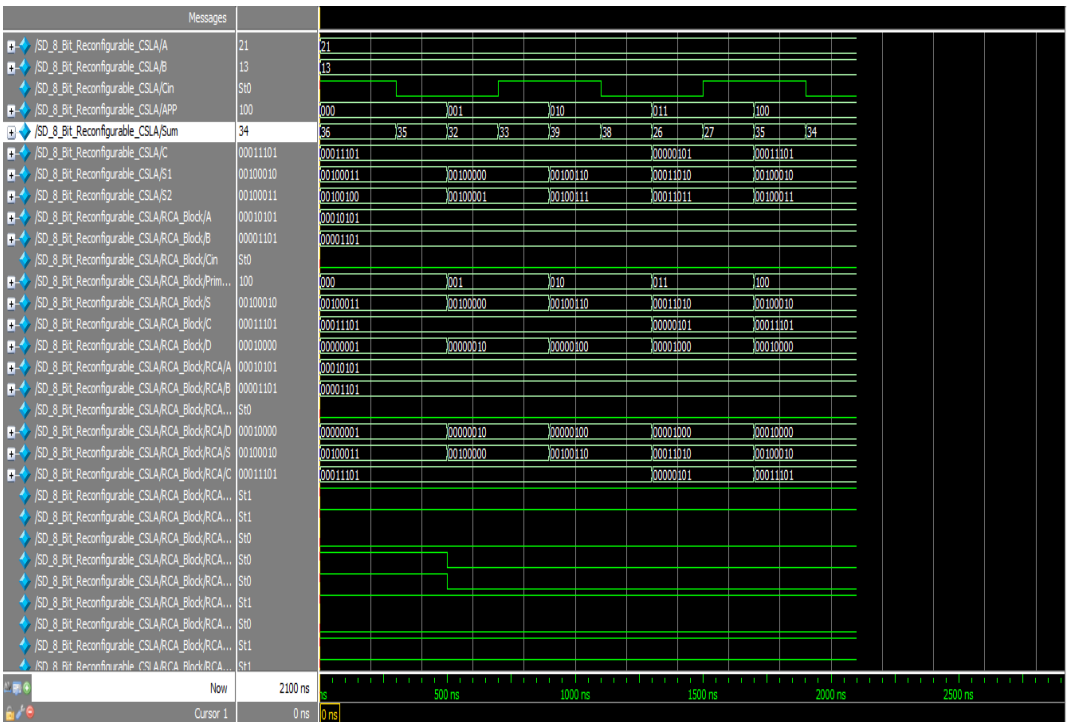


**Figure 9. Simulation Result of 8bit Reconfigurable CSA Block Working in Accurate Mode As well As Approximate Mode**

**Description:** The simulation results in Figure 9 is the enchantment part of the project justifying the 8 bit dual mode carry select adder working in approximate and accurate mode. In this scenario addition of 21 plus 13 is taken and output gives 34, which specifies it is working in accurate mode. In next cycle of operation output gives sum as 33 and 36. This specifies it is working in accurate mode of operation. The result obtained is one or two bit error rate in approximate mode as compared to accurate mode. So there will be no huge impact in output result in error tolerant operations. By this the power consumption of such devices and the delay constraints can also be rescued to major extent. The power analysis and timing analysis shows the drastic reduction in output results. By this one can conclude that dual mode operation can be much more efficient and adaptable to error tolerant applications.

**Table 3. Comparison of Results: In Power, Area and Timing Constraints In Normal And Dual Mode Approximations**

| | Power | Delay | | | Area | | |
|---|---|---|---|---|---|---|---|
| | | Gate | Path | Overall | LUT | Slices | Gate |
| Normal Analysis | 42mW | 10.201 ns | 7.22 ns | 17.423 ns | 16 | 10 | 105 |
| Proposed Analysis | **36mW** | **9.220 ns** | **6.29 ns** | **15.519 ns** | 26 | 15 | 156 |

The table III gives the comparison between the Power Area and timing constraints in designed methodology. The proposed work shows the successful drastic reduction of power of 36mV. Delay constraints in various aspects like Gate delay, Path delay and Overall delay is comparatively reduced to 9.22ns, 639ns and 15.519ns respectively. Due to some circuitry overhead, area constraints are quite increased.

## 4. Conclusion

The proposed work includes Realization and reconfiguration of approximate arithmetic unit in which the main concern is to reduce the power consumption in arithmetic unit operations. Reduction of the power in 1 bit DMFA makes it well suitable for the low power operation systems and fast execution systems. The trail of the adder/ subtractor blocks is also proposed keeping the 1 bit DMFA as a base in that Dual mode RCA, Dual mode CSA, and Dual mode CSA is also analyzed. The experimental result shows the drastic reduction of the power compared to the previous work. These approximation methodologies can also be extended to the various applications like video encoding and compression and digital signal processing where the power constraints and delay plays a severe role in the process.

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