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Design & Performance Analysis of Low Power Reversible Residue Adder

Ankush[1] and Amandeep Singh Bhandari[2]

[1]*M.Tech (Research Scholar) Department of ECE Punjabi University, Patiala, India*
[2]*Assistant Professor Department of ECE Punjabi University, Patiala, India*
[1]*amongia9@gmail.com*, [2]*singh.amandeep183@gmail.com*

Abstract

Adder circuits play an important role in reversible computation, which is helpful in diverse areas such as Low power CMOS design, quantum computing and nano technology. A reversible gate has equal number of inputs and outputs; so that, there should be one to one mapping between input and output vectors. Therefore, the input vector states can be always uniquely recovered from the output vector states. This paper presents a reversible residue circuit that requires only two reversible gates i.e. Modified TSG gate and Modified Fredkin Gate and consumes Low power. The design provides a significant reduction in the quantum cost of the circuit compared to the existing Residue Adder reversible logic implementation. For coding of design, VHDL language has been used. Xilinx design tool 14.4 and Xilinx project navigator tools are used for synthesis and simulation purpose.

Keywords*: Reversible logic, Residue Adder, Power Measurement, Quantum Cost*

1. Introduction

Reversible logic is a concept of digital circuit design which was invented with the concept of creating digital logic circuits with zero power consumption and minimum power loss. It replaces irreversible logic gates with reversible gates in the conventional digital circuits.

Reversible logic has received great attention in the recent years due to its ability to reduce the power dissipation .Normal combinational logic circuits dissipate heat for every bit of information lost during their operation. Due to this the recovery of a piece of information once lost is completely impossible. However, if the same circuit is constructed using the reversible logic gates, not only is the recovery possible but also the dissipation of heat reduced. According to Rolf Landauer (1961), whenever we use a logically irreversible gate we dissipate energy into the environment. The loss of information is associated with laws of physics requiring that one bit of information lost dissipates kTln2 of energy, where k is Boltzmann' constant and T is the temperature of the system. Interest in reversible computation arises from the desire to reduce heat dissipation, thereby allowing [1]:

I. Higher densities

II. Higher speed

Later Bennett, in 1973, showed that this KTln2 joules of energy dissipation in a circuit can be avoided if it is constructed using reversible logic circuits [2].

According to Moore's law, the number of chip components doubling every 18 months, the irreversible technologies would dissipate a lot of heat and heat reduces circuit life. Reversible logic not only recovers the lost information but also dissipate less heat.

A Reversible Logic Gate is an n-input, n-output device with One-to-One Mapping, which helps in determining the outputs from the inputs and vice versa. An important

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constraint present on the design of a reversible logic circuit using reversible logic gate is that fan-out is not allowed wherever necessary, extra outputs can be added to make the output count equal to that of the input. The main challenges are reducing Quantum Cost and Power Consumption.

Reversible logic has numerous applications in the field of electronics and microelectronics which are ultra low power in nano scale computing, quantum computing, emerging nanotechnology cellular automata and the other approach of reversible logic is ballistic computation, mechanical computation

2. Terms Related to Reversible Logic Gates

2.1. Quantum Cost

Quantum Cost of the circuit is considered by knowing the number of simple reversible gates (gates of which rate is previously identified) needed to realize the circuit.

2.2. Garbage Output

The output of the reversible gate that is not used as a main output or as input to other gates is called the garbage output. In little the unexploited output of a reversible gate (or circuit) is the garbage output (s). These garbage outputs are required in the circuit to retain the reversibility concept. [4]

2.3. Constant Inputs

The proposed reversible full adder gate requires only one constant input and it is theoretically minimum.

2.4. Gate Count

Total number of reversible logic gates used to implement the intended logic circuit.

2.5. Total Reversible Logic Implementation Cost (TRLIC) [4]

This refers to the summation of gate count constant inputs, garbage outputs and quantum cost of the circuit.

3. Basic Reversible Logic Gates

3.1. DPG Gate

It is a 4*4 Double Peres Gate .The input vector is I (A, B, C, D) and the output vector is O (P, Q, and R, S). The quantum cost of DPG gate is 6.

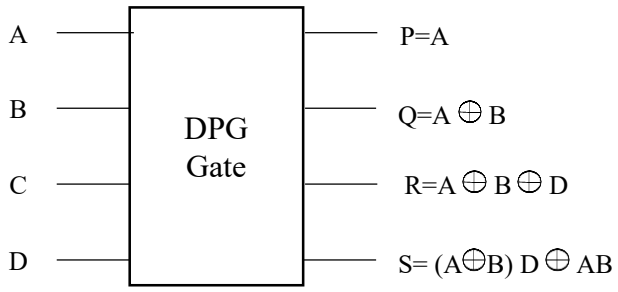

Figure 1. DPG Gate

3.2. MTSG Gate

It is a 4*4 MTSG gate. The input vector is I (A, B, C, D) and the output vector is O (P, Q, and R, S). The quantum cost of MTSG gate is 6. The full adder using MTSG is obtained by C=0 & D=Cin.

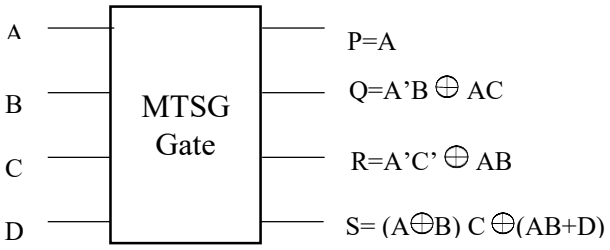

Figure 2. MTSG Gate

3.3. MFRG Gate

Modified Fredkin gate is 3x3 reversible gate. The input vector is I (A, B, C) and the output vector is O (P, Q, and R). The output is P=A, Q=AB'⊕ AC' and R=A'C⊕AB. Quantum cost of Modified Fredkin gate is 4.

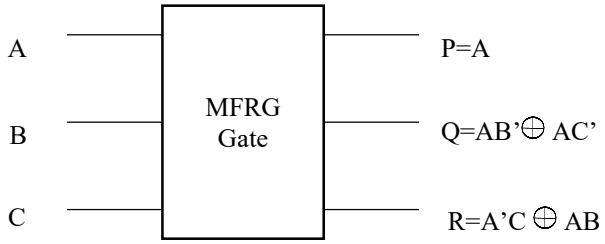

Figure 3. MFRG Gate

4. Proposed Work

A residue number system (RNS) features *i*th residue digit of sum, difference and product is exclusively dependent on the *i*th digits of the operands [5, 7]. In general, to compute a remainder, it is usually to use read-only memories to do residue arithmetic [6]. However, to store all residue arithmetic tables, many read-only memories are required. Residue Number system is a carry-free arithmetic system that enhance the speed of computations, and exhibits fault-tolerant capabilities [12].

Proposed Architecture 1:

DPG & Modified Fredkin based Reversible 4-bit residue ripple adder

Proposed design of 4-bit residue ripple adder using reversible gates is obtained with eight DPG gates and five Modified Fredkin gates. Residue adders are very important components in building residue based- multiplier, residue to binary converters, binary to residue converters and other arithmetic operations. The three input Modified Fredkin gate serves as multiplexer. Quantum cost of reversible Double Peres gate (DPG) is 6 and Quantum cost of Modified Fredkin gate is 4.Architecture of proposed 4-bit residue ripple adder shown in Figure 4. DPG gates is used to generate carry per select stage. Proposed work with low Quantum cost and power consumption as compare to existing work. 4-bit

residue adder designed by using reversible DPG gate and Fredkin gate in existing work. Quantum cost of DPG gate is 6 and Quantum cost of Fredkin gate is 5.

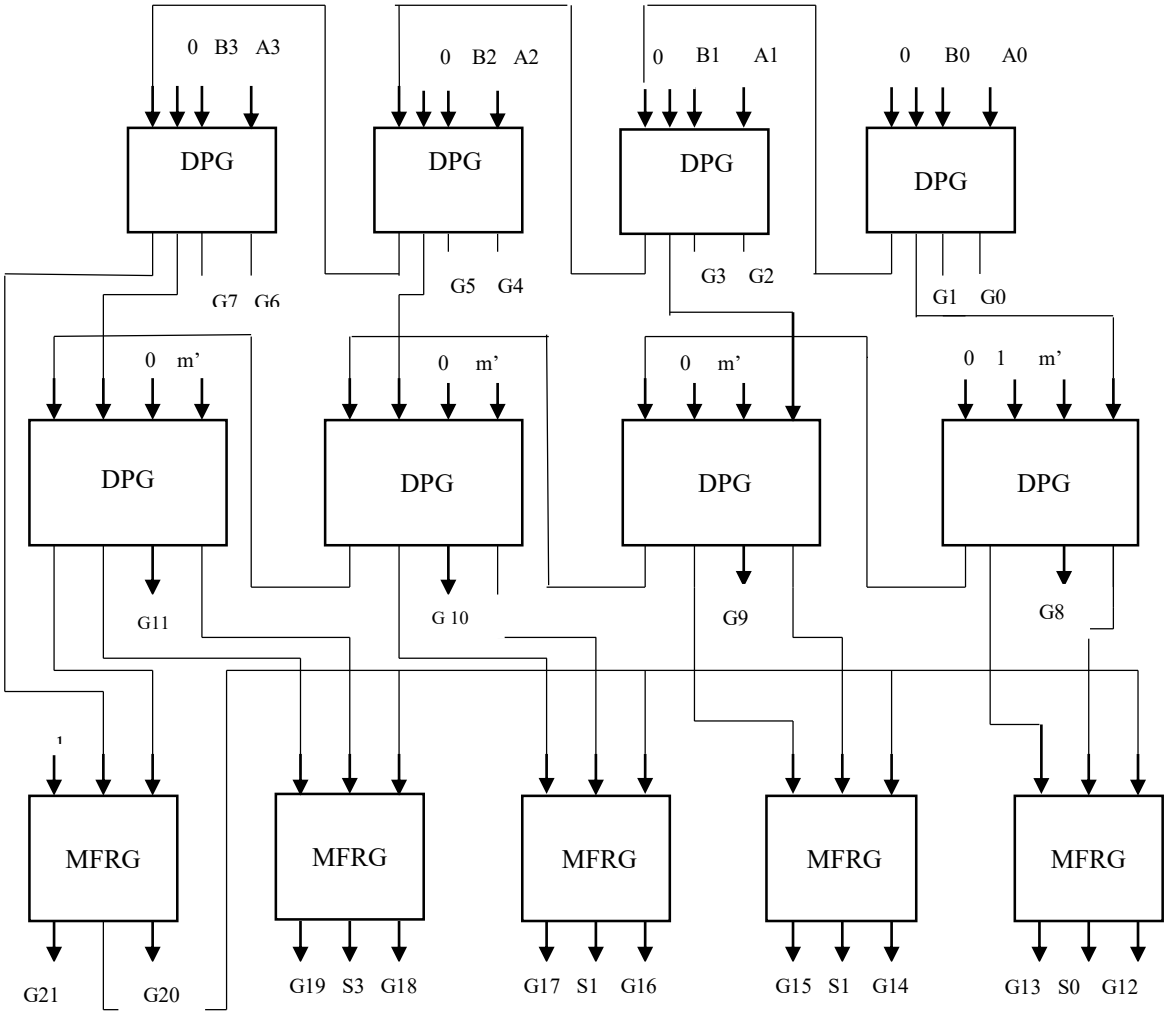

Figure 4. DPG & Modified Fredkin based Reversible 4-bit Residue Adder

Proposed Architecture 2:

Modified TSG & Modified Fredkin based Reversible 4-bit residue ripple adder

Proposed design of 4-bit residue ripple adder using reversible gates is obtained with eight MTSG gates and five Modified Fredkin gates. The three input Modified Fredkin gate serves as multiplexer. Quantum cost of reversible Modified TSG gate is 6 and Quantum cost of Modified Fredkin gate is 4.Architecture of proposed 4-bit residue ripple adder shown in Figure 5. MTSG gates is used to generate carry per select stage. Proposed work with low Quantum cost and power consumption as compare to existing work. 4-bit residue ripple adder is designed by using reversible Modified TSG gate and Modified Fredkin gate in existing work. Quantum cost of TSG gate is 9 and Quantum cost of Fredkin gate is 5.

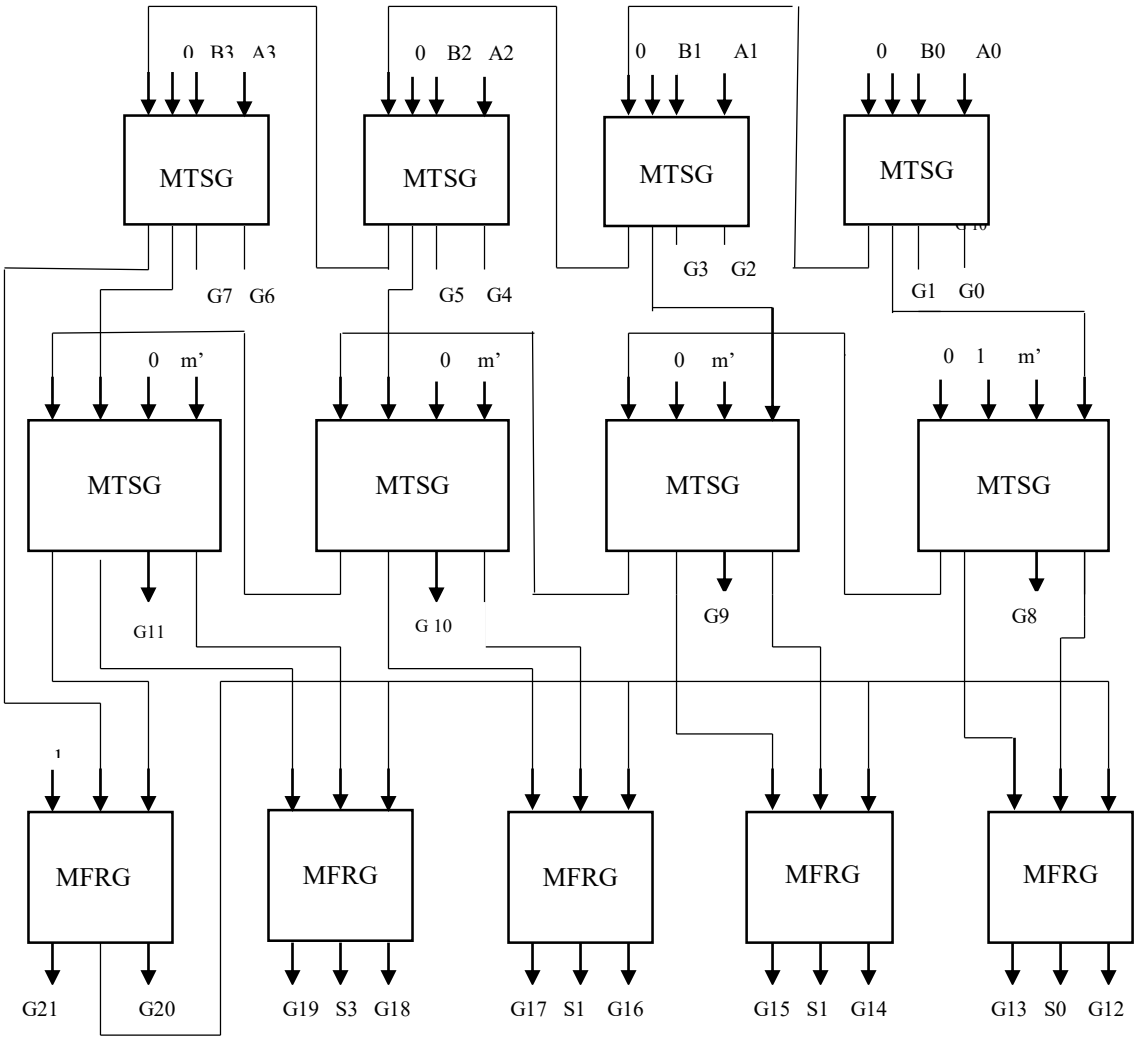

Figure 5. Modified TSG & Modified Fredkin based Reversible 4-bit Residue Adder

5. Simulation Results

Table1. Comparison of Proposed Work with Existing Work

Residue Ripple Adder	Quantum Cost	Power Consumption
Proposed Design (Figure 4.)	68	3.767 W
Existing Design [8]	73	4.247 W
Proposed Design (Figure 5.)	68	2.087 W
Existing Design [8]	97	4.141 W

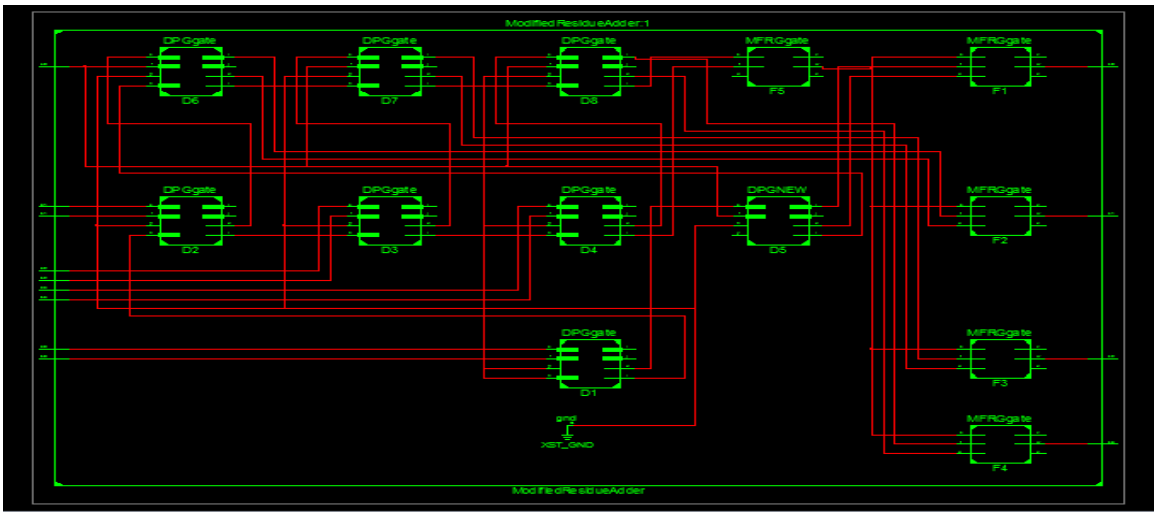

Figure 6. RTL View of DPG & Modified Fredkin based Reversible 4-bit Residue Adder

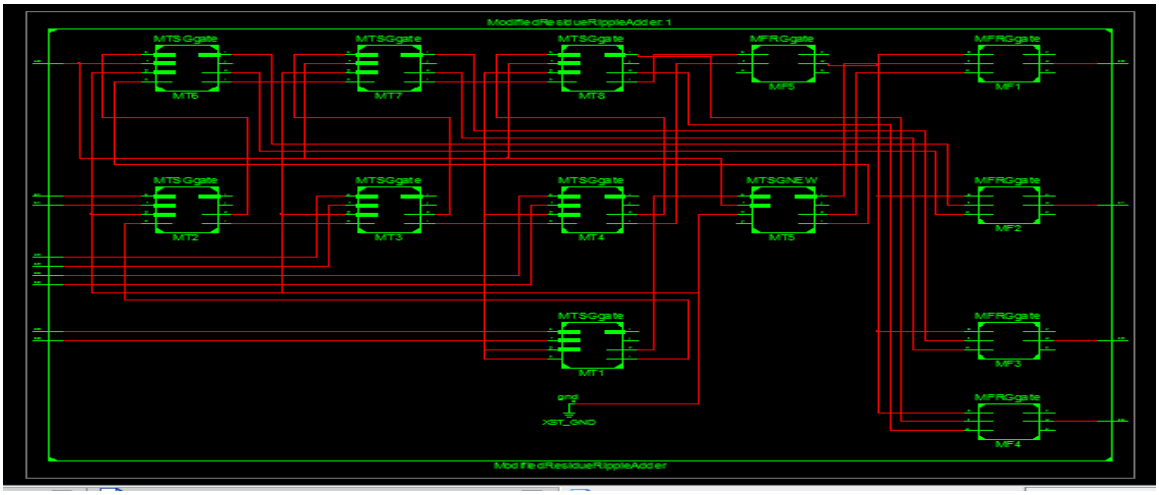

Figure 7. RTL view of Modified TSG & Modified Fredkin based Reversible 4-bit Residue Adder

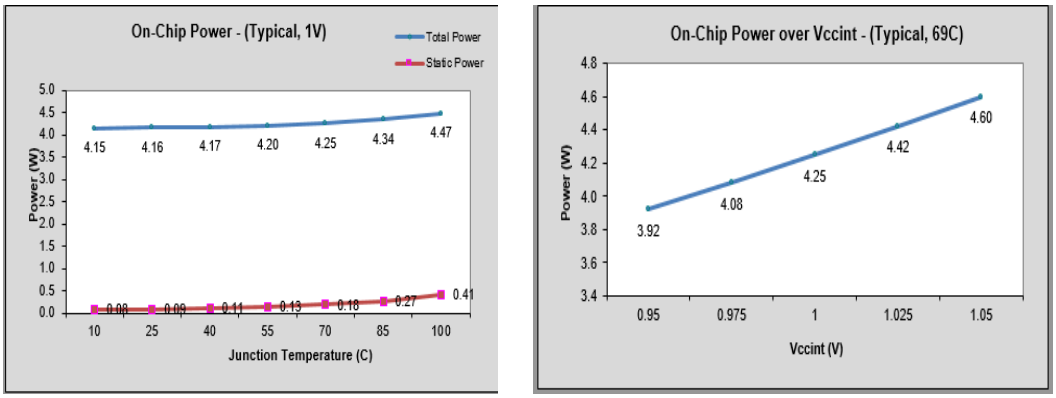

Figure 8. Power Consumption graphs for DPG & Fredkin based Reversible 4-bit Residue Adder

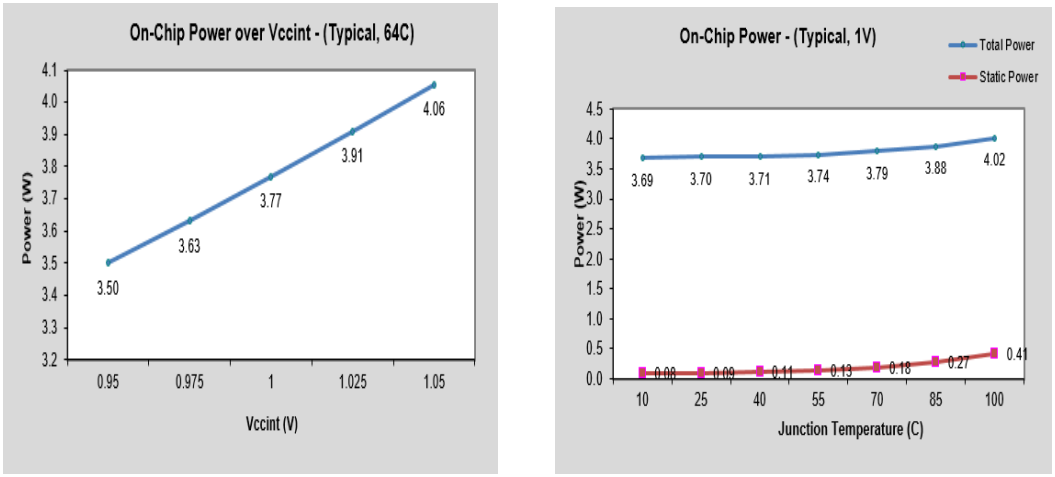

Figure 9. Power Consumption graphs for DPG & Modified Fredkin based Reversible 4-bit Residue Adder

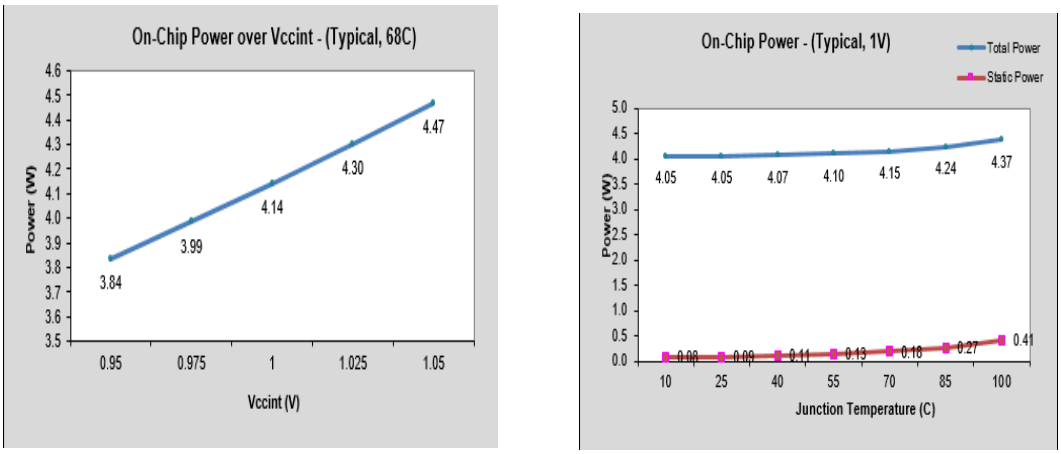

Figure 10. Power Consumption graphs for TSG & Fredkin based Reversible 4-bit Residue Adder

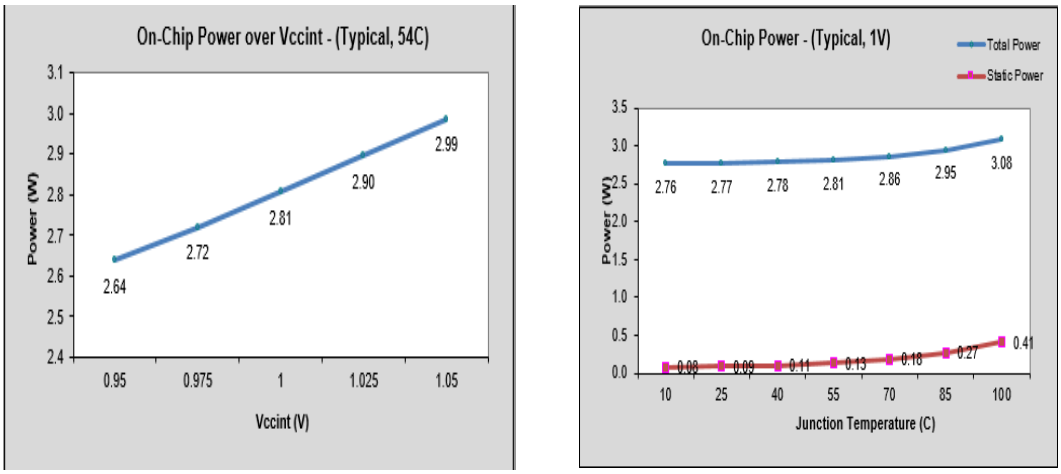

Figure 11. Power Consumption graphs for Modified TSG & Modified Fredkin based Reversible 4-bit Residue Adder

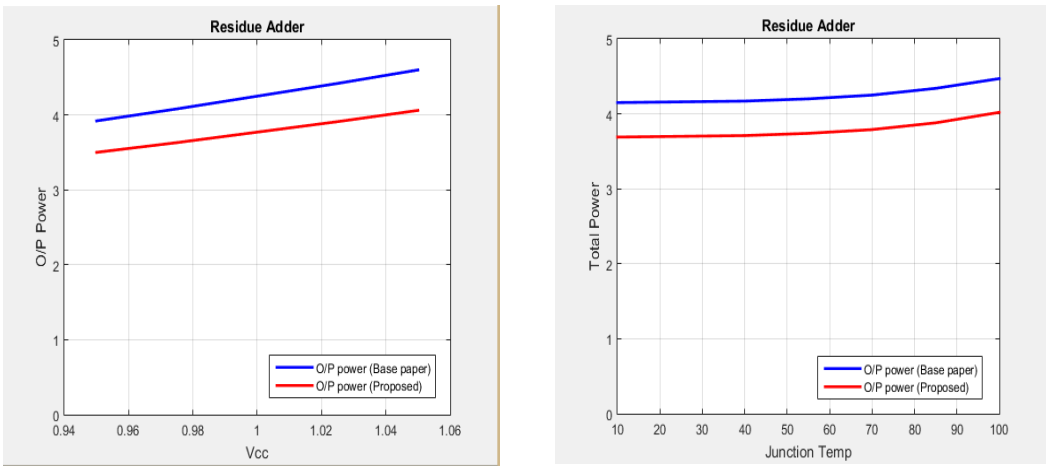

Figure 12. Comparative Results for Power Consumption for proposed Residue Ripple Adder using DPG & Modified Fredkin Gates and existing Results

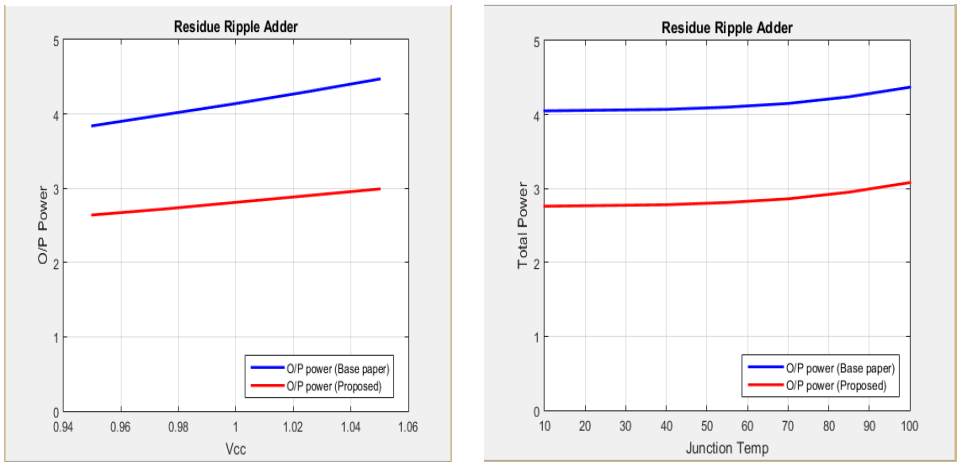

Figure 13. Comparative Results for Power Consumption for Proposed Residue Ripple Adder Using Modified TSG & Modified Fredkin Gates and Existing Results

In the Figure 12. The graph between the Vcc & Output power shows that the proposed design consumes 3.77 watt power while the existing design consumes 4.25 watt power. Similarly the graph between the Junction Temperature & Power shows that the proposed design consumes 3.74 watt power while the existing design consumes 4.28 watt power.

In the Figure 13. The graph between the Vcc & Output power shows that the proposed design consumes 2.81 watt power while the existing design consumes 4.14 watt power. Similarly the graph between the Junction Temperature & Power shows that the proposed design consumes 2.81 watt power while the existing design consumes 4.14 watt power.

Hence it can be concluded that the proposed reversible residue ripple adder design consumes less power than the existing design.

6. Conclusion

In this paper, reversible logic synthesis were carried out for both designs (Figure 4 & 5). The design have been proposed for the ease of reversible logic implementation and it has been found that the proposed designs (Figure 4 & 5) are better than the existing one in terms of quantum cost and power consumption. This work forms an important move in building large and complex reversible combinational circuits**.**

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Authors

Ankush, He was born in India in the year 1991. He received his Bachelor of Engineering in Electronics and Communication from Chandigarh Engineering College, Landran (Mohali), India in 2013 and presently pursuing M.Tech in Electronics and Communication from Punjabi University, Patiala. His main research interests include Low Power VLSI Design and Digital Design.

Amandeep Singh Bhandari, He is an Assistant Professor in Department of Electronics & Communication Engineering (ECE) at Punjabi University, Patiala. His area of specialization is VLSI design, Wireless communication, Antennas. He is member of International Association of Engineers and IIIR. He is a Post Graduate from Thapar University, Patiala in 2010 and has been consistently involved in research work on VLSI and Wireless communications. He is doing Ph.D in "LTE Security" from Punjabi University, Patiala.