International Journal of Hybrid Information Technology
Vol. 9, No.8 (2016), pp. 359-366
http://dx.doi.org/10.14257/ijhit.2016.9.8.31

Design and Analysis of 4 Bit Johnson Counter Using Clock Gating

Sonia Sharma[1] and Neeraj Kr. Shukla[2]

[1]*student (M.Tech. Vlsi Design),*
The Northcap University, Gurgaon, Haryana, India

Abstract

In VLSI design the reduction of power is an important criterion. The performance of a system mainly depends on the method of designing of various blocks of that system. To provide an efficient and meaningful architecture of a VLSI chip, a devoted design is needed which is power serviceable with less intricate. As computer systems have sequential circuit mostly, hence it is very necessary to design a sequential circuit which is more efficient and less power consuming. As different kind of counters are the important segments for different sequential circuits. Here, in paper we have proposed an efficient clock gating 4-bit Johnson counter using low power d flip flop. Power of d-flip flop is reduced by using power gating technique. By doing analysis in cadence at 180nm technology it is counted that our proposed design has lower power consumption i.e. power of the proposed design comes to be reduced by 40.3% which is $62.63e^{-6}$ and the reduced output is $37.4e^{-6}$. This is a great achievement in the VLSI industry than the conventional design, with a little enhancement of delay.

Keywords*: Clock Gating, power gating, Johnson counter, Negative edge, D-Flip flop, virtuoso, power*

1. Introduction

In present days power reduction is one of the most important challenges for VLSI industry. The circuitry and power consumption increased day by day due to the advancement of the devices. Hence the need of power reduction gets increased. Here power gating and clock gating techniques are applied over negative edge triggered d-flip flop and Johnson Counter respectively. Clock gating is a technique used in various sequential circuits to reduce dynamic power. Clock gating reduces power by adding additional logic circuitry to shear the clock tree. Prune the clock deactivate portion of the circuitry so that the flip flops in them do not switch states. Switching states form one to zero and vice-versa again and again consumes more power. Hence by stopping the switching activity the dynamic power get reduce to zero. And the only leakage current can provoked. In the D flip-flop to reduce leakage power and dynamic power, power gating technique is used, and efficient 4 bit Johnson counter is designed.

Johnson counter is a basic ring counter and it is very useful as well, because it provide a very specific loop synchronously, which is very useful for the various logic design[1] MOD is 2n for n inputs. The register cycles through a sequence of bit-patterns. Johnson counter has an advantage that it requires only half the number of flip flops as compared to the conventional ring counter. By disabling clock signal that consumes more power, reduce power dissipation of both its internal node and clock line. Here the effective power reduction is achieved due to less signal switching and reduce leakage power.

In this work analysis of power and delay is calculated by applying clock gating technique. The main circuit area is increased by adding the additional circuitry. The speed and power dissipation performance has been done to analyses merit and demerits of the design. This paper is distributed in the following sections. In section II comparison between low power techniques is mentioned. In section III low power design of D-lip flop

ISSN: 1738-9968 IJHIT

and simulation is mentioned. In section IV conventional design of Johnson counter is described. In Section V proposed design of 4-bit Johnson counter is explained with the truth table .section VI explains derived equations of the clock gating scheme. Section VII explains the simulation work of the proposed design in section VIII results is mentioned. IX section presents conclusion and future scope of the proposed design.

2. Comparison between Low Power Techniques

Clock gating and power gating are the low power techniques used in this paper. Clock gating is applied over the proposed Johnson counter and power gating technique is used to reduce power of the D flip-flop. By clock gating dynamic power is reduced by blocking the extra switching in the flip flops. As switching consumes more power comparatively the whole design. But by clock gating leakage power remain there whenever we are in sleep mode. To reduce leakage power, power gating technique is used .by power gating not only the dynamic power is reduced the supply voltage is also gated [4] that can happen at different points of time.

Table 1. Low Power Strategies [4]

Design level	Strategies
Operating system level	Portioning ,Power down,
Software level	Regularity, Locality Concurrency
Architecture level	Pipelining ,Redundancy ,Data Encoding
Circuit/logic level	Logic styles, Transistor Sizing and Energy Recovery
Technology level	Threshold Reduction, Multi Threshold Devices

3. Low Power Design of D Flip-Flop

Delay flip flop is one of the most important clocked flip-flops as it ensures that two inputs of flip flop would never be same at one time. Power gating technique is used to reduce power of D-flip flop.

D flip flop perform a unique operation that it store the same input as applied over the D terminal as soon as the clock pulse is high. When the clock is low the Preset and the clear inputs get high and the D flip flop store the same data as per the input, so it will not change the data and the output will be the same as the input but after certain delay. There are two additional transistor connected over the design one is header and the second one is footer [4]. A low leakage power PMOS is applied as a header MOS which will be used as sleep or standby mode, NMOS transistor is used as footer MOS, the header and the footer MOS splits the whole design in the two potions *i.e*. Permanent power connected with VDD and the ground cell that can derive the cell and turned off.

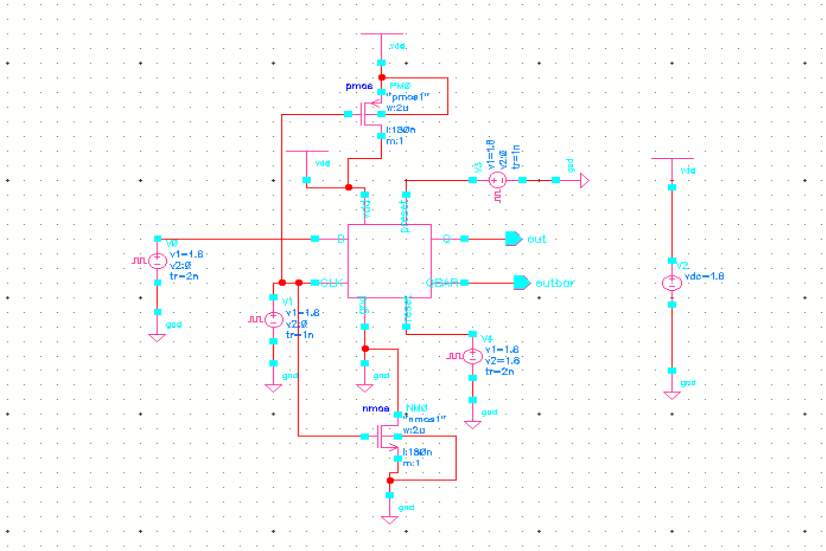


Figure1. Schematic for Power Gating D Flip-Flop

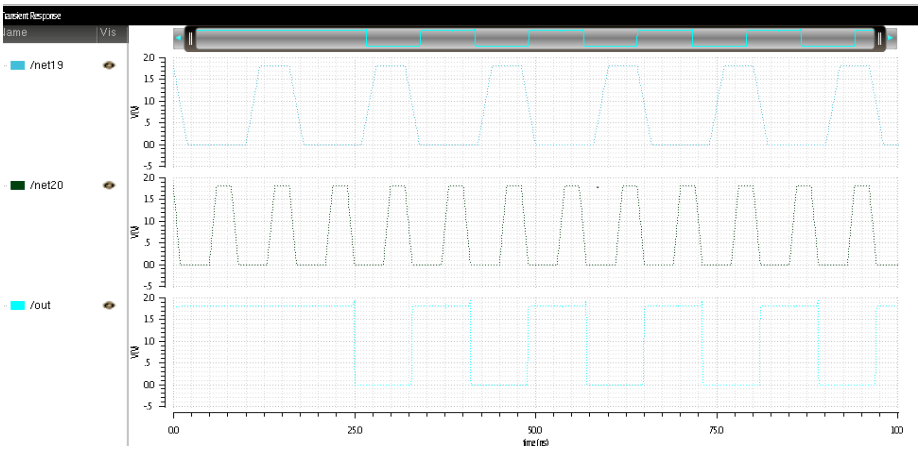


Figure 2. Simulation of Power Gating D- Flip Flop

The power gated d-flip flop is the reduced power flip flop. Power of the conventional d flip flop was 225.2 e^{-6} Watt which was reduced to 89.24 e^{-6} Watt. Hence by using the reduced D-flip flop conventional Johnson counter is designed.

4. Conventional Design of Johnson Counters

Johnson counter is one of the most important Counters used in the digital industry. It a type of ring counter which perform a special sequence of outputs. Conventional Johnson counter consists of 4 master slave d-flip flop connected sequentially. The clock applied on each of the flip flop at the same time. Some power and delay analysis are done with the conventional Johnson counter. The schematic and the waveform are as shown in the Figure 3.

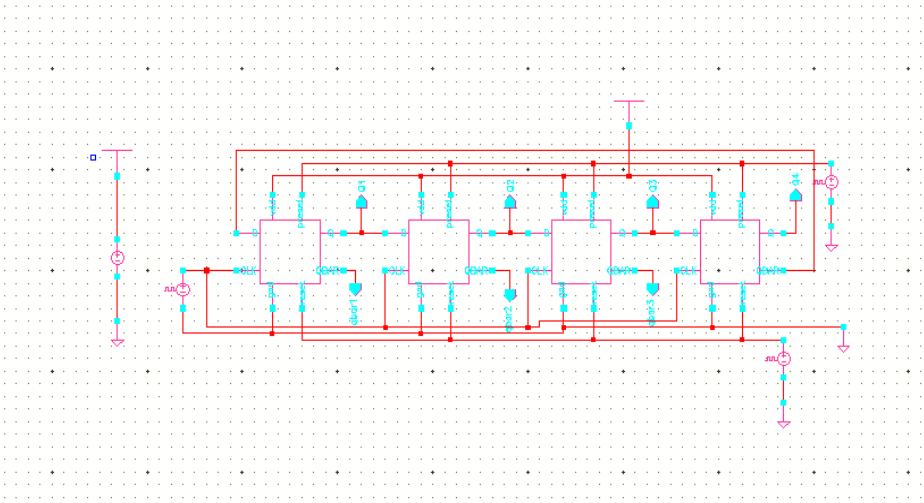


Figure 3. Schematic of Conventional Johnson Counter

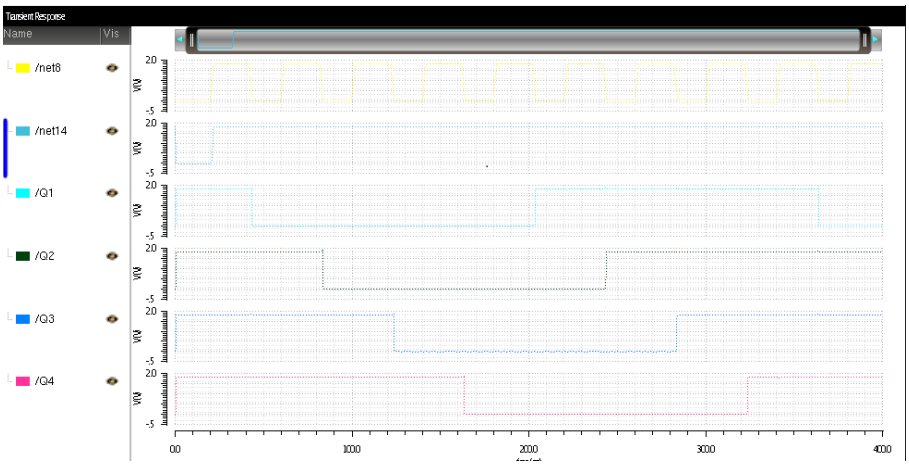


Figure 4. Waveform of Conventional Johnson Counter

5. Proposed Design of Johnson Counter Using Clock Gating Technique

We proposed 4 bit Johnson counter using clock gating technique in clock gating scheme some extra transitions get blocked to reduce the power dissipation. In clock gating scheme clock is applied asynchronously with different frequency and time period.

Derived equations and inputs

$F_1 = f/2$

$Clk_{Q0}=clk_f.clk_{f1}.clk_{f2}$ Eq1

$Clk_{Q1}=clk_f.clk_{f1}'.clk_{f2}$ Eq2

$Clk_{Q2}=clk_f.clk_{f1}.clk_{f2}'$ Eq3

$Clk_{Q3}=clk_{f1}.clk_{f1}'.clk_{f2}'$ Eq4

$F_2=f/4$ Eq5

The above are the relationship between master clock and the clock sequences [1].frequency f1 is the master clock and the frequencies in the lower sequences are the masking clock consist of f_1 and f_2 of the master clock.

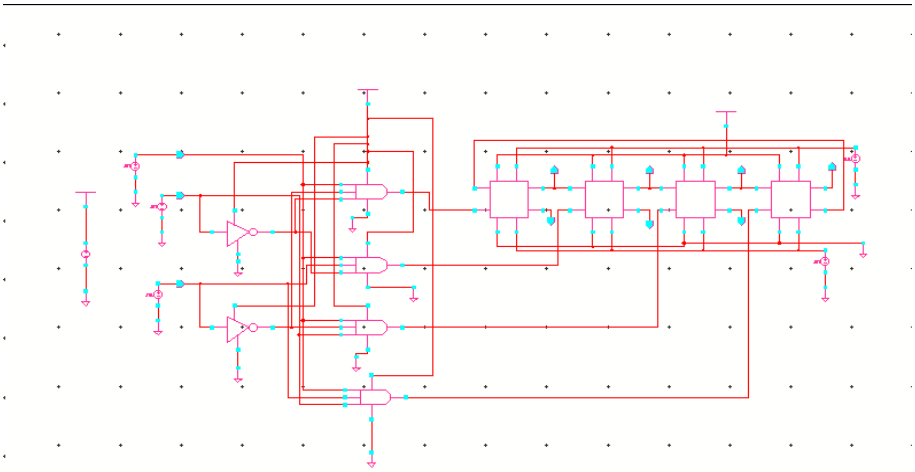


Figure 5. Schematic for Clock Gating Johnson Counter

If number of bit is n, then number of states s_n will be

$S_n=2n$, where n is the number of flip-flops

n = 1,2,3,4,5,6…….2^k

k=0 and positive integers

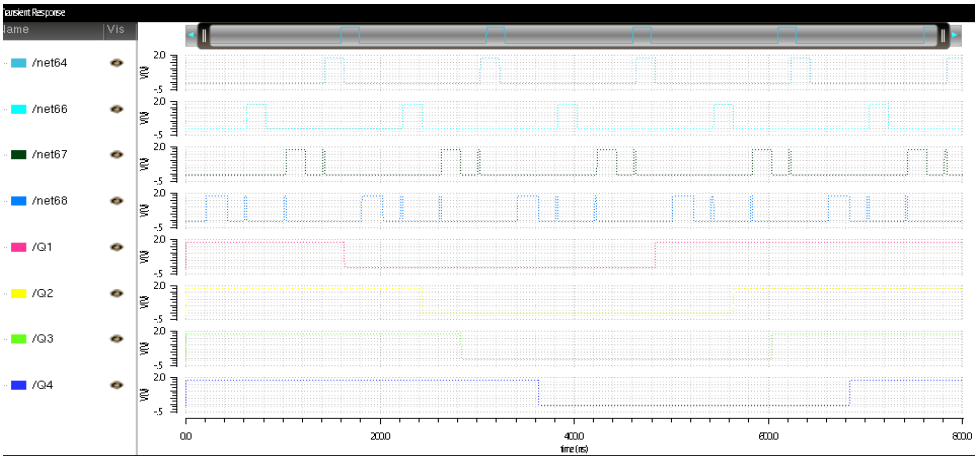


Figure6. Simulation of Proposed 4-Bit Johnson Counter

Table 3. Truth Table for 4 Bit Johnson Counter

State	Q4	Q3	Q2	Q1	Clock pulse
S1	0	0	0	0	1
S2	1	0	0	0	2
S3	1	1	0	0	3
S4	1	1	1	0	4
S5	1	1	1	1	5
S6	0	1	1	1	6
S7	0	0	1	1	7
S8	0	0	0	1	8

6. Simulations

Simulation of our proposed design and the conventional design in cadence Cadence Virtuoso IC6 with 180nm technology .Simulations have been run for 4 bit Johnson counter, power gating D-Flip flop and clock gating 4 bit Johnson counter. Both the simulation are analyzed and compared to discuss the advantage and power dissipation of both the circuitry.

Our proposed system is a negative edge triggered system. The outputs get change only when the negative edge of the clock appears. Negative edge is applied to remove glitches in the Outputs [2].

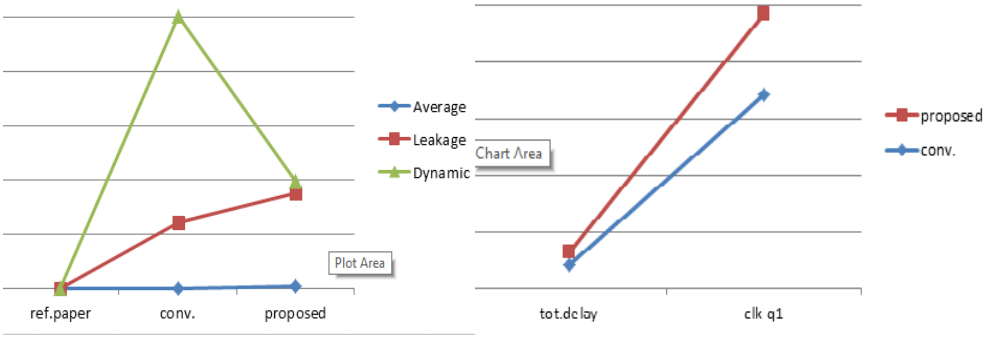
Figure 6 represents the simulation of clock gating 4-bit Johnson Counter; Figure 4 shows the working of the conventional design. In conventional schematic all the clock pulses are synchronous, they do not have any delay in between the clock input, master slave D flip-flop are here implemented for shifting the data from right to left. It is observed that data is shifting unnecessary most of the time only two shifts are necessary for the counter. By clock gating the extra transitions are blocked so as to reduce the power consumption, as shown in Figure 6 that blocks get the clock pulse when it require the transitions. Theoretically total of 40% of power get reduced in proposed design, with a negligible increment in delay. It is observed that overall power consumption get reduced in proposed design of clock gating including the power gating.

7. Results

As shown in Table 4 the outputs are shown. The power of the proposed design comes to be reduced by 40.3% which is $62.63e^{-6}$ and the reduced output is $37.4e^{-6}$. This is a great achievement in the VLSI industry. There are some trades off also present *i.e*. they delay in overall circuitry get enhanced .the design get large in size so only desk application can be created.

Table 4. Results of the Conventional and Proposed Design

Parameters		**Reference paper[2]**	**Conventional**	**Proposed design**
Power (Watt)	Average	14.5% Reduced	62.63 e^{-6}	37.40 e^{-6} (40.1%Reduced)
	Leakage	-	12.3 e^{-6}	17 .62 e^{-6} (43.2% Hike)
	Dynamic	-	50.33 e^{-6}	19.87 e^{-6} (60.5% Reduced)
Circuit delay(Sec)		-	42.32 e^{-9}	342.7 e^{-9}
SNM		-	0.8	0.6
Clock to Q delay(Sec)		-	22.66 e^{-9}	142.7e^{-9} (120.04% Hike)



Power Comparison **Delay Comparison**

It is noticed that our research work is a major contribution in the VLSI industry future research is suggested to develop a more power efficient clock gating system for not only the Johnson counter but also other design [2].

8. Advantages of Virtuoso Cadence

Here in this work we used Cadence Virtuoso IC6 with 180nm technology. Here are some advantages of cadence tool over the other tools.

Miniature size and low profile.

Extended operating temperature range -40 ºC to+ 125ºC.

AEC-Q200 qualified.

TS16949 certified production lines.

Acknowledgments

I would like to thank Dr. Neeraj Shukla, (Associate Professor, Department NCU Gurgaon) for his continuous guidance and incitement and guidance. I am also thankful to Ms. Rakhi Nangia, (Assistant professor) NCU Gurgaon, Mr. Rajesh Yadav, (Lab Engineer NCU Gurgaon) for their continuous encouragement technical and personal level. I would also like to thank my family for their constant support and encouragement.

References

[1] S. M. Ismail, S. Rahman, M. M. Rahman and N. S. Ferdous, "A Design Scheme of Toggle Operation Based Johnson Counter with Efficient Clock Gating", International Conference on Computational Intelligence, Modelling and Simulation, Kuantan, **(2012)**, pp.393-399, 25-27.

[2] S. Md. Ismail, A. B. M. Saadmaan and F. Tamanna Islam, "Low Power Design of Johnson Counter Using Clock Gating", ,Computer and information technology(ICCIT), 2012 December 15th international conference ,Chittagong, **(2012)**, pp.510-517,22-24.

[3] J. Shinde and S.S. Salankar, "Clock Gating- A Power Optimizing Technique for VLSI Circuits", Annual IEEE India Conference, Hyderabad, **(2011)**, pp.1-4, 16-18.

[4] K. Kaur and A. Noor, "Strategies & Methodologies For Low Power VLSI Designs: A Review", International Journal of Advances in Engineering & Technology, International Journal of advances in engineering & technology, **(2011)**, pp.159-165.

[5] A. Abba and K. Amarender, "*Improved Power Gating Technique for Leakage Power Reduction*", International Journal of Engineering and Science, vol.4, **(2014)**, pp.6-10,

[6] S. Sujitha and K. Rafha, "*Design of Low Power Flip Flop Using Clock Gating and Power Gating*", international Journalof engineering science and computers, **(2015)**, pp. 1152-1157.