International Journal of Hybrid Information Technology
Vol. 9, No.6 (2016), pp. 117-126
http://dx.doi.org/10.14257/ijhit.2016.9.6.10

Low Leakage Asynchronous PP based Single Ended 8T SRAM bit-cell at 45nm CMOS Technology

Sonam Jain[1] and Neeraj Kr. Shukla[2]

[1]PG Student, [2]Associate Professor
VLSI Design Group, Department of Electrical, Electronics & Communication Engineering, THE NORTHCAP University, Gurgaon (Haryana) India
[1]sonamjn98@gmail.com [2]neerajkshukla@ncuindia.edu

Abstract

Low power SRAM memory designs has become challenging for portable device applications. Semiconductor/ VLSI industry growth has exponentially demanding low leakage power SRAM designs for high performance chips and microprocessors. To get optimized standard cell memory design for battery operated devices at deep sub micron CMOS technology, a low leakage Asynchronous 8T SRAM is proposed. In this paper gated–ground P-P based low leakage 8T SRAM bit cell design is proposed for reducing the standby leakage power dissipation. The Proposed 8T SRAM bit - cell has used single bit line (single voltage source) for reading and writing operations to reduce active power consumption. The reduction of voltage swing and low standby leakage results appreciable reduction in total power consumption of the proposed design. The SPECTRE simulation and analysis at a 45nm CMOS feature size shows significant results in the proposed design at 0.7v supply voltage. Proposed Asynchronous single ended 8T SRAM bit - cell greatly reduced 99.92% stand by leakage power consumption and 11.76% of write '1' active power consumption from the existing 8T SRAM bi – cell design. Whereas comparing with the standard 6T SRAM bit – cell design, proposed design also achieved 99.88% standby leakage power reduction and 95.8% of total active write '1' power consumption from the conventional 6T SRAM bit – cell. This results overall total average power reduces in the proposed 8T SRAM bit-cell design i.e. reduction of 99.93% from the existing 8T SRAM bit – cell and 80.63% from the conventional 6T SRAM bit – cell design while keep maintaining the read static noise margin and write noise margin.

Keywords*: Aspect ratio, CMOS technology, Low power, SRAM bit-cell, stacking effect, standby leakage, VLSI chips*

1. Introduction

A high performance VLSI chip prefers SRAM based cache which increases the speed of data flowing in the circuit so system speed increases. Dynamic power dissipation is the main concern of the total power dissipation at above 180nm CMOS technology, but as scale down the CMOS technology, leakage power dominates and degrades the performance of the chip according to the survey of ITRS (international technology roadmap for semiconductors)[2].

Liang Wen presented [1], single ended, robust 8T SRAM cell for low voltage operation. Single bit-line scheme has been used to achieve write and read operations by which read and write stability improves. This work has carried out at ultra low voltage which results power dissipation reduces also. In [2], Neeraj Kr. Shukla has presented a novel architecture *i.e*. P3 SRAM bit-cell for Experimental result shows that given design dissipates less leakage comparative to the conventional 6T SRAM bit-cell.In [3] Deepak Mittal has discussed leakage reducing the power consumption. In this work mainly focus

ISSN: 1738-9968 IJHIT

on the active and standby leakage power for reducing the total power dissipation in the cell. power reduction. In this work power gating techniques are applied in sense SRAM amplifiers for decreasing the leakage power. Additionally which is also contributes in the total power consumption that is also reduced. This technique is very efficient and reduces total power dissipation approximately 99% than other techniques. In [12], Shilpi Birla has discussed about stability parameter with the leakage power in the SRAM bit cell. In this work, a novel PP based 9T SRAM cell has presented for the better stability and reduced leakage power to the existing design of the 6T SRAM cell and the 8T SRAM cell.

2. Conventional 6T SRAM bit – cell design

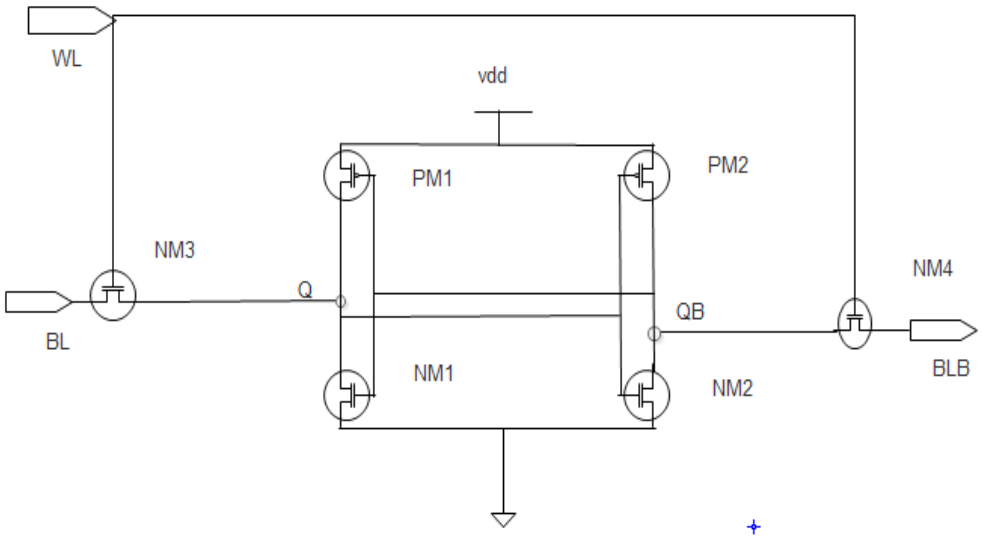

Figure 1. Schematic of conventional 6T SRAM bit – cell

In the conventional 6T SRAM design, operations are performed when the word line(WL) is asserted. Operations are performed by two opposite inverter pairs through I/O ports. In the conventional 6T SRAM bit – cell, two bit lines are used; BL (bit line) and BLB (bit line bar) for performing the operations in the 6T SRAM bit – cell design. Q and QB are the output storage ports in the Figure [1].

Basically 3 types of operations are performed.

A. Write operation

For write '1' at the storage node Q, BL passes '1' to the storage node Q when WL asserts. Due to the two opposite inverter pairs action, data bit will flip on the another storage node of the cell. So, '0' is stored on the storage node QB. To write data bit '0', zero will pass by the BL to the storage node Q.

B. Read operation

Read operation is also performed when BL and BLB are in precharge state. When WL enables, Stored data in the SRAM cell is shown by the output ports (Q and QB).

C. Hold operation

In this operation, word line is disabled. Stored data hold by the inverter pairs transistors. No switching action occurs in this standby mode.

In this conventional 6T SRAM bit – cell design, leakage power dissipation becomes the major issue as we scales down the CMOS technology. Due to which total power consumption in the design will increase and affects other performance parameters.

3. Existing 8T SRAM bit – cell design

In this figure [2], single ended 8T SRAM bit – cell is presented. In this design, read – write operations are performed by single bit – line. Read noise margin is enhanced by the cutting off the positive feedback loop of the two opposite asymmetrical inverter pair.

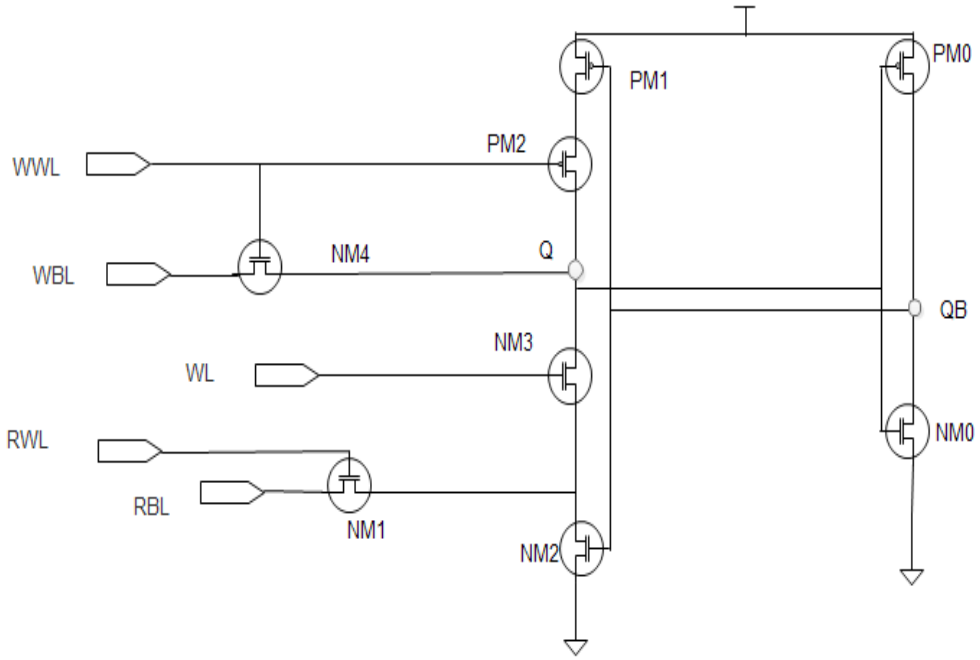

Figure 2. Schematic of existing 8T SRAM bit – cell

In this existing 8T SRAM bit – cell read and write operations are held when the WL (Word Line) goes low. For read and write mode, RWL (Read Word Line) and WWL (Write Word Line) must be enabled high respectively. In case of write data bit '1', this design limits to write data bit '1' because of weak '1' pass by NMOS to the storage node in the cell. But it is overcome by using the assist techniques. After passing data bit '1' to the storage node, WWL goes off and design comes in the standby mode so data bit '1' reached to approximately VDD level.
Read operation is held by RWL goes to high. With that RBL (Read Bit Line) enables. Stored data bit can read on output nodes (Q and QB) in Figure [2].

4. Proposed Asynchronous Single Ended 8T SRAM bit – cell

The proposed design is operated at low voltage at deep sub – micron CMOS technology. In this proposed work integrated approach is applied for low power consumption design. For reducing active power consumption, low voltage and Single Ended bit line is used when the memory is operational (active mode). And gated – ground PMOS are employed to lower the gate leakage current and full supply body biasing scheme is applied to lower the sub threshold leakage current.

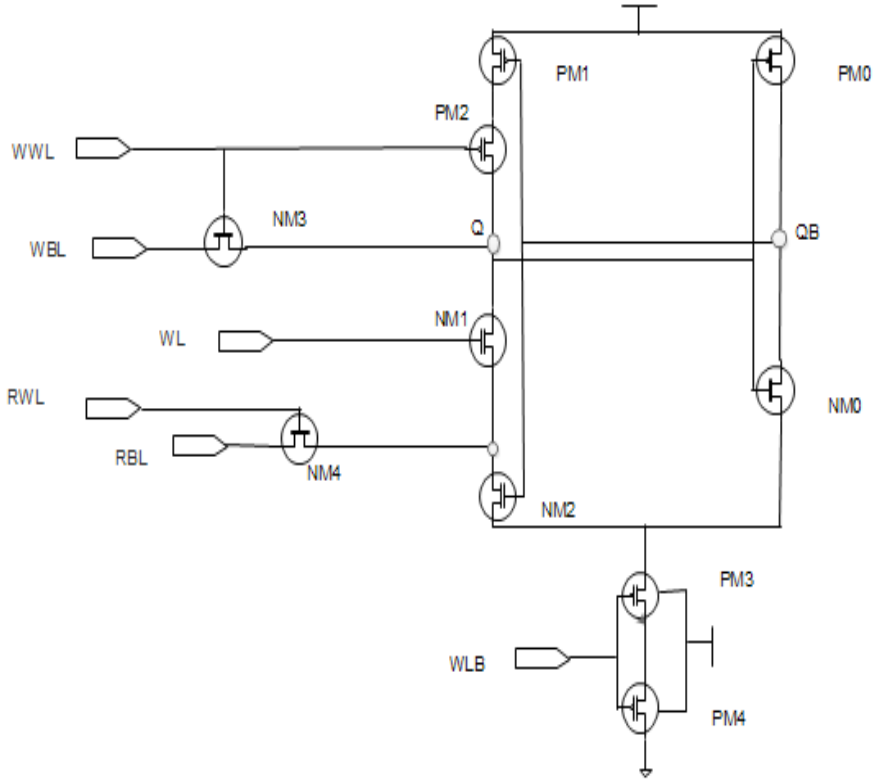

Figure 3. Schematic of Proposed Asynchonous Single Ended 8T SRAM bit – cell

Due to this total standby leakage reduces. When the proposed cell is in active mode, gated-ground PMOS are turned off. So, series stacking effect of the two PMOS (PMOS placed between cell and ground) reduces the leakage which effect in stable and increased read noise margin where storage node does not floats. When the cell is in standby mode (WLB = 0), sub threshold leakage reduces with the gate - ground PMOS are turned on and full supply body bias reduces gate leakage currents. Due to reduction of active and standby leakage dissipation in the cell, total power consumption of the cell is greatly reduced.

WL (Word Line) is active low for read and write operation. While active high during hold mode and WLB (Word Line Bar) is vice – versa. To enable the read and write mode, RWL (Read Word Line) and WWL (Write Word Line) will be active high respectively.

4.1. Write Operation with Single Bit Line

When the cell is in write '1' mode, WL is active low (WL=0) and WLB will be active high, with the WWL is asserts. After asserting WWL, WBL is also enables. Transistors NM1 and PM2 are turned off so due to this WBL is directly transferred data bit '1' to the storage node Q via NM3 transistor. In this write operation, storage nodes Q and QB do not tolerate any disturbance problem because of the single bit line scheme by which positive feedback loop of the cross coupled inverter is cut off by transistors NM1 and PM2 which enhances the noise margin [1]. Due to weak 1 pass through NM3, storage node could not reach at VDD level. But by employing assist techniques and stacking effect, successfully data bit '1' write in the proposed bit – cell when cell enters into standby mode. Due to low leakage by the gated - ground PMOS transistors (PM3 and

PM4) with full supply body biasing, storage node easily reached to VDD level in the inactive mode. While writing data bit '0' in the memory cell, it is normally achieved because the strong 0 pass by NMOS (NM3).

4.2. Read Operation with Single Bit Line

WL is active low with the RWL goes to high. After enabling RWL, RBL goes to VDD level.WLB is active high. Now stored data is passing through the transistors NM2 and NM4 to the output nodes. By enabling the non destructive read operation *i.e.* (transistor NM1 is turned off), the dedicated read path temporally decouples from the storage nodes [1]. In this proposed design, read data bit '0' not floats much because leakage current is lowered here. So accumulation of charge at storage nodes is very less.

5. Analysis and Simulation Work

5.1. Operation Performance in the Proposed Design

Table 1. Operation Performed in the Proposed Asynchronous Single Ended 8T SRAM bit cell

WL	1	0	0	0
WLB	0	1	1	1
WWL	0	1	1	0
WBL	0	0	1	0
RWL	0	0	0	1
RBL	0	0	0	1

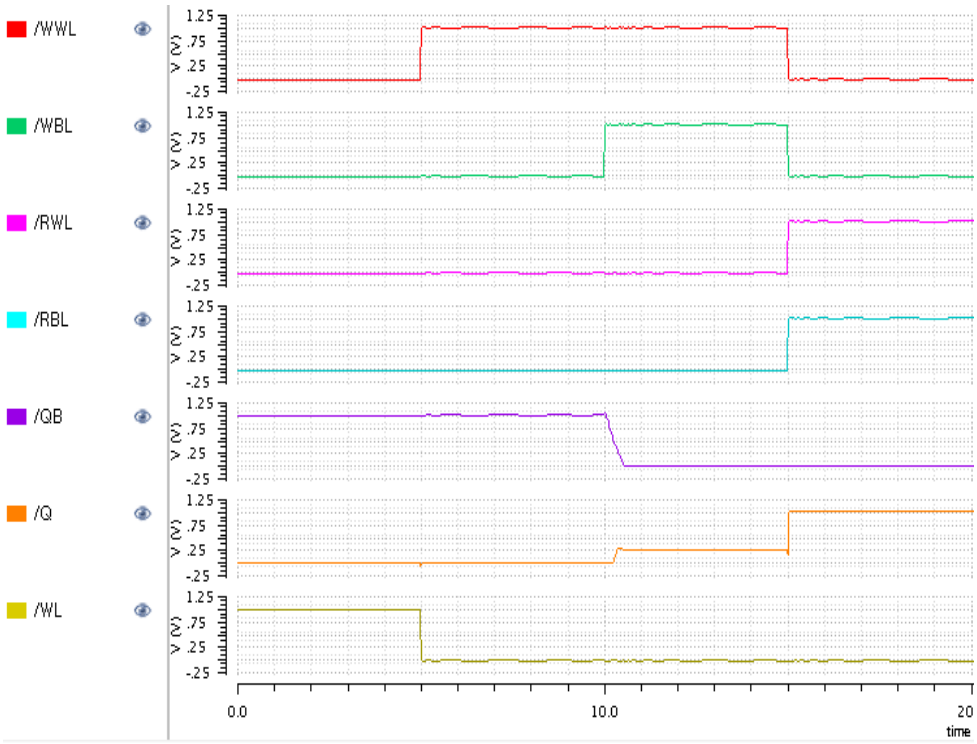

Figure 4. Waveform of the Operation Held in Proposed 8T SRAM Bit Cell

In this Figure [4], operational waveform occured; Hold, Write '0',Write '1'and Read operation in the proposed SRAM bit – cell at voltage supply 1v.

5.2. Leakage Power Dissipation

Table 2. Stand By Leakage Power Dissipation

VOLTAGE SUPPLY	CONVENTIONAL 6T SRAM CELL	EXISTING 8T SRAM CELL	PROPOSED 8T SRAM CELL
1.8V	3.44E-05	5.37E-05	1.75E-08
1.5V	1.28E-05	1.88E-05	3.30E-09
1V	3.96E-07	5.32E-07	1.23E-10
0.8V	4.40E-08	6.25E-08	2.81E-11
0.7V	1.10E-08	1.67E-08	1.31E-11

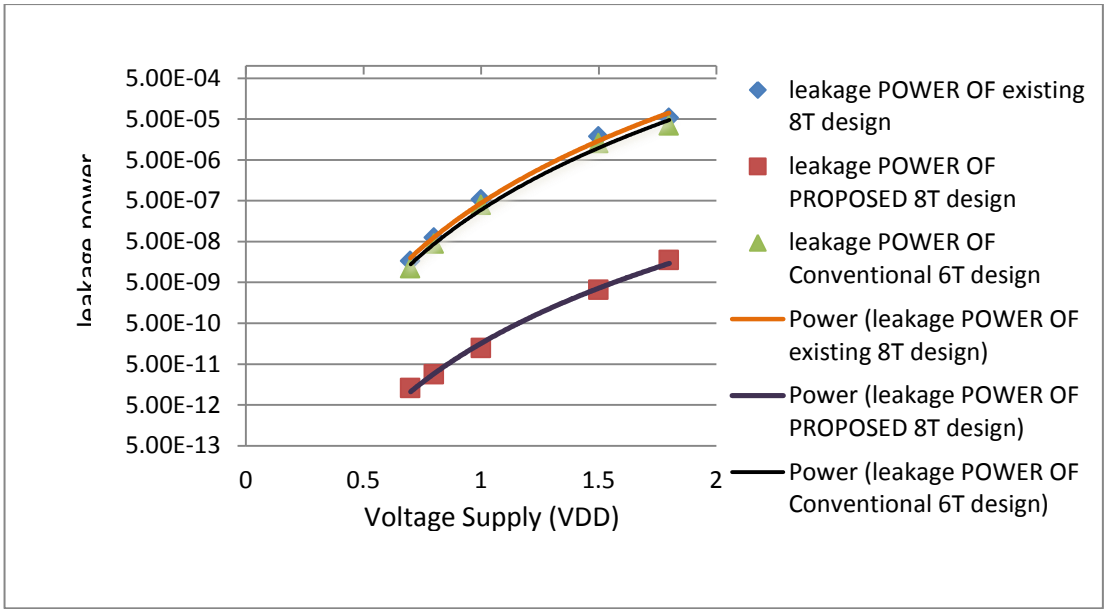

Figure 5. Comparison between Standby Leakage Power of Conventional 6T, Existing 8T and Proposed 8Tdesign at 45nm CMOS Technology

The proposed design achieves 99.92% standby leakage power reduction from the existing 8T SRAM cell design at 0.7volt voltage supply. Along with proposed SRAM bit cell achieves 99.88% standby leakage power reduction from the conventional 6T SRAM cell at 0.7volt voltage supply.

5.3. Write '1' Power Consumption

From Figure [6] shows Power Consumption for writing data bit '1' of conventional 6T SRAM bit cell, existing 8T SRAM bit cell and the proposed P-P based single ended 8T SRAM bit cell at different voltage supply is given.
Also Figure [7] shows the result of active power consumption to write '1' at 0.7v supply voltage. LINE 1 and LINE 2 shows in Figure [7] that proposed cell reduces active power consumption 11.76% from the existing 8T SRAM bit cell and also reduced 95.8% power consumption from the conventional 6T SRAM cell design respectively.

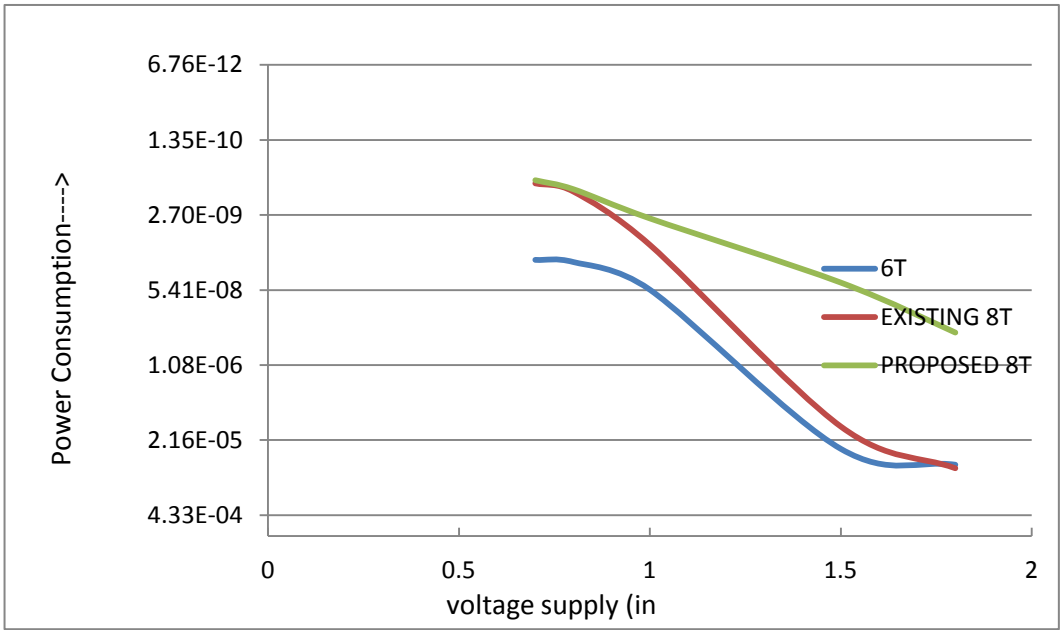

Figure 6. Write '1' Active Power at Different Voltage Supply of Different Memory Cells

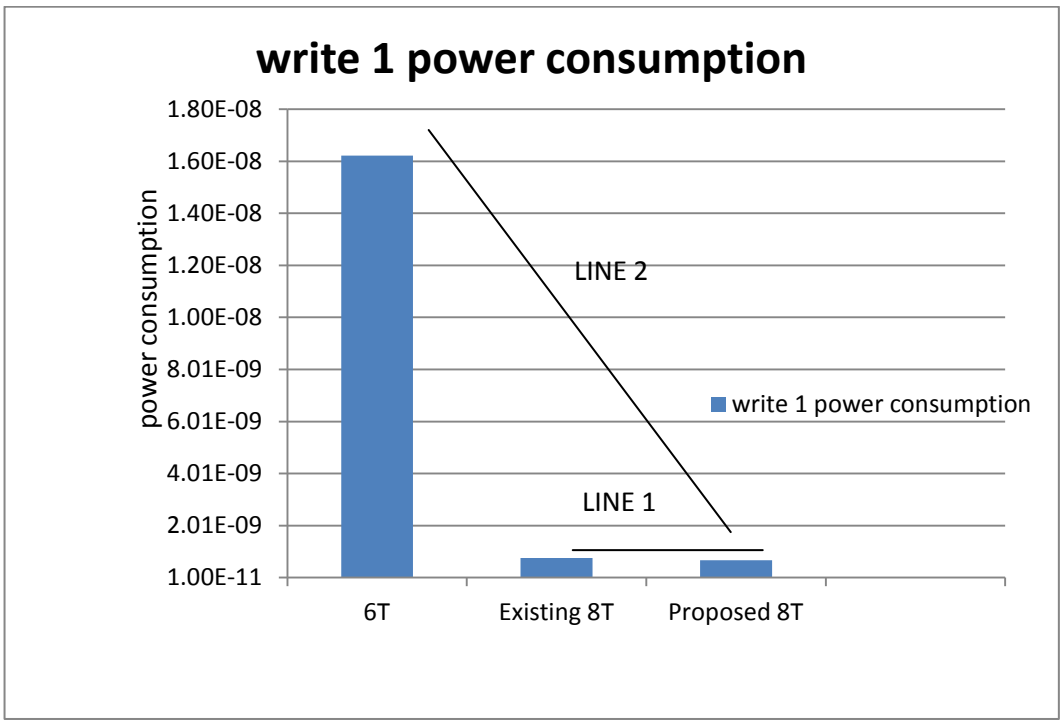

Figure 7. Write '1' active power consumption in the different memory cells at 0.7volt power supply

5.4. Total Average Power Consumption

Table 3. Total Average Power Consumption

VOLTAGE SUPPLY	CONVENTIONAL 6T SRAM CELL	EXISTING 8T SRAM CELL	PROPOSED 8T SRAM CELL
1.8V	4.32E-05	3.90E-05	1.67E-08
1.5V	1.62E-05	1.84E-05	9.51E-09
1V	3.02E-08	7.76E-06	6.74E-09
0.8V	1.21E-08	3.72E-06	2.74E-09
0.7V	1.12E-08	1.84E-06	2.15E-09

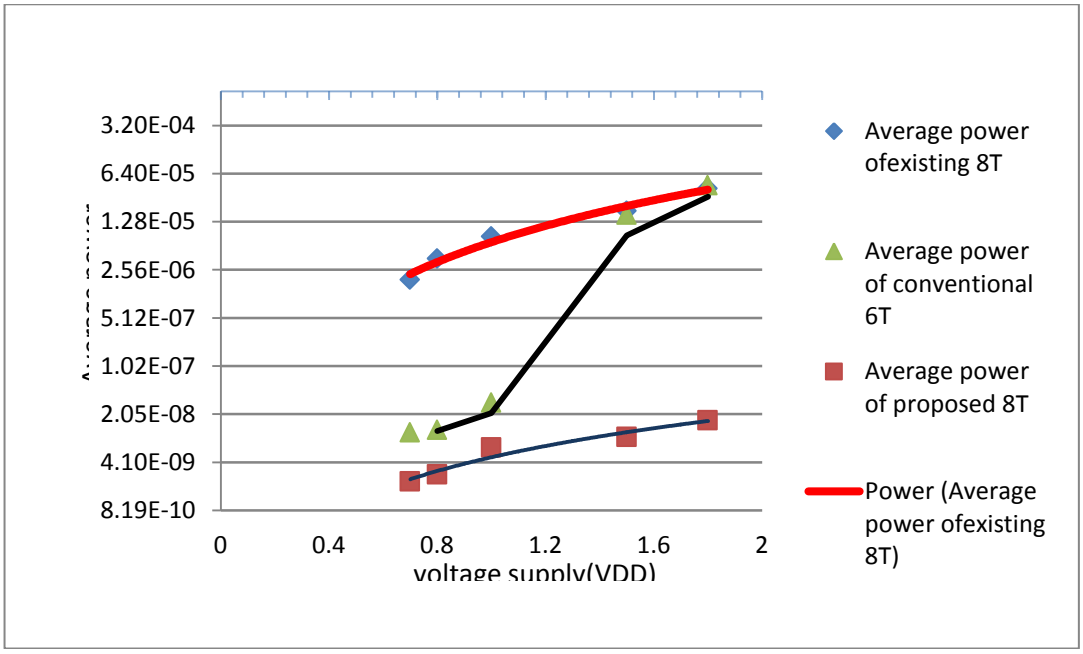

Figure 8. Comparison between Average power of conventional 6T, existing 8T and proposed 8Tdesign at 45nm CMOS technology

Experimental result shows that the proposed 8T SRAM bit cell design reduces 99.93% of total average power from the existing 8T SRAM design and 80.63% from the conventional 6T SRAM bit cell at 0.7volt voltage supply.

5.5. Stability Analysis

Stability calculated by N-curve analysis. In this work, Read Stability of proposed 8T SRAM bit cell is similar with the existing 8T SRAM bit cell. But write ability of proposed cell is increased 0.5% from the existing 8T SRAM cell at 0.7v supply voltage. Conventional 6T SRAM bit cell has very less stability compare to proposed design at 0.7v at 45nm CMOS technology.

6. Conclusions

In this paper, Low Leakage Asynchronous Single Ended 8T SRAM bit cell is proposed. The proposed design utilizes an integrated approach gated – ground PMOS with full supply body biasing. Experimental result shows that the proposed 8T SRAM bit cell design at 0.7volt voltage supply, achieved 99.92% standby leakage power

reduction from the existing 8T SRAM design and 99.88% standby leakage power reduction from the conventional 6T SRAM cell. Also reduces write '1' active power consumption 11.76% from the existing SRAM bit cell and 95.8% power consumption from the conventional 6T SRAM cell design. So that proposed design achieved total average power consumption 99.93% from the existing 8T design and 80.63% from the conventional 6T SRAM cell. Along with this proposed 8T SRAM bit cell Area and delay are compromised in the proposed single ended asynchronous 8T SRAM bit cell.

7. Future Scope

Area can be optimized in the proposed Low Leakage Asynchronous Single Ended 8T SRAM bit cell with reduced delay. There are many area reduction techniques available. By employing appropriate technique in the proposed design, area can be improved along with stability while maintaining the other parameters in the memory cell.

References

[1] L.Wen, Z. Li and Y. Li, "Single-ended, robust 8T SRAM cell for low-voltage operation", Microelectronics Journal, vol. 44, **(2013)**, pp. 718–728.
[2] N. K. Shukla, R. K. Singh, and M. Pattanaik, "A novel approach to reduce the gate and sub-threshold leakage in a conventional SRAM bit-cell structure at deep-sub micron CMOS technology", International Journal of Computer Applications (IJCA), vol. 23, no. 7, **(2011)**, pp. 23-28.
[3] D. Mittal and T. Vigneswaran, "Leakage reduction using power gating techniques in SRAM Sense Amplifiers", Asian Research Publishing Network (ARPN) Journal of Engineering and Applied Sciences, vol. 10, no. 7, **(2015)**, pp. 2994-3000.
[4] N. Rahman and B. P. Singh, "Design of Low Power Sram Memory Using 8T SRAM Cell", International Journal of Recent Technology and Engineering (IJRTE), vol. 2, **(2013)**, pp. 23-27**.**
[5] S. Reddy and S.Chintala, "Stability Analysis of 8T SRAM cell at ultra low voltage", International Journal for Technological Research in Engineering (IJTRE), vol. 2, **(2014)**, pp. 260-264.
[6] A.-T. Do, Z.-H. Kong, K.-S. Yeo and J. Yung Shern Low, "Design and Sensitivity Analysis of a new Current-Mode Sense Amplifier for Low-Power SRAM", IEEE Transactions on Very Large Scale Integration (VLSI) systems, vol. 19, no. 2, **(2011)**, pp. 196-204.
[7] E. Grossar, M. Stucchi and K. Maex, "Read Stability and Write-Ability Analysis of SRAM Cells for Nanometer Technologies", IEEE JOURNAL of Solid-State circuits, vol. 41, no. 11, **(2006)**, pp. 2577-2588.
[8] S. Kaur and A. Kumar,"Analysis of Low Power SRAM Memory Cell using Tanner Tool", International Journal of Electronics & Communication Technology (IJECT), vol. 3, **(2012)**, pp. 80-84.
[9] S. Jadav, Mr. Vikrant and M. Vashisath, "Design And Performance Analysis of Ultra Low Power 6t Sram using Adiabatic Technique", International Journal of VLSI design & Communication Systems (VLSICS) , vol. 3, no. 3, **(2012)**, pp. 95-105.
[10] K. Dhanumjaya, M. Sudha, Dr. MN, G. Prasad and Dr. K. Padmaraju, "Cell Stability Analysis of Conventional 6T Dynamic 8T SRAM cell in 45nm Technology", International Journal of VLSI design & Communication Systems (VLSICS), vol. 3, no. 2, **(2012)**, pp. 41-51.
[11] K. S. Jeeva Bharrathi and M.Ravikumar, "Power Reduction using Single Ended 8T SRAM cell with NBTI Technique", International Journal of Advanced Research in Computer and Communication Engineering, vol. 4, **(2015)**, pp. 524-527.
[12] S. Birla, R. K.r Singh and M. Pattanaik, "Stability and Leakage Analysis of a Novel PP Based 9T SRAM Cell Using N Curve at Deep Submicron Technology for Multimedia Applications", Circuits and Systems, vol. 2, **(2011)**, pp. 274-280.
[13] N. Kr. Shukla, R.K.Singh and M. Pattanaik, "Design and Analysis of a Novel Low-Power SRAM Bit-Cell Structure at Deep-Sub-Micron CMOS Technology for Mobile Multimedia Applications", International Journal of Advanced Computer Science and Applications (IJACSA), vol. 2, no. 5, **(2011)**, pp. 43-49.
[14] S. K. S. Hamdioui, "Trends and Challenges of SRAM Reliability in the Nano-scale Era", IEEE International Conference on Design & Technology of Integrated Systems in Nanoscale Era, **(2010)**, pp. 1-6.
[15] R.K. Singh, M. Pattanaik and N. Kr. Shukla, "Characterization of a Novel Low-Power SRAM Bit-Cell Structure at Deep Sub-Micron CMOS Technology for Multimedia Applications", Circuits and Systems, vol. 3, **(2012)**, pp. 23-28.

