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An Optimize Approach to Design MUX Based Decoder Using Source Coupled Logic

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Abstract

In Combination logic there are some patterns which commonly occur and it is convenient to represent these in their own separate units often they are also available as separate integrated circuits. This research paper covers the two of these, the decoder and the multiplexer. In this work, designing of 2:1 MUX and MUX Based Decoder using SCL (Source Coupled Logic) is done. Power and value of current spike (Rail–to-Rail current) is found for the circuits. The Simulation is done using 180nm technology using TANNER (Version 9.2) tool.

Keywords: *MUX, MUX Based Decoder, SCL, SCL Inverter*

1. Introduction

The concept of digital data manipulation change the society in attractive way even all the electronic gadgets are in digital formats. Due to invention of various digital IC technologies we are in VLSI era. These digital technologies have their own advantages and disadvantages. Due to invention of Bipolar Junction Technology (BJT) the first IC had been implemented that is TTL (Transistor- Transistor Logic). TTL logic provides higher packing density but slow turn off process. A new technology had been developed called ECL (emitter coupled logic) which is fastest logic but provides higher power dissipation. But unfortunately, in VLSI era, BJT is defeated by MOS technology. MOS provides lower power dissipation and high packing density than BJT. But again CMOS beat the MOS technology as it provides excellent static characteristics like lowest static power dissipation and highest Noise margin. But the problem with the CMOS ICs is their dynamic power dissipation and digital switching noise. This problem is solved if we use differential amplifier. Because these amplifiers are not only less sensitive to noise but also enable us to bias amplifier and couple the amplifier stage together without the requirement for bypass and coupling capacitor. This born various technologies like SCL (source coupled logic), FSCL (folded Source Coupled Logic), MCML (MOS current Mode Logic). Static CMOS logic provides several advantages in designing digital circuit, that are low sensitivity to noise, good performance, low power consumption, *etc*. But it show some disadvantages while designing mixed mode ICs. In VLSI circuit, several logic gates switches simultaneously and resulting current causes switching noise. The mixed mode IC has both analog and digital circuit on single semiconductor die so this noise affect analog circuit through substrate coupling. This reduces speed and accuracy of mixed mode ICs. Various methods are used to reduce this noise in mixed mode ICs like separate analog and digital supply line, diffuse guard band, bonding pads *etc*.[1]-[4].Source coupled logic(SCL) was developed to reduce this digital switching noise and it is most successful methods among all the constant current source technique[5]-[10]. In

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1990 the first paper was published on SCL, in which two logic families Source Coupled Logic (SCL) and Folded Source Coupled Logic (FSCL) was introduced [11]. Synthesis of various combinational and sequential circuits using FSCL was done in 1992 [12]. In this paper, three techniques namely series-gated technique, multiplexer-minimization (MUX-MIN) and variable-entered mapping methods was given. In 2003, SCL gates both with and without an output buffer were designed and analysis of noise margin (NM) and delay of both the model had been done [13]. In 2008, SCL gate inverter had been designed and also describes layout effect on the SCL performance [14]. In 2011, MCML-FB (MOS current mode with feedback) was introduced. This logic is used for implementation of digital circuit at high frequencies [15]. The study of MCML-FB for the implementation of digital circuit for wireless communication system had been done [16]. Synthesis of D-LATCH using MCML was done. This is based on triple-tail concept [17]. Multiplexer using low- voltage MCML was implemented. This is also is based on triple-tail concept [18].

2. Decoder Circuit

A decoder circuit is a combinational circuit having n inputs and 2^n outputs. The 2×4 decoder circuit may be represented as two address lines A0 and A1 so that correspond four outputs, which will have the address 00, 01, 10 and 11. So these two bits correspond to address, so for example if A0 and A1 are both 0, this output is represented by 00 will be active if on the other hand we have A1 as 0 and A0 as 1, 01 will be active and so on. And of course there are many larger decoders for example, 3 bits coming in gives us 8 outputs which can be addressed so essentially it maps an address onto a range of outputs which are addressed and when we look at sequential logic, this is commonly used for example where the input bits maybe the bits representing the state or the output of the state register and then the output that is active corresponds to the specific state that is active at that time. Now this circuit can be implemented using discrete logic very simply.

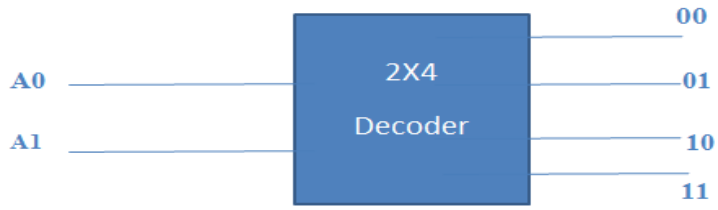

Figure 1. Block Diagram of 2×4 Decoder

So, we have 4-outputs and for each of those we have AND gate. So let our two address lines A1 and A0 which go down like this. So, if we want to represent this by 00, the two inputs must be inverted so that goes to that one and that goes to that one and this one we want to represent 01, in which case A1 is 0 and A0 is 1, in this case we want 10 so A1 will be connected to 1 and A0 to 0 and so on. If we want 3 bits coming in we will need 8 outputs so that is the decoder.

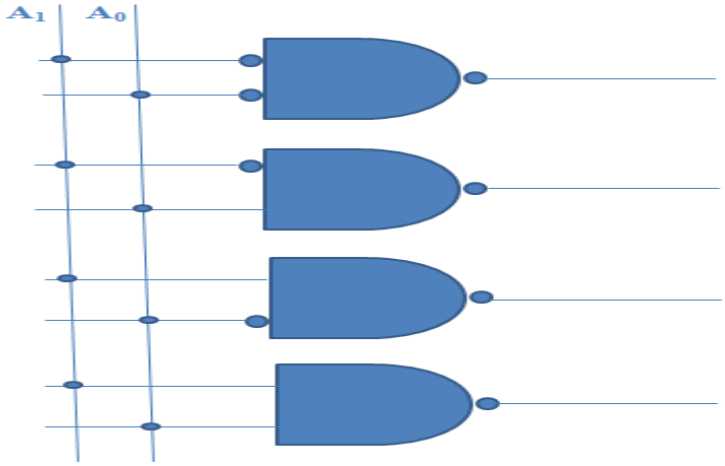

Figure 2. 2×4 Decoder with Logic Gates

3. Multiplexer Circuit

A multiplexer is a data selector combinational circuit. A 4 to 1 multiplexer *i.e*. 4 inputs and 1 output represented as a rectangle and since we have 4 inputs, we need two address lines S1 and S0 and we will have 4 inputs and one output and which input connects to the output depends on these address lines so if S1 and S0 are both 0 , 00 is connected to the output, and so on. And of course we can have 8 input and 1 output mux and so on. This is again a commonly used block and if we want to take an example we can use this to represent any combinational logic function that we want.

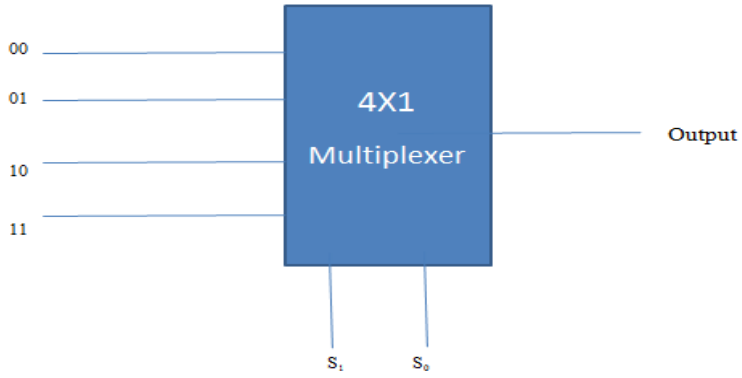

Figure 3. Block Diagram of 4×1 Multiplexer

Therefore MUX can be used to represent any truth Table that we want in one block unit and it is widely used when we have to construct complex logics. So, while designing this one can see these common patterns represented by the decoder or the MUX, then it will be much simpler if you can map then on the appropriate block unit, it greatly reduces the complexity of the circuit and when we look at the sequential logic it will often be the key as to use these units instead of more complicated individual gates.

4. Source Coupled Logic (SCL)

SCL is almost same as Emitter Coupled Logic (ECL) that is used with bipolar technology. SCL is a “Dual Rail Logic”. The SCL circuit consist NMOS differential pair biased with a constant current source Iss. The inverter circuit using SCL logic shown in Fig.4.Circuit have both input and its complement (Vi, Vi’) and output comes differential

form (Vo, Vo'). NMOS source coupled pair which operates in saturation or cut-off region. The biased constant current source Iss steered any one side of transistor while other is cut-off. This current converted into the differential output voltage by 2 PMOS transistor where these PMOS are working in linear region. If ΔV is the voltage drop across M3 (M4) transistor, differential output voltage become equal to 2 ΔV.

Logic function that implemented by SCL are placed between PMOS (active load) and biased current Iss. These logic functions are implemented using NMOS. Since it is dual-rail-logic, complicated to wire.

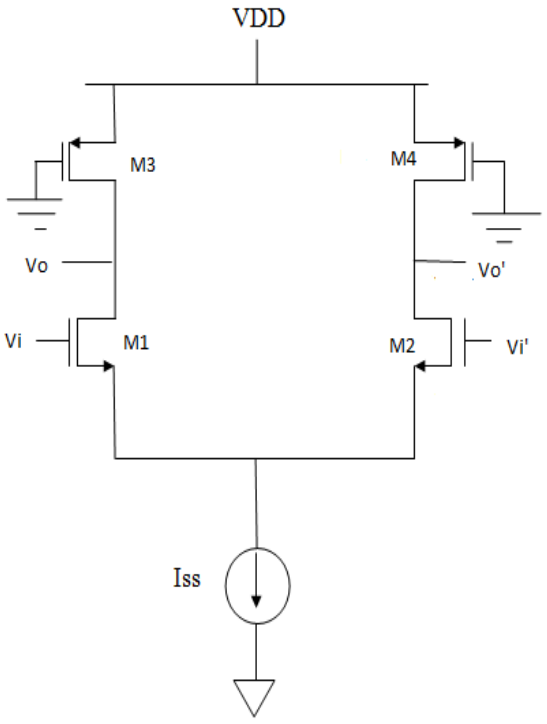

Figure 4. SCL INVERTER

5. Experimental Results and Proposed Methodology

5.1. Multiplexer-Minimization (MUX-MIN) Method

This is a technique, used to synthesize combinational SCL circuit. Using this method we always get a simplest circuit of a complex electrical system. In contrast, our main goal to apply this method in SCL gates to reduce the switching noise instead od number of branches and switching devices.

It's based on Shannon Expansion Theorem [19].In mux-min technique, NMOS differential pair act as 2×1 current-multiplexer.

So using this method an arbitrary n-variable function F (a, b, c,.....) can always realize where function F (a, b, c,.....) is 1st factorized w.r.t. 'a' then 'b' and so on as written in Equation(1)

$$F(a, b, c \ldots) = F(0, b, c, \ldots\ldots) a' + F(1,b,c,\ldots\ldots)a \quad (1)$$

Where F(0, b , c, ...) and F(1, b , c, ...) is evaluated w.r.t. a = 0 & a = 1.Now factorization w.r.t. b of the function is given by Equation (2) and Equation (3).

$$F(0, b, c \ldots) = F(0, 0, c \ldots) b' + F(0, 1, c \ldots) b \quad (2)$$

And

$$F(1, b, c \ldots) = F(1, 0, c \ldots)\, b' + F(1, 1, c \ldots)\, b \quad (3)$$

5.2. 2:1 MUX using SCL

Multiplexer is device that has several input and one output.2n input MUX has n select line and one output. A 2:1 MUX is implemented using SCL is shown in Fig.5. It consists 2 input and its complement (V2, V2', V1, V1') and one select line and its complement (So, So'). The circuit is implemented using MUX-MIN method. Depending upon the value of input and select line biased current Iss steered either side of transistor and Difference of Vo and Vo' gives the output of the MUX.

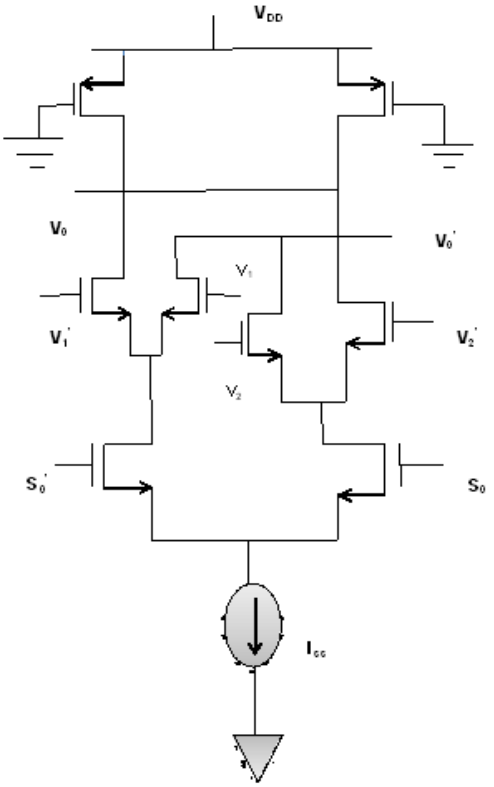

Figure 5. SCL 2:1 MUX

5.3. Mux Based Decoder Using Scl

The high speed analog-to-digital converters (ADCs) are generally based on a flash structure [20], [21]. It use {(2n)-1} comparators where n is the number of bits. The output of comparators are Thermometer code that is converted into binary code using Thermometer-to-binary decoder, which can be implemented by various of approaches, *e.g.*, a ROM, ones-counter [20], [22], or the multiplexer-based decoder found in [23-24]. In this paper we design a multiplexer-based Thermometer-to-binary decoder for N= 4bit because the use of a multiplexer-based decoder consume lesser power compared with other similar design.

The multiplexers used in this work are based on Source Coupled Logic (SCL), shown in Fig.6 selected.

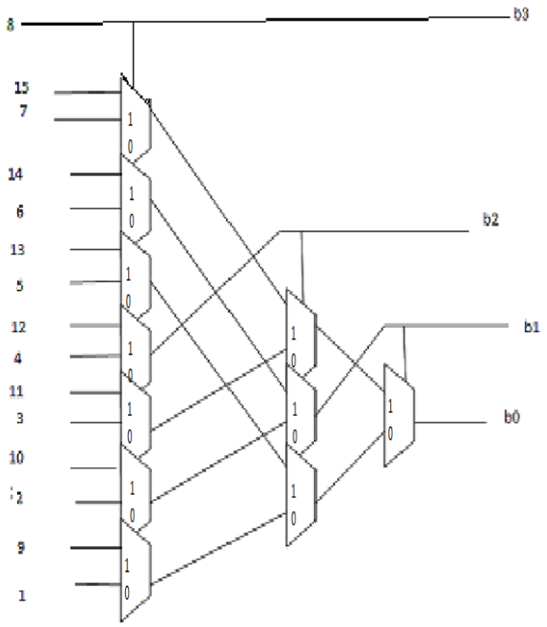

Figure 6. MUX Based Decoder

The circuit shown in Fig.5 and Fig.6 are simulated using TANNER (version 9.2) and 180nm technology to study the characteristics of MUX and MUX based Decoder. Parameters are provided through Table 1. As mention above, SCL was developed to reduce Digital switching noise for mixed mode ICs. SCL provides rail-to-rail current in the range of 5-10 µA. Thus noise generation has been reduced.

Table 1. Parameter for SCL Based Circuit

Property / Device	No. of transistor (NMOS\PMOS)	Average power	Average delay	Rail-to-Rail current
2:1 MUX	6\2	1.799999e-005 watts	0.21n	10µA
MUX based Decoder	66\22	3.240000e-012 watts	0.02n	10µA

6. Conclusion

In this paper report a decoder has designed with regular structure and short critical path. The logic family plays a vital role in the designing of any digital circuits. Because of low power requirement and better efficiency the SCL technology is used. The designing and analysis of 2:1 MUX and MUX Based Decoder has simulated using 0.18µm SCL technology. Various parameters like average power, average delay, maximum current spike and number of transistor has been calculated. The current through the circuit remains constant throughout the transition so more efficient technology.

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