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# Analysis of Fredkin Logic Circuit in Nanotechnology: An Efficient Approach

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***Abstract***

*In last few decades, typical lithography based VLSI technology used to improve higher scale integration, low switching speed and low powered computing of semiconductor constituents. However, this trend meets severe challenges of tunneling, short-channel effects and leakage current. Quantum-dot Cellular Automata (QCA) is one of the promising substitutions to traditional semiconductor-based technology which proposed a unique scheme of information transmutation as well as computation. QCA hold the assurance of rapid speeds, higher switching frequency, highly scalable feature and notably reduced sizes. In this paper, an efficient layout of fredkin gate is proposed based on QCA and CMOS technology which lessened total covered area, the number of cell and clock, latency time and number of coplanar wire crossing compared with the earlier design also the VHSIC Hardware Description Language (VHDL) of proposed fredkin gate is presented. For simulating and confirming the proposed circuit QCADesigner and Microwindlite, familiar verification and simulation tools has been occupied. The proposed design has a promising prospective in the organizing of nanoscale low power exhausting information processing system and can stimulate complex digital applications in QCA.*

***Keywords***: *Quantum Cellular Automata (QCA), Fredkin Gate, QCADesigner, MICROWIND, VHDL*

## 1. Introduction

Quantum dot cellular automata are efficient and emerging nanotechnology to replace Complementary metal oxide semiconductor (CMOS) technology and it depends on advanced physical phenomena as coulombic interactions and inventive approaches which completely depart from the regular CMOS-based model. QCA is envisaged as a rising nanotechnology for next generation ICs [1, 2] further it proposes a different technique of information and computation [3, 4]. In current age reversible circuit made an immense consideration in information processing. Energy loss is an essential speculation in establishing a digital system. In the early 1960s, R. Landauer manifested that high technology circuits and systems organized employing irreversible logic circuit results in energy dissipation due to information fall. Landauer's doctrine presents that the loss of one bit of information lost will dissipate $kTln2$ joules of energy, where $k$ is the Boltzmann's constant and T is operating temperature in Kelvin [5]. Next Bennett, in 1973 demonstrated that to elude $kTln2$ joules of energy dissipation in a circuit, it must be assembled from reversible circuits [6]. In reversible circuits information drop is not expedient so it is preferred to form combinational circuit. A number of QCA based circuits have been presented based on inverter, majority voter and QCA wires. Divers reversible circuits as well as combinational and sequential circuits have been suggested so far [7-17]. This paper, an efficient and potent design of fredkin gate is proposed that is

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more competent in terms of area, complexity and cell counts corresponding to the earlier layout [18].

## 2. QCA: Synopsis

A cell is the elementary component of QCA and consists of two electrons along four quantum dots that are arranged at the vertices of a square [19-21]. The electrons are impulse to the edge locations for coulombic repulsion [22]. QCA cell has two form of polarization [23, 24] P = -1 or binary 0 and P= +1 or binary 1 as shown in Figure 1. The equation for the cell polarization is defined as [8],

$$P=\frac{(\rho_1+\rho_3)-(\rho_2+\rho_4)}{(\rho_1+\rho_2+\rho_3+\rho_4)} \quad (1)$$

Where, the charge at dot *i* denoted by $\rho_i$

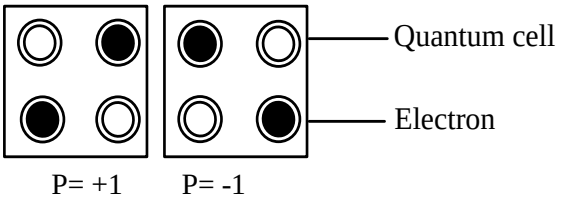


**Figure 1. Four Dotted QCA Cell with Binary Encoding**

The essential part of QCA based structure is QCA wire, majority voter and inverter. QCA wire is a collection of interconnected cells in which signal propagates from one place to another because of electrostatic interactions. QCA wires can be either formed up of $45^o$ cells or $90^o$ cells. In case of inverter, if two cells place at $45^o$ with respect to each other their interaction will be opposite and for that $45^o$ cells are mainly used for coplanar wire crossings. Figure 2 delineates the structure of two wire types.

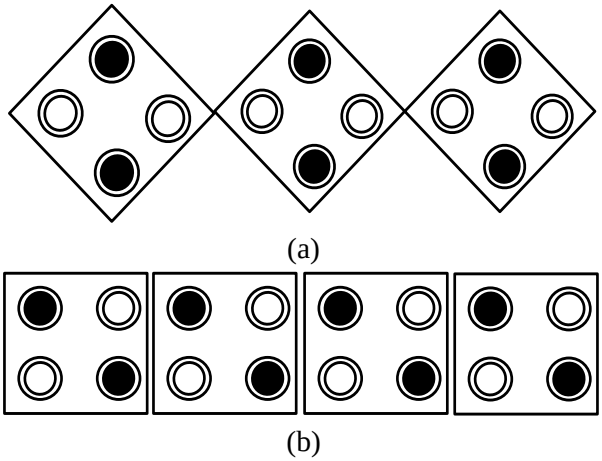


**Figure 2. QCA Wire (a) $45^o$ (b) $90^o$**

Three input majority voter ($Maj_3$) is the basic logic gate in QCA. $Maj_3$ can be composed offive cells; three inputs, one output and unique middle cell. The middle cell also recognized as device cell which switches to principal polarization [24] and resolves the firm output. $Maj_3$ can be performed as a 2-input AND or 2-input OR logic gate if the polarization of three input cells is fixed to p = -1 or p = +1, therefore, shown in Figure 3. The logical term of $Maj_3$ is as follows:

 

$$MV(A, B, C) = AB+BC+CA \quad (2)$$

To make "AND" and "OR" gate using majority gate set one of the MV input fixed to 0 or 1. Equation 3 and 4 shows the "AND" and "OR" gate operation when C=0 and C=1.

$$MV(A, B, 0) = AB+A.0+B.0 = AB \quad (3)$$
$$MV(A, B, 1) = AB+A.1+B.1 = A+B \quad (4)$$

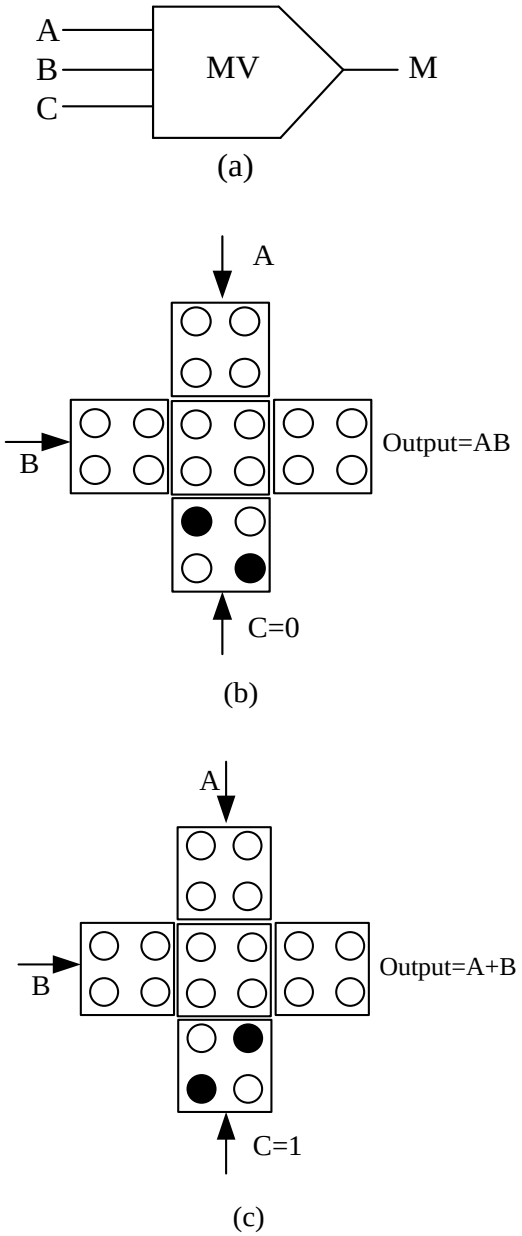


**Figure 3. Fundamental Form of 3-Input Majority Voter Gate (a), Function as 2-Input AND Gate (b) and 2-Input OR Gate (c)**

The QCA inverter essentially transmissions the cell polarization to the reverse polarization as shown in Figure 4. This inverter is made of seven cell or four QCA wires. The input polarization is divided into two polarizations and eventually, two wires unite and form the opposite polarization.

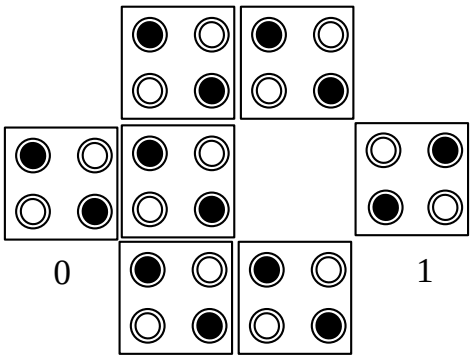


**Figure 4. Seven Cell QCA Inverter**

QCA timing is achieved by clocking in four specific and periodic states [25]. A QCA clock induces four stages in the tunneling barriers of the cells above it. In early level, the channel barriers begin to raise. The next level is attained when the channeling barriers are high enough to hinder electrons from channeling.

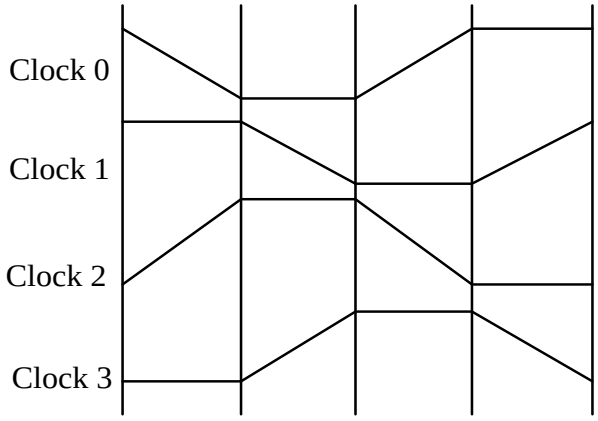


**Figure 5. QCA Signal for Clocking Zones**

The tertiary stage appears when the high barrier begins to lower. And in the last stage, the channeling barriers grant electrons to willingly tunnel again. So the four levels are Relax, Switch, Hold, and Release. A regular QCA architecture needs four clocks, each of which is periodically $90^{o}$ out of state along the prior clock. There is a latch between two clocking sections and clocking system arranges essential pipelining [26, 27] as well as grants multi-bit data transmission for QCA through signal latching.

## 3. Materials and Mechanisms

An analysis is completed to gain the needed tools and chosen to find out the proposed design. The design level is approved using different approximate simulators like the nonlinear approximation approaches and bistable simulation engine. But these approaches are iterative and do not form the certain measures. Eventually, the QCA Designer ver. 2.0.3 is chosen and this simulation engine is illustrated [28]. At the design, small block of QCA is formed and simulated for checking its accuracy. Then these small blocks of QCA are united together through QCA wire to attain the urged design.

Lastly, the integrity of the circuit is analyzed by the simulation engine of QCA Designer ver. 2.0.3 [29]. The simulation engines result the required waveform for the logical circuit. In the simulation, the software produced few criterion which involves default values like the size of cell, relaxation time, samples number, relative permittivity

 

*etc*. This paper, the simulated waveform of the proposed circuit perfectly fits the logical output and input.

The proposed circuit in CMOS is simulated and designed using MICROWIND [30] engine. This tool is ideal and convenient to design and achieve the covered surface of the various logic circuit.

## 4. Proposed Design and Presentation

A gate is called reversible if there is a one to one correspondence between its number of inputs and number of outputs assignments. Reversible circuit induces a specific set of output vector for each set of the input vector and it obtained extensive attention because their scope to abate the power dissipation. In this part, a decisive design formation of a reversible fredkin logic circuit is presented.

### 4.1. Fredkin Gate

Fredkin gate also recognized as CSWAP gate is a 3x3 gate with input vector $I_v(A, B, C)$ and output vector $O_v(X, Y, Z)$. The outputs are X=A, Y=A'B+AC, Z=AB+A'C. Figure 6 illustrates the block layout and QCA circuit representation of fredkin gate and Table 1 presents the logical Table of this circuit.

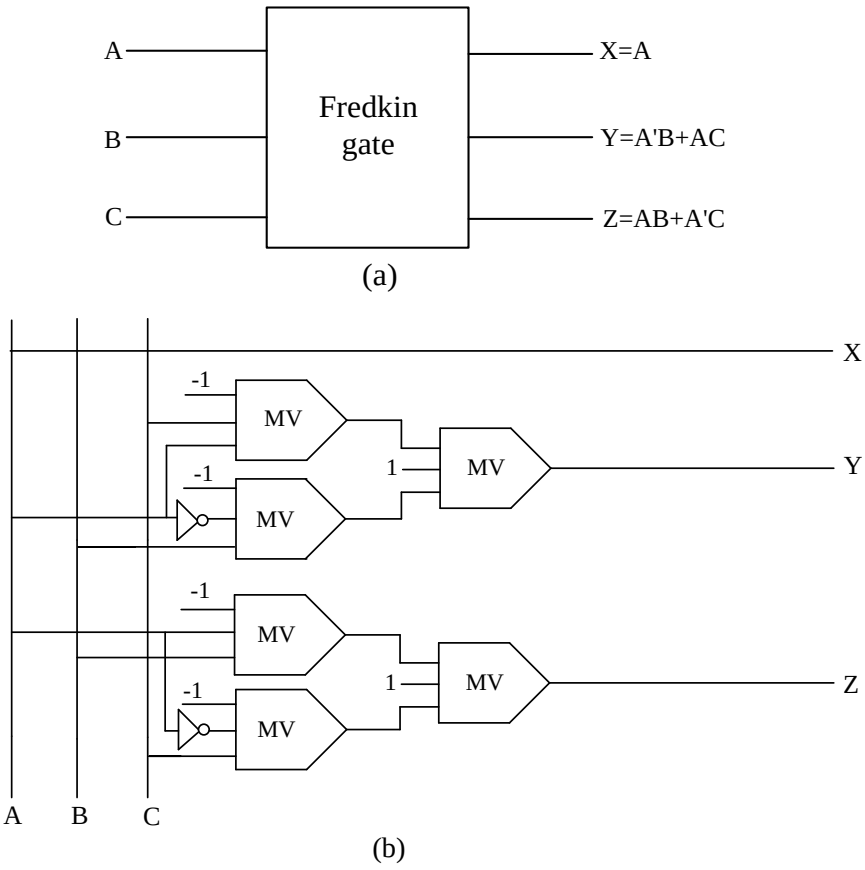


**Figure 6. Block Diagram of (a) Fredkin Gate (b) Proposed Layout of Fredkin Gate in QCA**

**Table 1. Truth Table of Fredkin Gate**

| Input | | | Output | | |
|---|---|---|---|---|---|
| A | B | C | X | Y | Z |
| 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 0 | 1 |
| 0 | 1 | 0 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 | 1 |
| 1 | 0 | 0 | 1 | 0 | 0 |
| 1 | 0 | 1 | 1 | 1 | 0 |
| 1 | 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 | 1 |

### 4.2. VHDL Implementation of Fredkin Gate

```
Library ieee;
Use ieee std_logic.1164..all;
Entity fredking is
Port (A, B, C : in std_logic;
X, Y, Z : out std_logic);
end fredking;
architecture ckt of fredking is
signal Abar, S1, S2, S3, S4 : std_logic;
begin
X<= A;
Abar<= not A;
S1<=Abar and B;
S2<= A and C;
Y<= S1 or S2;
S3<= Abar and C;
S4<= A and B;
Z<= S3 or S4;
End ckt;
```

## 5. Simulation and Result Analysis

The urged model has been functionally designed and simulated using the QCADesigner 2.0.3. Consecutive parameters in the bistable approximation are employed which are the default figures in QCADesigner. These parameters are shown in Table 2.

**Table 2. Parameters of Bistable Approximation**

| Criterion | Value |
|---|---|
| size of cell | 18nm |
| dot diameter | 5.000 |
| number of samples | 12800 |
| convergence tolerance | 0.001000 |
| radius of effect | 65.000000nm |
| relative permittivity | 12.900000 |
| layer separation | 11.500000 |
| clock amplitude factor | 2.000000 |
| clock high | 9.800000e–022 |
| clock low | 3.800000e–023 |
| upper threshold [1] | 0.500 |

 

| | |
|---|---|
| lower threshold [0] | -0.500 |
| maximum iterations per sample | 100 |

In circuit design, two fixed polarization P=-1 and P=+1 is used which are employed to switch the logic condition. The layout of proposed circuit is shown in Figure 7 and the simulated outcome is specify in Figure 8.

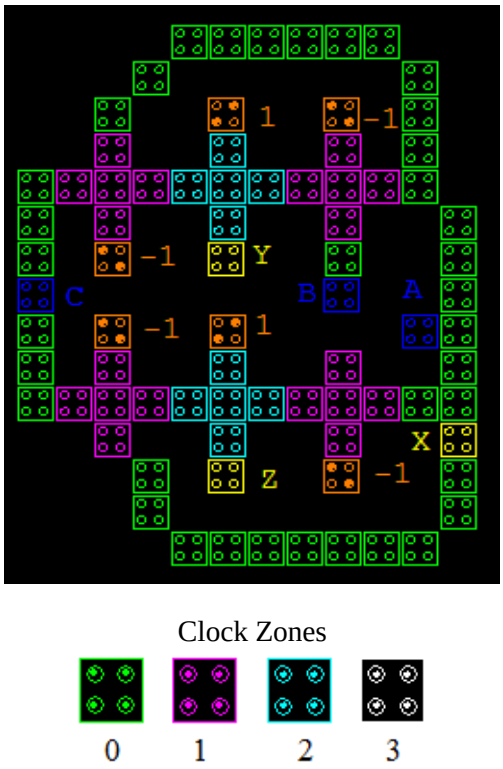


**Figure 7. QCA Simulated Circuit Design of Proposed Fredkin Gate**

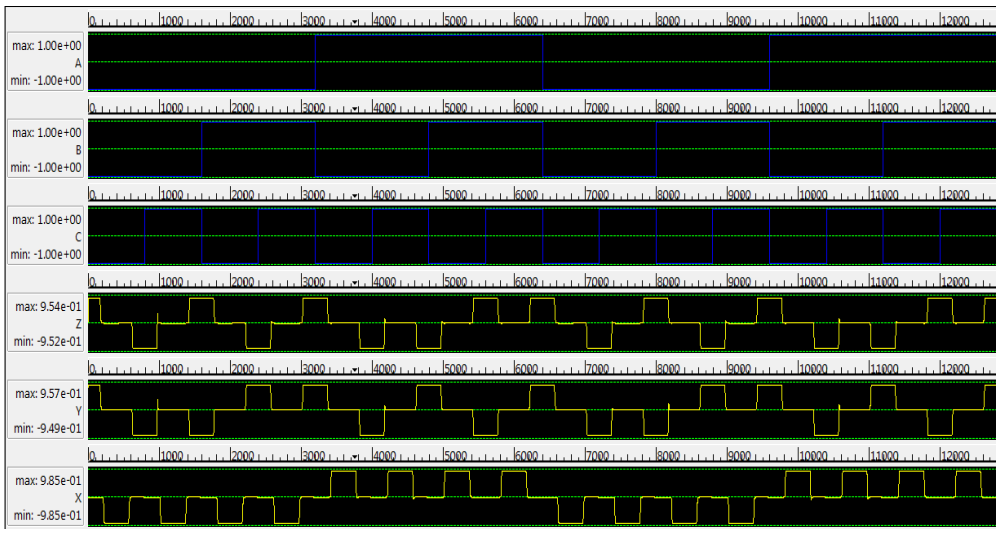


**Figure 8. Simulated Waveform for Fredkin Gate**

The layout of proposed circuit in CMOS is prescribed in Figure 9 which is designed using Microwindlite tool, a rapid organized EDA tool for back end and front end chip design into an integrated flow.

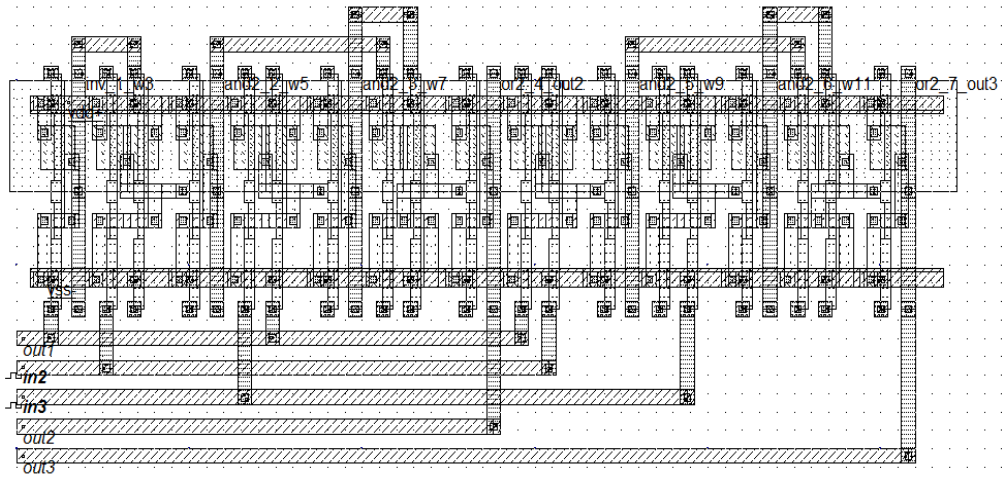


**Figure 9. Simulated Circuit Design of Fredkin Gate**

**Table 3. Performance Criterions of Proposed Design**

| Parameter | Proposed fredkin gate | fredkin gate [18] |
|---|---|---|
| Number of cells | 79 | 246 |
| Clock used | 3 | 4 |
| Time delay (clock cycle) | 0.75 | 1 |
| Number of wire crossings | 0 | 5 |
| Area in QCA ($\mu m^2$) | 0.07 | 0.375 |
| Area in CMOS ($\mu m^2$) | 122.3 | |

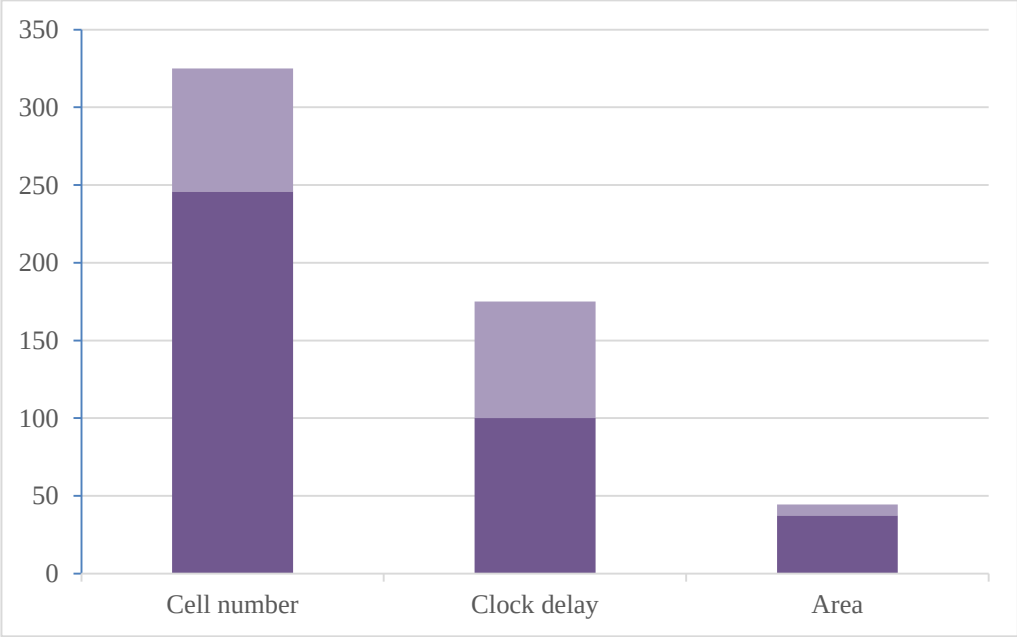


**Figure 10. Comparative Figures for Cell, Time Delay and Area of Proposed Fredkin Circuit**

## 6. Conclusion

This paper analyzes an adept approach of fredkin gate based on QCA and CMOS technology. Functional operation of fredkin gate in the enhancement of combinational circuits would be productive in respect of power redeeming and delay. During the design, a concentration is made to dwindle the number of cells as well as the area. The proposed design in QCA is 1747 times smaller in size than CMOS technology and ignore multi-layer wire crossing that would be very significant for designing compact and fault tolerant low power consuming nanomaterial. The simulation effect endorsed that the proposed design executes well. Therefore, it concludes that the urged layout should be promising pace towards the intention of quantum computers as well as low power design in nanotechnology.

The forthcoming work can be extended as to design systems to handle large-scale circuits along the inevitable objective of synthesizing quantum circuits.

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