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Parameter Analysis of different SRAM Cell Topologies and Design of 10T SRAM Cell at 45nm Technology with Improved Read Speed

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Abstract

Read stability and write ability, or SNM (static noise margin) in total, of a SRAM cell is the effective tool to determine the practicability of the cell. Leakage current, read speed and read stability are few of the constrained parameters desired for any practical SRAM cell. The aim of this paper is to analyze the read behaviour of the multiple SRAM cell structures using cadence tool at 45nm technology and to compare the cells for read operation while keeping the read and write access time and the supply voltage as low as possible. In particular, the leakage currents, leakage power and read behaviour of each SRAM cells are examined . A 10T SRAM cell implementation is proposed here that results in reduced leakage power and leakage current, at the same time with increased read stability in comparision with the conventional 6T SRAM cell as well as 7T, 8T and 9T SRAM cells. As a result, the 10T SRAM always consumes lowest leakage power and leakage current; improve read stability as compared to the 6T, 7T, 8T and 9T SRAM cells. This paper is aimed to reduce the leakage power, leakage current and improve the read behaviour of the different SRAM cell structures using cadence tool at 45nm technology while keeping the read and write access time and the power as low as possible.

Keywords*: SRAM Cell, Leakage Current, Leakage Power, Read Stability, Low Power*

1. Introduction

The proposed SRAM topology in this paper uses a multiple 10T structure that is aimed to produce faster read operation without disturbing the basic cell [1]. In case of conventional 6T SRAM, the read operation is performed by asserting the word line high and accessing the latch by access transistors. Due to static noise the read operation may lead to disturbance and corruption of the data stored in the cell,

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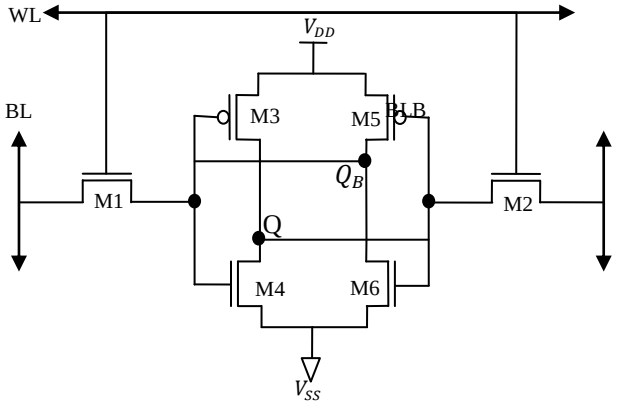

Figure 1. The Schematic of Conventional 6T SRAM Cell

In conventional 6T cell, the read operation is quite a slow process, due to undesirable time the access transistors takes for activation to access the latch. Delayed read operation in SRAM does mean time required to respond to a particular operation (read or write) would be quite large resulting in increased leakage power over this long period of time in the idle circuit. This reduction in the performance makes the cell objectionable for use in the practical applications [2].

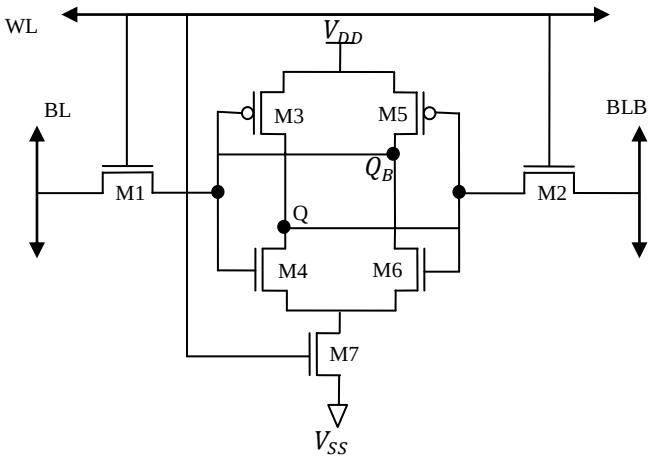

Figure 2. The Schematic of 7T SRAM Cell

Also, the static noise margin (SNM) [3, 4] dramatically declines as the supply voltage is reduced. Reduced supply voltages may lead to data corruption and invalid data sensing from the cell, which would be an undesirable situation for practical designs. Another disadvantage of supply voltage reduction is delay in read operation which reduces the speed performance of the cell. On the other hand higher supply voltage leads to larger leakage power making the cell again inefficient. In the basic memory element i.e. cross-coupled inverters, the two nMOS transistors (NM4, NM6) are expected to have more strength as compared to the access transistors for proper read operation.

In 7T SRAM cell structure an additional transistor placed in the ground path of a 6T SRAM cell to reduce leakage while the cell is in standby mode. In the standby mode, the bottom transistor is intended to cut-off the ground path and to eliminate the leakage paths through the inverter transistor sources but this cell cannot increase the read speed [5].

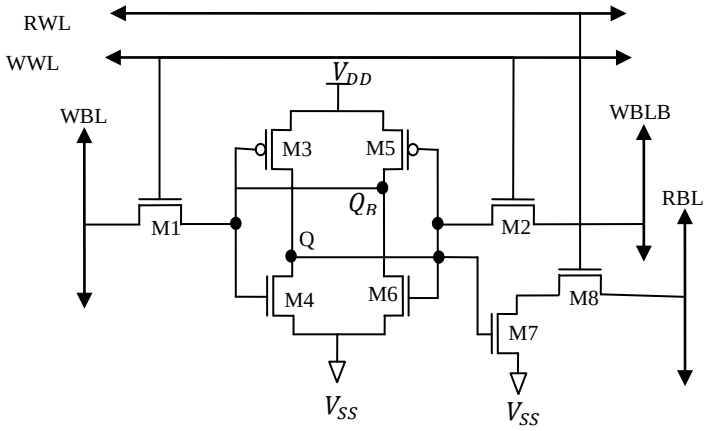

Figure 3. The Schematic of 8T SRAM Cell

The data stability and functionality of a 6T and 7T SRAM cells mostly depends on the sizing of transistors. The stability of a 6T and 7T SRAM cells are characterized by the ratio (β) of the size of the pull-down transistors to the access transistors. Higher β leads to enhanced data stability at the expense of increased leakage power and larger cell area. To overcome the problem of data storage destruction during the read operation, an 8T cell implementation was used, for which separate write/read bit and word signal lines are used to separate the data retention element and the data output element. Such a cell implementation provides a read-disturb-free operation [6].

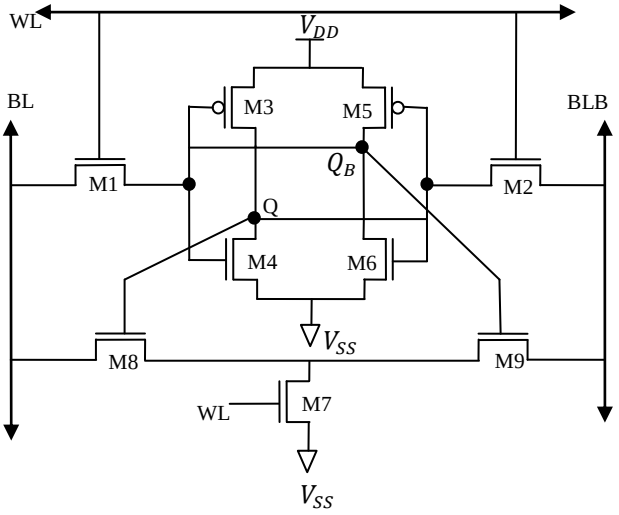

Figure 4. The Schematic of 9T SRAM Cell

For simultaneously reducing leakage power and enhancing data stability a 9T SRAM cell is used. In a 9T SRAM cell the data is completely isolated from the bit lines during a read operation. The read SNM of such circuit is thereby enhanced as compared to a conventional 6T SRAM cell. In an idle 9T SRAM cell, the cells are placed into a super cut-off sleep mode, thereby reducing the leakage power consumption [7].

However in case of SRAM, switching OFF the circuit does mean losing the data, and unfortunately it is a compulsion to keep the cell ON even in the idle state. This situation is a major challenge in reducing the leakage current as we have no option but to keep the circuit ON. To overcome the limitations mentioned above, the proposed SRAM cell has been designed with a different read process which reduces the time required to read the cell

and also reduces the chance of data corruption of cell by isolating it from the external read circuitry [8]. The efficiency of the cell is enhanced by designing it to work with lower supply voltages, which helps in further reduction of the leakage power.

2. Proposed 10T SRAM Cell

The SRAM structures have been designed to limit the noise in read operation by adding a different circuit for read operation which isolates the basic memory element from the external noise keeping the access transistors disabled while reading the cell. This addresses the drawback of the 6T cell read operation as discussed earlier. The 10T structure, shown in Figure 5, employs an inverter as read buffer [9] connected to the Qb (Q Bar) of the cell. As noted from the schematic that read buffer has been connected before the access transistors to access the memory element without having the requirement of switching them on. This reduces the time of reading by eliminating the switching time of access transistors as they are out of action during the read operation. However the write speed of the cell would still be slow which leads to degradation of write speed performance of the cell. The write waveform of the 10T structure is shown in Figure 7 and read waveform in Figure 8.

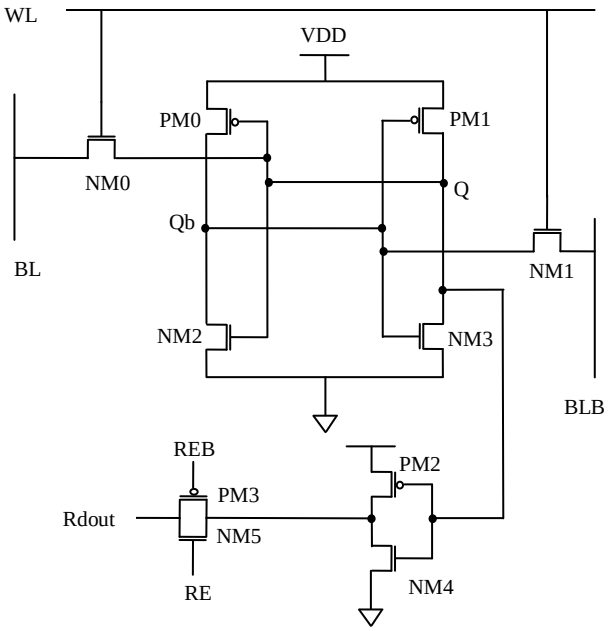

Figure 5. The Schematic of 10T SRAM Cell

In this design, a transmission gate is used for Read purpose. The additional signal REB is an inversion signal of read word line (WL). It controls the additional transistor PM3 of the transmission gate [10]. While the WL and REB are asserted and once the transmission gate is ON, a stored node is connected to Q. Thus a stored value at Q is being transferred to or read through inverter.

One of the major advantages of this design is that it is not necessary to prepare a precharge circuit as sense amplifier as required in 6T SRAM cell because the stored value is directly passed through transmission gate. A charge/discharge power on the Rdout is consumed only when the Rdout is changed [11]. Consequently, no power is dissipated on the Rdout if an upcoming data is the same as the previous state. The design reduces a bitline power in both cases that the consecutive “0”s and consecutive “1”s are read out [12].

The layout of the new 10T SRAM structure has been designed using Cadence Virtuoso tool with the aim of minimum area requirement. This makes the cell more efficient in terms of area as well as power. Figure 6 shows the layout of 10T SRAM cell.

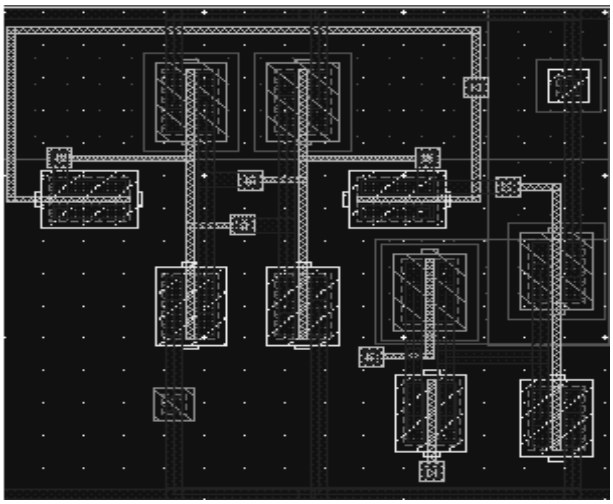

Figure 6. Layout of 10T SRAM Cell

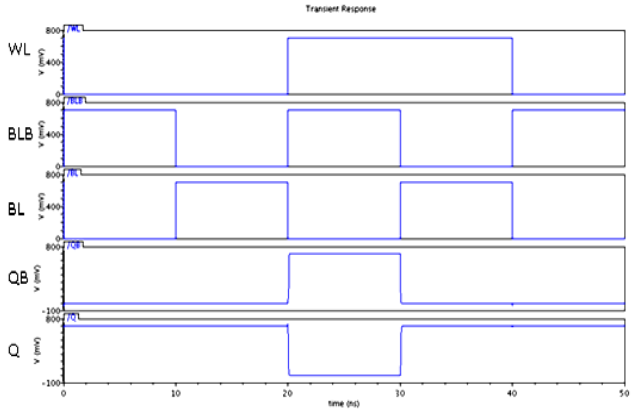

Figure 7. Waveform for Write Operation of 10T SRAM Cell

According to the write waveform, Q and QBar (QB) depend on Bit Line (BL) and Bit Libe Bar (BLB) respectively. When write line (WL) is at high voltage (say, 1 V) then output Q depends on BL and QB depends upon BLB. The write 1 delay, 120 ps, is less than the write 0 delay 110 ps in revealed waveforms.

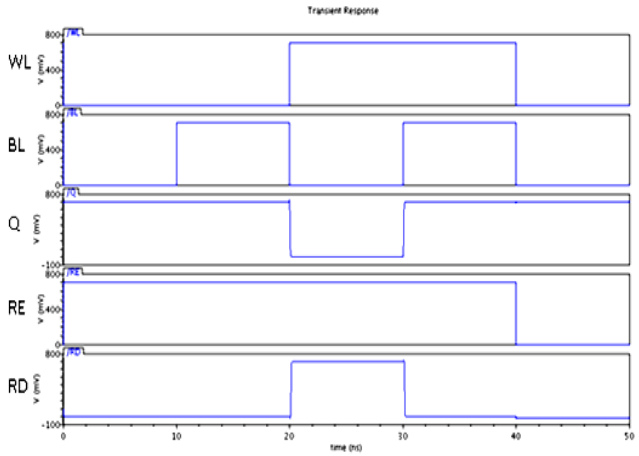

Figure 8. Waveform of Read Operation of 10T SRAM Cell

According to read waveform, as the inverter is connected directly with memory element before the access transistor to make the read operation independent on access transistors and buffer is connected to inverter output consequently the read buffer is connected to circuit for robust and fast read operation at low voltage. The read output depends on read enable (RE) and read enable bar (REB) which are kept at opposite voltages. The interval at which both WL and RE are high, the read will occur. Hence the circuit becomes independent of bit lines and gives disturb free read operation. The read delay in the circuit is 50 ps.

3. Power Consumption

Power consumed in any circuit can be due to a number of parameters like sub-threshold leakage, temperature and also at larger supply voltage (Vdd) [13, 14]. The 6T SRAM Cell has more sub-threshold leakage as compared to 10T SRAM Cell due to read-disturb free circuit. The disturb-free read circuit, connected to output node Q before access transistor, reduces the delay and leakage throughout the read cycle since the circuit becomes independent of access transistors and hence does not depend on bit lines.

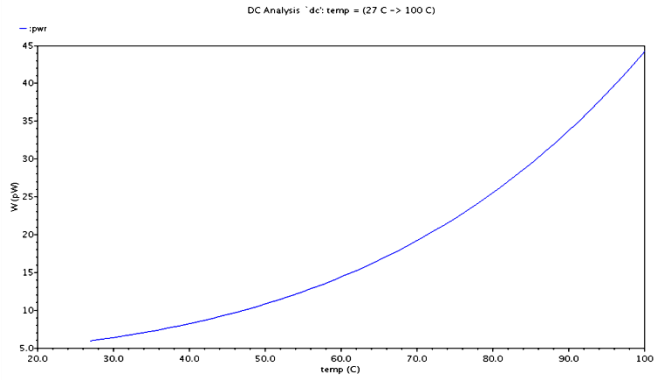

Figure 9. Power Versus Temperature Curve of 10T Cell

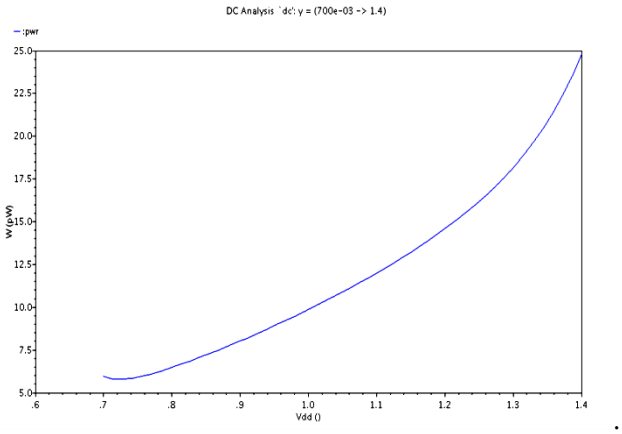

Figure 10. Power Versus Vdd Curve of 10T Cell

During the read cycle high voltage is stored at node Q, the transistor NM4 shows the leakage since it becomes off. Variation of power consumption with respect to supply voltage is plotted in Figure 17. The overall circuit leakage power is reduced to 19.09 nW. The leakage power waveform is shown in Figure 11.

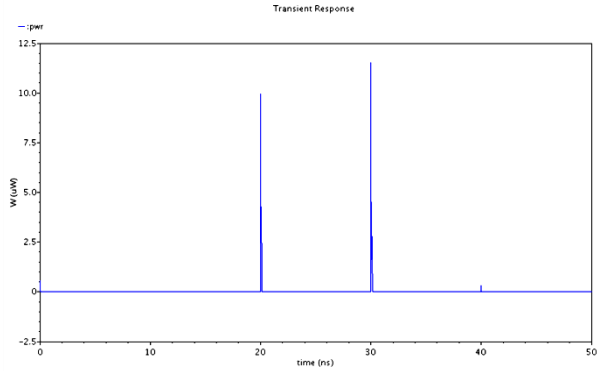

Figure 11. Leakage Power Waveform of 10T SRAM Cell

4. Simulation Results

The sim ulation of the 10T SRAM cell is performed with Cadence virtuoso tool at 45 nm technology. Calculation of different parameters is summarized in table 1. Results show that delay is improved to 13% and power has been reduced up to 36% with disturb-free read operation. The most important observation of this cell is that the read delay operation has been reduced up to 54% which can be clearly observed from table I, thus making the read operation very fast.

Table 1. Simulation Results for Different SRAM Cells

Sr. No.	Parameter	6T Cell	7T Cell	8T Cell	9T Cell	10T Cell
1	Technology	45nm	45nm	45nm	45nm	45nm
2	Supply Voltage	700 mv	700 mv	700 mv	700 mv	700 mv
3	Power	19.1 nw	16.8 nw	24.4nw	18.1nw	12.1 nw
4	Read Delay	110 ps	92.8 ps	81.7 ps	84.4 ps	50 ps

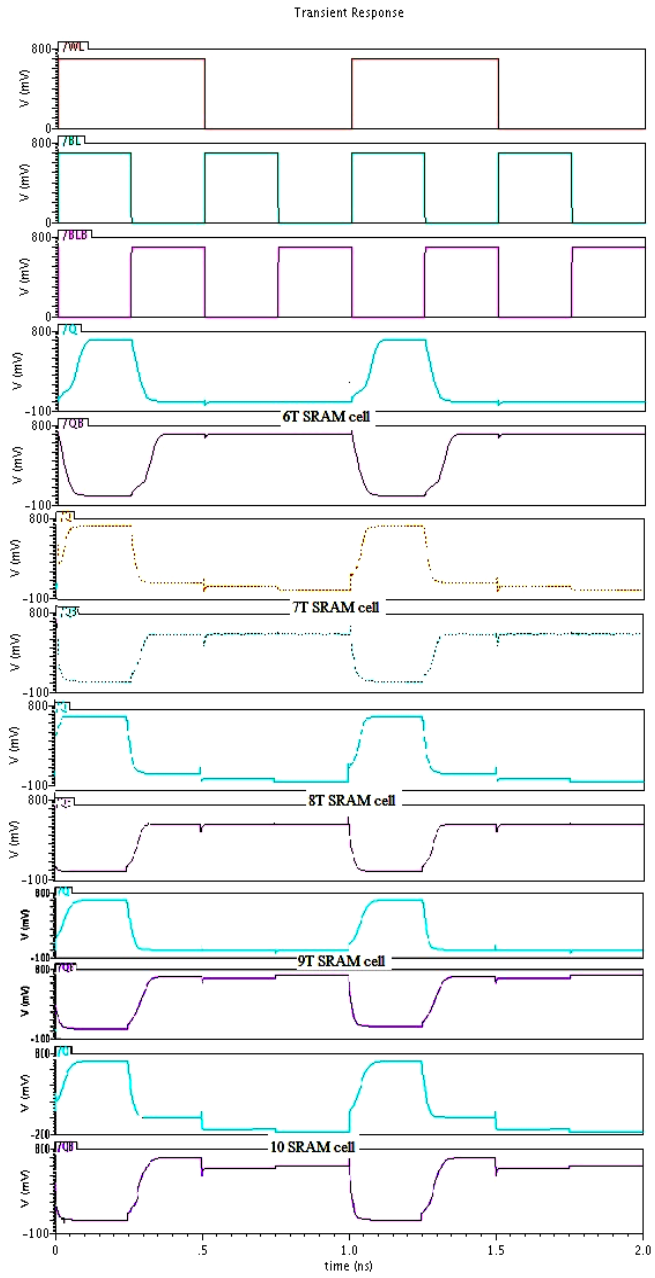

Figure 12. Waveform for Write Operation of 6T, 7T, 8T, 9T and 10T SRAM Cells

The SRAM cell here has been simulated using Cadence Virtuoso tool at 45nm technology. These results are compared with the performance results of the conventional 6T SRAM cell. With the accomplishment of the objectives of the research work, the results reveal that 10T SRAM cell consisting a read disturb free circuit improves the read delay and increases the SNM of the cell hence provides better performance and high speed. The power consumption of 10T structure has also been analyzed by varying the temperature and supply voltage of the cell which shows stable and desired level of power consumption.

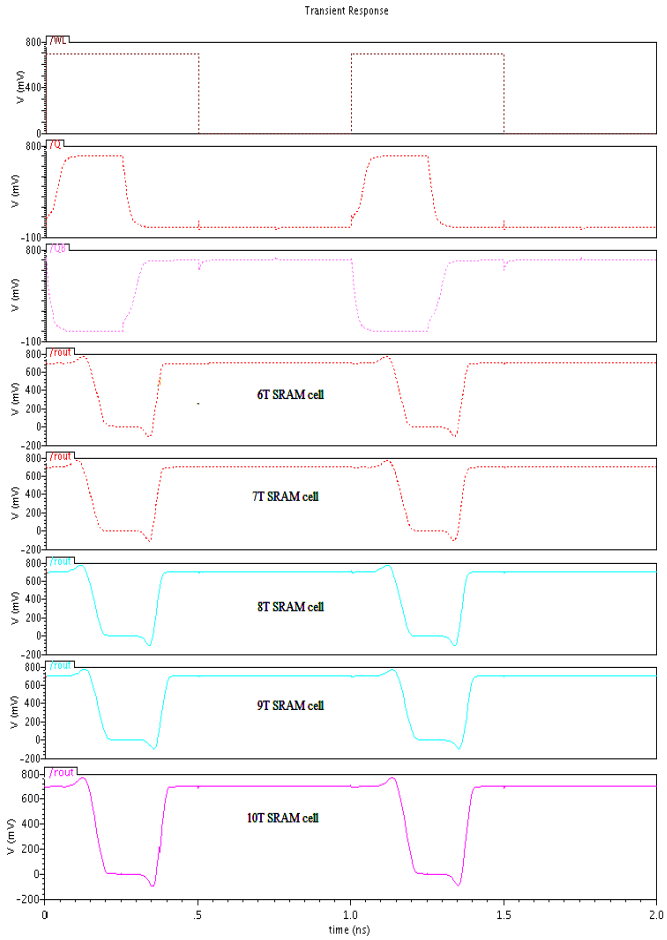

Figure 13. Waveform of Read Operation of 6T, 7T, 8T, 9T and 10T SRAM Cells

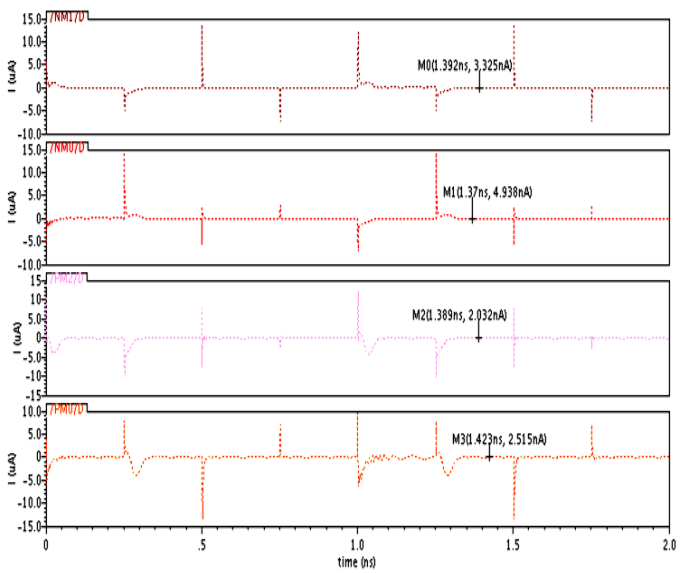

Figure 14. Waveform of Read Operation of 6T, 7T, 8T, 9T and 10T SRAM Cells

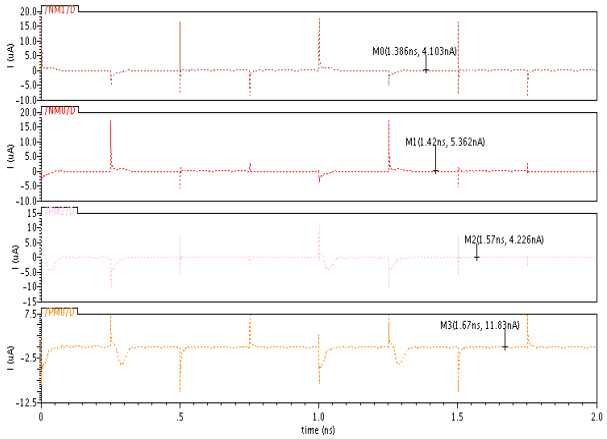

Figure 15. Leakage Current Waveform of 6T SRAM Cell

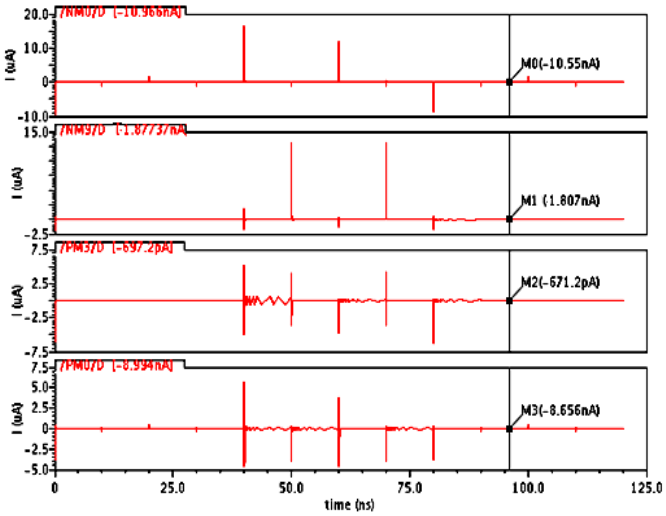

Figure 16. Leakage Current Waveform of 10T SRAM Cell

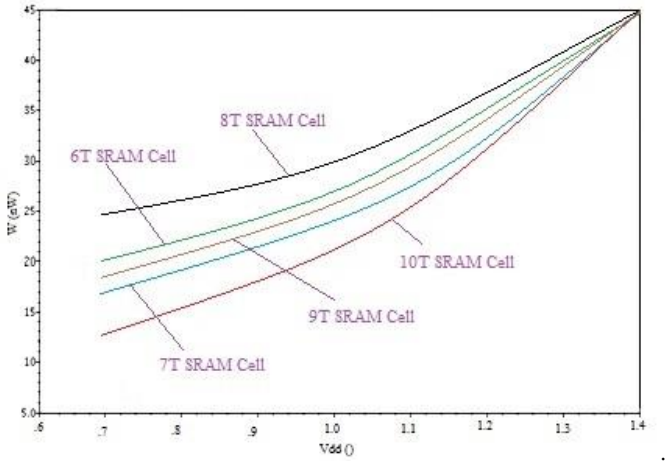

Figure 17. Power Versus Vdd Curves of 6T, 7T, 8T, 9T and 10T SRAM Cell

5. Conclusion

This paper compared the performance parameters of five SRAM cell topologies, which include the conventional 6T, 7T, 8T, 9T and the proposed 10T SRAM cell implementations. In particular, the leakage currents, leakage power and read behaviour of each SRAM cells are being analyzed. The conventional 6T, 7T and 8T SRAM cells are the most area efficient have least transistor count. However, the leakage power becomes large and the read stability decreases due to undesirable time the basic latch consumes to read the cell during read operation, moreover the cell data is prone to corruption due to external noise. Even though 9T SRAM cell would simultaneously reduce leakage power and enhance data stability but it shows no much improvement of leakage in comparision to 8T SRAM cell. To circumvent this problem the 10T SRAM cell design has been proposed in this research work, in which a dedicated inverter and transmission gate are appended as a single-end read port. The results show that the 10T SRAM always consumes lowest leakage power and leakage current; improve read stability as compared to the 6T, 7T, 8T and 9T SRAM cells.

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