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Implementation of Low Power Test Pattern Generator for Digital Integrated Circuits

Vardhana M[1*] and Niju Rajan[2]

[1] *I M.Tech. VLSI Design and Embedded Systems*
NMAM Institute of Technology, Nitte, India
[2] *Assistant Professor, Department of Electronics and Communication Engineering*
NMAM Institute of Technology, Nitte
[1] *vardhana619@gmail.com*
[2] *nijurajan@nitte.edu.in*

Abstract

Low power consumption is gaining more significance for design of digital system design. The system has to be operated efficiently by consuming low power, which greatly increases the life of the battery. Every system has to be tested for its performance, before it is released into the market, hence testing is one of the major area of research. Testing of digital system is one of the main and important part in the design and implementation of digital integrated circuits. To ensure that the designed system responds properly, according to the system specification, testing is carried out. The quality of the chip produced will depend upon, how best the testing strategies, or the test vectors are chosen for testing the integrated circuit. The test patterns are generated with the help of automatic test pattern generators. Thus the performance of test pattern generator is very important. In this paper, a low power architecture for generating the test patterns, for testing digital integrated circuits is implemented. Verilog coding is done and is simulated using CADENCE simvision, and the RTL schematic is extracted. The gate level optimization is carried. The power consumed before optimization was found to be 166.79 mw, and the power consumed after optimization was found to be 65.88 mw. This paper presents the VLSI implementation low power test pattern generator. The performance parameters such as area, power and timing are also derived after the analysis.

Keywords*: LFSR, Low power test pattern generator, DFT, BIST*

1. Introduction

With the increasing trends in VLSI technology, it is possible to incorporate more and more number of transistor on a single chip. Also, the frequency of operation is increasing day by day. It becomes complex, to test the reliability and functionality of the manufactured circuit, as the number of transistor on a given area is rapidly increasing. Thus the automated test pattern generators, are used to generate the necessary vectors to test the functionality of the developed chip. As the number of inputs in a given system increases, the size of the, input vector also increases. In order to minimize the complexity of testing, it is enough to test the circuit for the given set of input combination. Such a type of input vectors, which produces a different output in a faulty circuit, as with the fault free circuit is called as test vectors. The automatic test equipment is used to test the digital integrated circuits. These involve test pattern generators, which generates the necessary test vectors. Thus it is necessary that, the test pattern generators, doesn't consume more power. The designed test pattern generator has to produce the test vectors at the same speed as that of the operating frequency of the chip which is being tested. The speed of operation is directly proportional to the power consumption. Hence increase in

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speed increases the power dissipation. Hence it is very necessary to develop a pattern generator, which operates at the same speed as that of the circuit being tested, and also less power. In this paper, a low power architecture of test pattern generator is implemented using CADENCE. Optimization is carried out to reduce delay, power and also area. It is observed that there was significant improvement with respect to performance parameters, after optimization.

2. Literature Review

In modern system-on-chip design, power dissipation is one of the major challenging factor. Hence ones interest is to develop a low power system, in order to increase the system efficiency. Major works are carried out in the field of development of low power test pattern generator, which consumes less power and doesn't affect the fault coverage. The design of low power test pattern generator for built in self-test (BIST) circuit is described in [1]. It describes the general architecture for BIST, and also the various test pattern generation approaches. An architecture of linear feedback shift register (LFSR) has been implemented by two modules. It is observed that, the conventional LFSR consumed 22mW of power whereas, the modified LFSR consumed 17mW of power. A logic BIST using linear feedback shift register, has been described in [2]. The designed architecture is programmed using Verilog HDL and simulated using CADENCE EDA tool of 180 nm technology library. It claims that the design gives better performance in term of power dissipation as compared with the conventional LFSR. Low power structure for 2D LFSR has been discussed in [3]. It describes the different architecture and implements the low power architecture for BIST using 2D LFSR. Today's system on chip design and test face several problems, especially in terms of power. Generally, the power dissipation is more in test mode rather than normal mode of operation. Hence low power test application has become one of the major area of research and development. Built in self-test has emerged as a solution to this problem. BIST is a design for testability, which is used to test the chip by incorporating test logic. Test vectors, which are applied to a circuit, will consume more power than the normal mode, because of the reason that the random nature of patterns generated by LFSR. This result in more switching in test mode which in turn increases the power dissipation. Several techniques have been proposed to address the problem of power dissipation. A strategy called as dual-speed LFSR [4] is proposed to reduce the overall switching. LFSR is one of the main component of the test pattern generator, which is used to generate random sequences. The low power test pattern generator, presented in [5] is based on circular automata. Another low power test pattern generator is proposed in [6], which reduces the power in circuit under test. The test generation technique, used in the BIST [7] include pseudo exhaustive testing, weighted random testing using LFSRs and reseeding the LFSRs [8]. The main disadvantage of these technique, is that they do not provide high fault coverage. In this paper low power architecture [9] for test pattern generator is been presented. The architecture consumes less power, and can be effectively used for the testing [10] of digital integrated chips.

3. Methodology

In this paper, low power architecture for test pattern generator is presented using an LFSR. The system produces test patterns whose width is of 4 bit. It uses a linear feedback shift register, whose architecture is shown in the Figure 1. A simple LFSR consists of a D flip flop, with a feedback given via an EX-OR gate. The circuit produces random sequences at every rising edge of clock.

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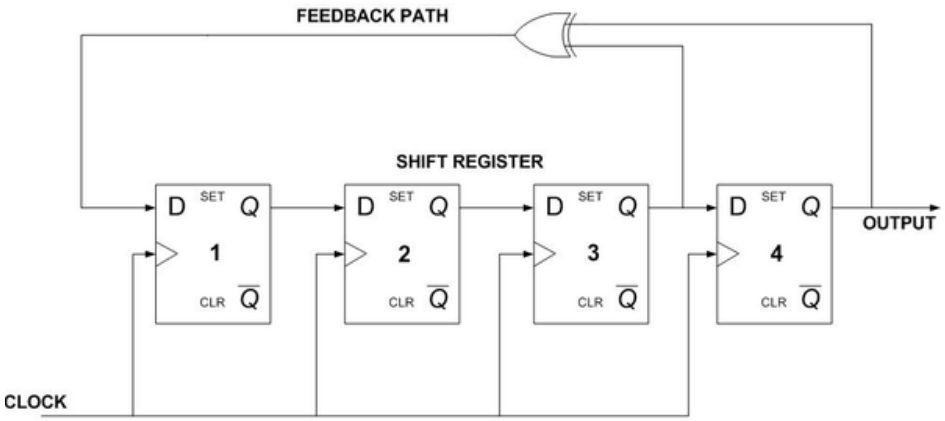

Figure 1. Linear Feedback Shift Register

The general block diagram for an m bit test pattern generator is shown in Figure 2. It consists of an LFSR, a counter, grey code converter and primitive gates.

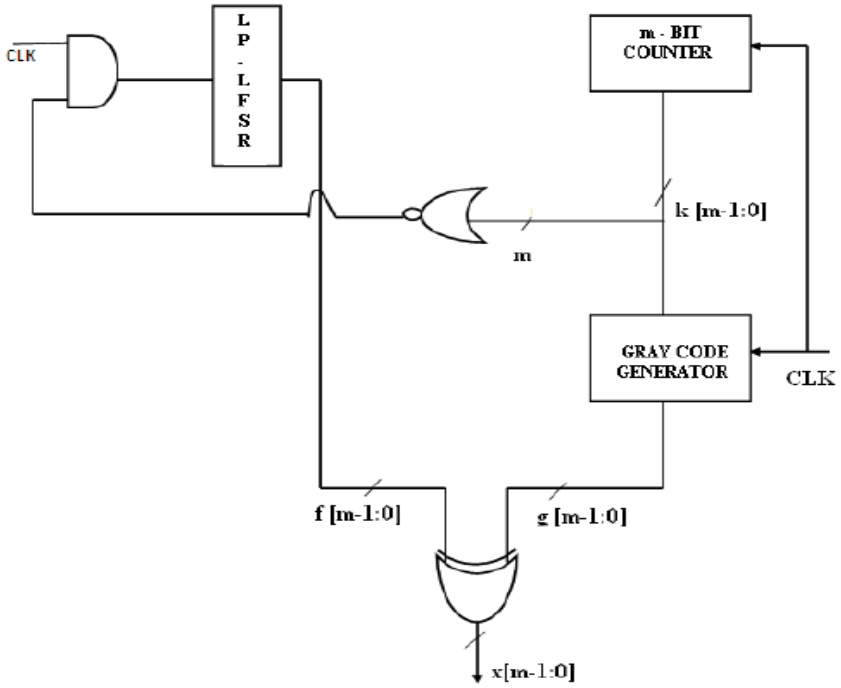

Figure 2. Low Power Test Pattern Generator

4. Results and Discussions

The low power architecture for test pattern generator shown in Figure 2 is implemented using CADENCE EDA tool at 180nm technology. Verilog coding is done for the architecture and simulated using CADENCE Simvision. Timing constraints are exercised and timing analysis for the same is done. The Script file is executed and the RTL schematic is obtained. The optimization of the design is carried out and the Register Transfer Logic is obtained before and after the optimization.

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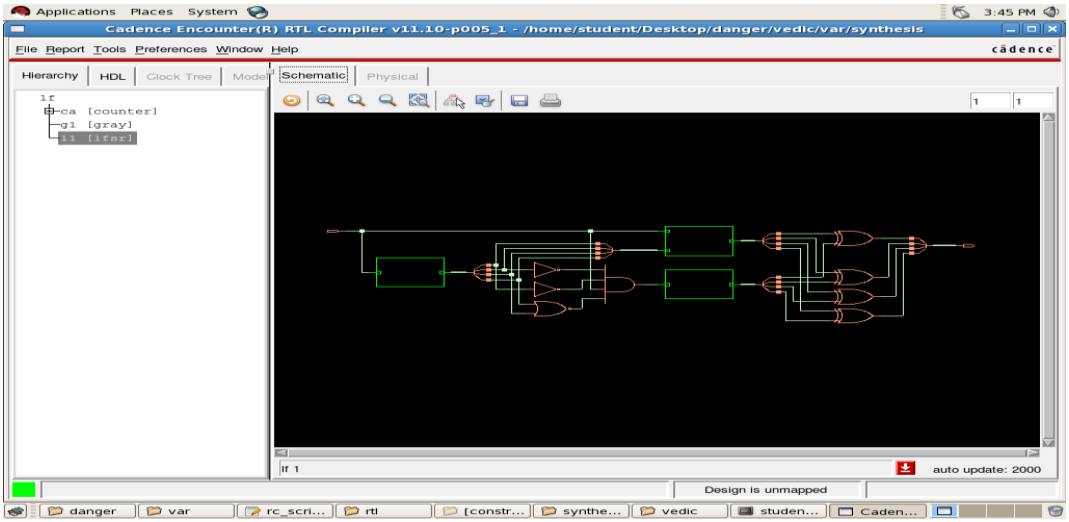

Figure 3. RTL of LPTPG before Optimization

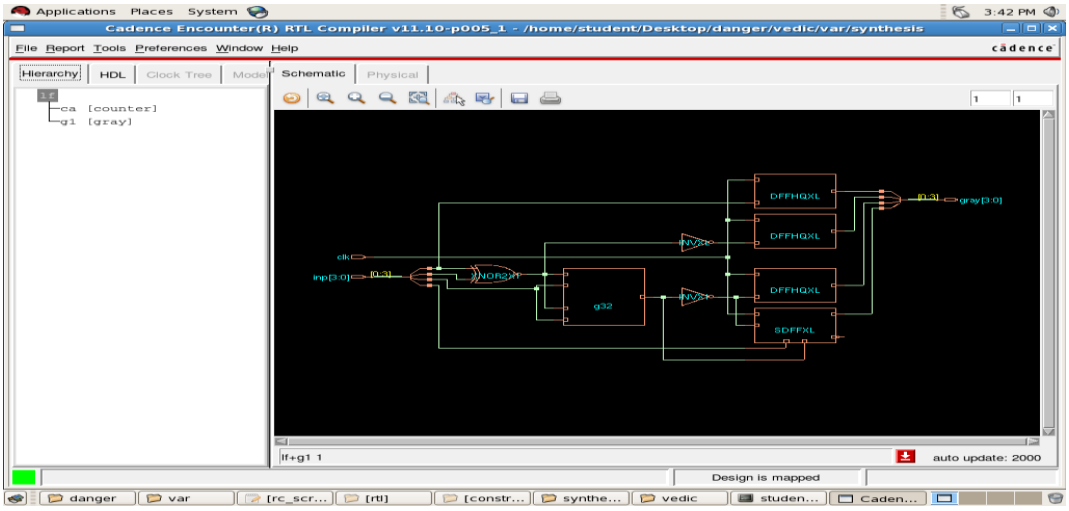

Figure 4. RTL of LPTPG after Optimization

Figure 3 and Figure 4, shows the RTL schematic of the Low Power Test Pattern Generator, before and after optimization respectively. It can be clearly seen that the number of components here reduced as a result of optimization.

Critical path in the circuit is one of the main parameter that has to be taken care while designing a digital integrating circuit. Critical path is defined as the maximum path length from the input to the output. Figure 5, and Figure 6 shows the critical path for LPTPG before and after optimization respectively.

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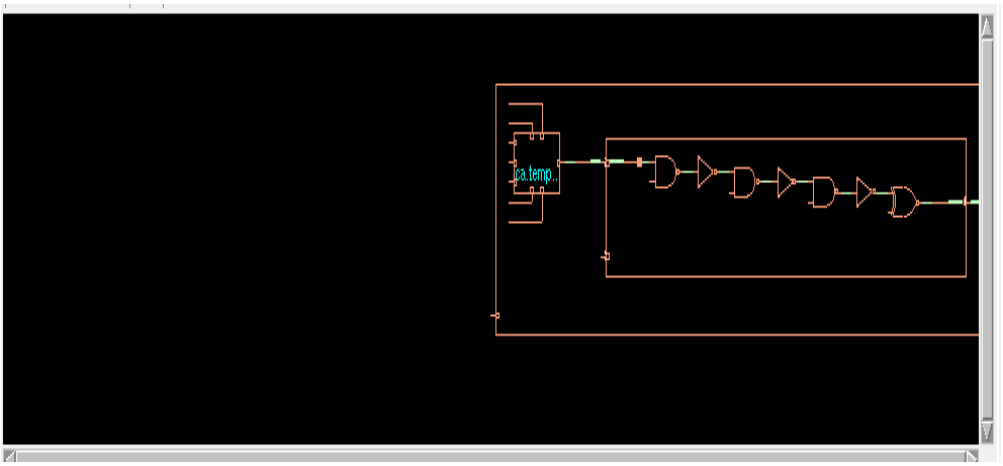

Figure 5. Critical Path for LPTPG before Optimization

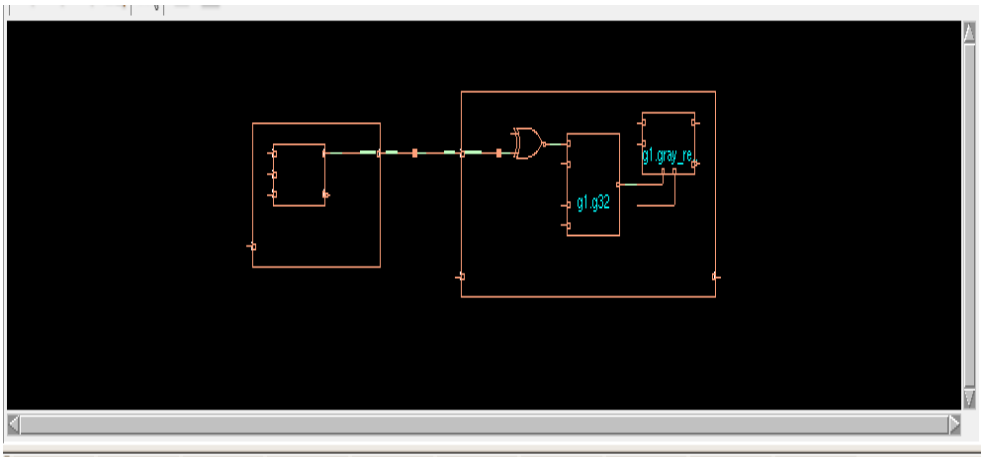

Figure 6. Critical Path for LPTPG after Optimization

The simulation of the low power architecture for Test Pattern Generator is done and the simulation results are shown in Figure 7.

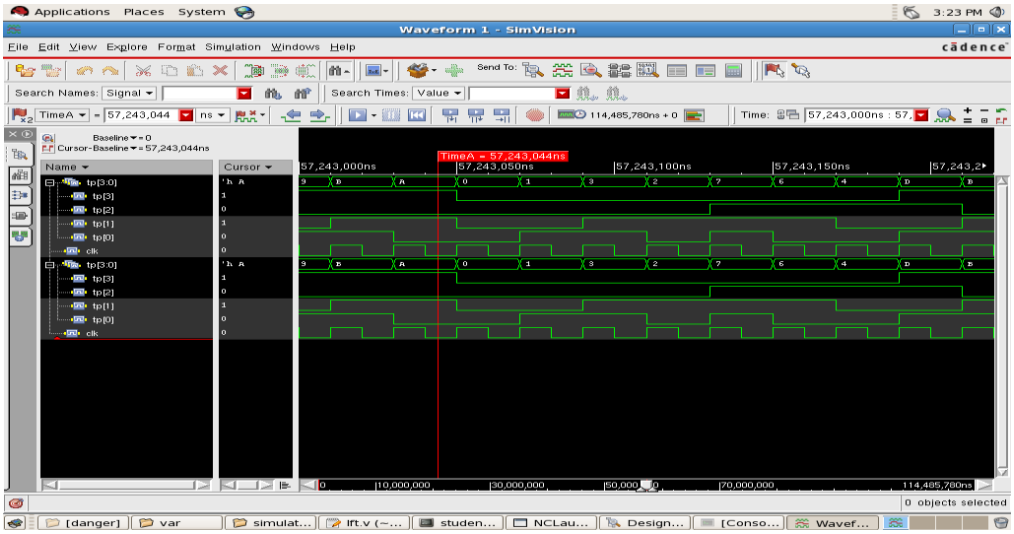

Figure 7. Simulation Waveform

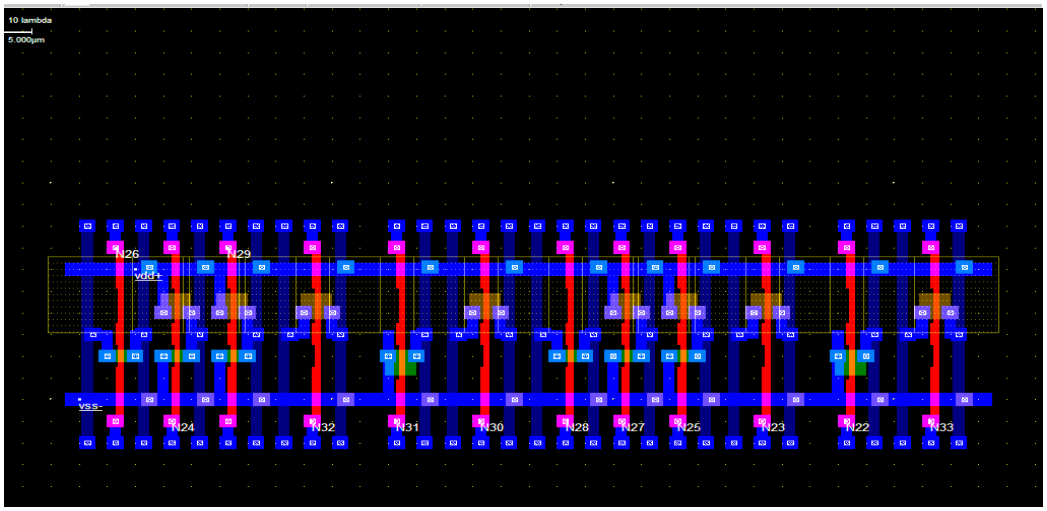

Figure 8. Layout Diagram for 4 Bit LFSR

Layout is drawn for 4 bit LFSR using Microwind tool and is shown in figure 8. This layout serves as a mask which can be transferred to the foundries, in order to manufacture the integrated chip.

The analysis of the design is carried out and the performance parameters are obtained before and after optimization as shown in Table 1.

Table 1. Performance Parameters of LPTPG

Parameters	Power (nw)		Area	Timing (ps)
	Leakage	Dynamic		
Before Optimization	83.762	166712.24	2142	8785
After Optimization	17.77	65865.404	582	8324

Figure 9 and Figure 10 shows the percentage power usage of each and every modules, before and after optimization, respectively. Graphical representation of the performance variation of the LPTPG is presented in Figure 11.

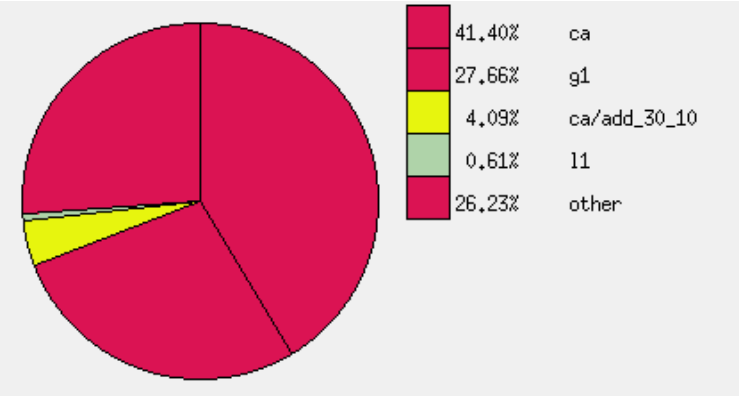

Figure 9. Power Usage of LPTPG before Optimization

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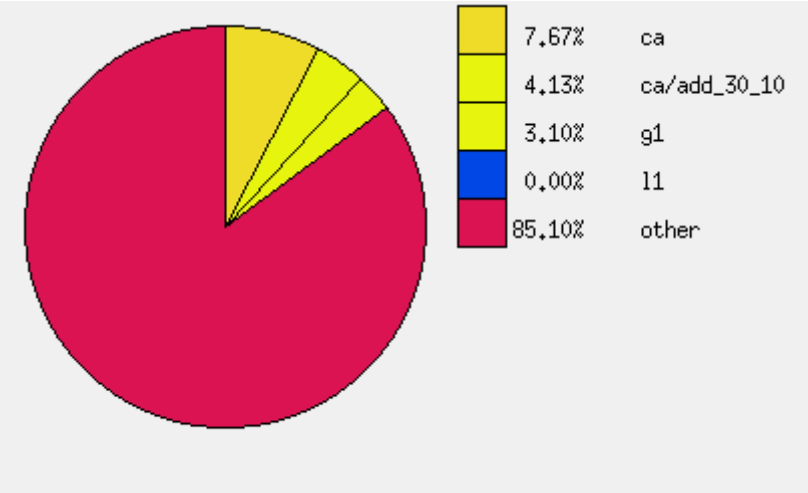

Figure 10. Power Usage of LPTPG after optimization

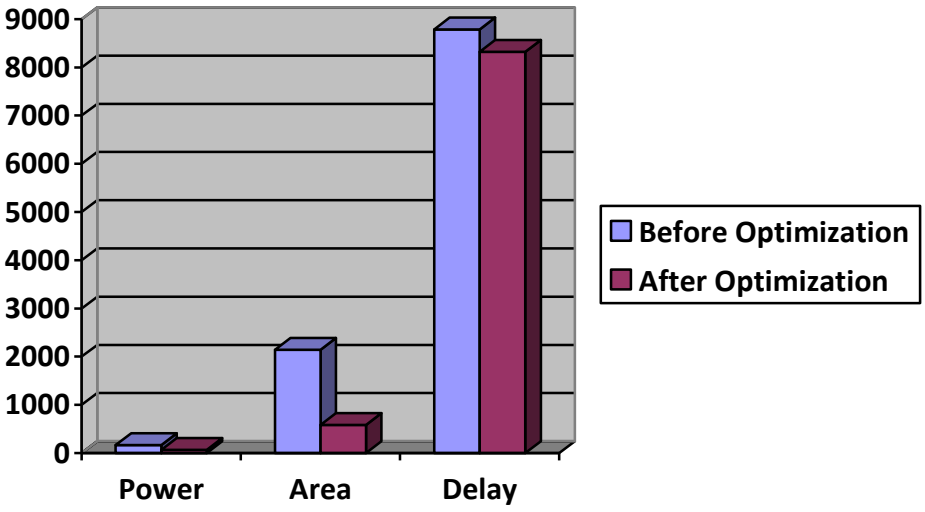

Figure 11. Variation of Performance Parameter

5. Conclusion

In this paper, the implementation of Low Power Architecture for Test Pattern Generator has been implemented. CADENCE EDA tool is used for analysis and simulation of the architecture. The timing analysis has been carried and for the optimum speed. RTL schematic of the architecture is obtained and critical paths are observed. The optimization of the circuit, greatly reduced the power consumption, area and delay. The increasing trends in VLSI has resulted in high speed circuit. The testing of these high speed circuit is very difficult. The test pattern generators are also required to function at the same speed of the circuit under test. As the speed increases, the power consumption also increases. In this paper, efficient design for low power test pattern generator is presented and simulation of the design is performed. Optimization of the design, increased the efficiency of the design to a significant extent.

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Authors

Vardhana M, he completed B.E. in E&C in 2016 from Sahyadri College of Engineering and Management. Currently pursuing M.Tech. In VLSI Design and Embedded Systems, in NMAM Institute of Technology, Nitte. Runner up of the National Level CADENCE Design Contest 2016, organized by CADENCE.

Niju Rajan, she completed B.Tech. in E&C in 2006 from Kerala University. Worked for a year at TKM College of Engineering, Kollam (Aided), in the Department of E&C from August 2007 to August 2008.Joined Department of E&C of NMAMIT, Nitte in September 2008. Completed M.Techh. in Microelectronics and Control Systems from Department of E&E (VTU PG Extension Centre) during 2011-13. Currently working as Asst.Prof. In Department of E&C at NMAMIT, Nitte. Total 9 years of teaching experience. Presented the paper titled "Experimental Investigation on Active Vibration Isolation using Piezo electric Actuators" in the International Conference on Advanced Computing and Communication Systems – 2013, at Sri Eshwar College of Engineering, Coimbatore. This paper had won the Best Paper Award. Presented one paper in an International Journal.

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