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Design Techinque SVL withUltra Low Power FULL-RATE 2:1 MUX

Sanjay singh Kushwah and SaritaBhadauria

ECED, GEC Gwalior, India
Sanjaykushwah15@gmail.com
ECED, MITS, Gwalior, India
saritamits61@yahoo.co.in

Abstract

In this paper, we illustrate a 0.4Tb/s full rate 2:1 MUX. In order to suppress the dilapidation of signals and to increase the operation speed, we designed interconnection for the circuit using self controllable voltage level (SVL) techniques. The circuit shows rise and fall times of about 100fs and consumes 0.5nW. The CMOS logic, such as SVL logic is renewed in this design. The designed circuit is realized in a standard 45nm process and uses 0.7V supply voltage. Our optimization technique using the proposed method reduces power consumption and leakage current by significant amount of multiplexer circuit. The same techniques and architectures are applicable for more advanced semiconductor technologies to push the speed even further.It is easy to tell that our 2:1 MUX attain the highest datarate 0.4Tb/s without increasing much power consumption as compared the data rate 50Gb/s and power to previous work.

Keywords: *MUX, CMO, Low Power, Leakage Current, SVL*

I. Introduction

SERIAL DATA communication systems are operating at throughputs up to 0.4TB/s have been applied to increase the transmission capacity. Until now, communicationsintegrated circuits (ICs) operating at such high speeds have required the use of specialized high-speed technologies, such as GaAs, InP, or SiGe [1–2]. Aggressive technology scaling in CMOS processes, however,over these compound semiconductor technologies fetch a number of advantages. In spite of all these advantages, one key apprehension, namely lower unity-gain frequency, for use in high-speed IC designmakes CMOS typically demanding. Many bandwidth enhancement techniques have been developed to push the operating speed of CMOS circuits near the unity-gain frequency maximum value. Recently, numerous researchers have designed diverse building blocks of a 40-Gb/s transceiver in CMOS technology. In a 120-nm CMOS technology a 40-Gb/s half-rate 2:1 multiplexer (MUX) and 1:2 de-multiplexer (DEMUX) incorporating shunt and series inductive peaking were designed and fabricated [3]. In [4], a 0.18- m CMOS process a 40-Gb/s amplifier and electrostatic discharge (ESD) protection circuit were implemented, featuring shunt and series peaking. More recently, a 40-Gb/s transceiver in 0.13- m CMOS was reported in [5].

At the moment deep-submicron CMOS transistors are accomplished to handle such high switching speeds. In CMOS,thebasic building block is a 2:1 multiplexer which achieves already operating speeds of 25Gb/s [6]In CMOS a 10Gb/s 8:1 multiplexer has been reported [7] and a complete Transmitter with an integrated 16:1 MUX has been published [8]. Low power consumption and low cost is the advantage of CMOS transistors. Lower speed is the drawback of CMOS transistors in comparison to Si-Ge devices. The 20-Gb/s data outputs from two of these retimers will be multiplexed by the half-rate select circuit

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and similar to that used in [9], includes a number of bandwidth enhancement techniques [10]. Knowledge of the minimum low-power mode supply voltage allows a designer to exploit the maximum achievable leakage reduction for a given technology. Understandings of low voltage SRAM data preservation behavior further open the ∂opportunity for aggressive memory supply Voltage minimization, which has been the bottleneck inVLSI system voltage scaling. There are tworenowned techniques that decrease leakage power (PST). Firstly is that to use a multithreshold-voltage CMOS (MTCMOS) [13]. It efficiently reduces PST through the use of high Vt MOSFET switchesby disconnecting the power supply. However, there are major drawbacks through the use of thistechnique, such as the information that both memories and flip-flops based on this technique cannot retain data. The furthertechnique is that to use a variable threshold voltage CMOS (VTCMOS) [14] that decreases PST by increasing the substrate-biases. This technique also faces some crucial problems,due to the substrate-bias supply circuits such as a large area penalty and a large power penalty. To resolve the abovementioned drawbacks, a small leakage current reduction circuit called a self-controllable voltage level (SVL) circuit has been built-up that not only extensively reduces PST, but also retains data during a stand-by period. The amount of gate leakage current has increased gradually and is probable to become analogous or even superior to the sub threshold leakage for future CMOS devices [15]. Which have been proposed to decrease sub-threshold leakage in SRAM cellsof the numerous techniques [16-18], apply a self-controllable switch (SVL) in active mode which allows full supply voltage to be applied and decreased supply voltage appears to be particularly proficient for reducing gate leakage currents as well.In low power design, it is difficult to suppress leakage current. In memory, Leakage power reduction duringdata-retention in SRAM standby is often addressed by reducing the supply voltage.

II. Conventional 2:1 MUX

In electronics, a multiplexer is a device that selects one of several analog or digital input signals and forwards the selected input in to a single line. A multiplexer of 2^n inputs has n select lines, which are used to select which input line to send to the output. Multiplexers are mainly used to increase the amount of data that can be sent over the network within a certain amount of time and bandwidth. A Multiplexer is also called the data selector. They are used in CCTV, and almost every business that has CCTV fitted, will own one of these. An electronic multiplexer make it possible for several signals to share one device or resource, for example one A/D converter or communication line, instead of having one device per input signal. An electronic multiplexer can be considered as a multi input, single output switch. In telecommunications and signal processing, an analog time division multiplexer (TDM) may take several samples of separate analogue signal and combine them into one pulse amplitude modulated (PAM) wide-band analogue signal. Alternatively a digital TDM multiplexer may combine a limited number of constant bit rate digital data streams into one data stream of a higher data rate, by forming data frames consisting one timeslot per channel.

Process variations are posing a major challenge to nano scale integrated circuits design. Various criteria have been formulated in the past for analytically calculating the worst-case static noise margins of logic circuit.

In Digital circuit design, the selector wire is of digital value. In case of 2-to-1 multiplexer a logic value of 0 would connect to I_0 to the output while the logic value of 1 would connect I_1 to the output.

A 2-to-1 multiplexer has a Boolean equation where A and B are two inputs Sel (S) is the selector input and Vout is the output.

$Vout = (A.S_0) + (B.S_1)$

A straightforward realization of 2-to-1 MUX would need 2 AND gate, an OR gate and a NOT gate. Symbol Diagram of 2:1 MUX is shown in Figure 1, Schematic of conventional

2:1 MUX is shown in Figure 2 and the output waveform of conventional 2:1 MUX is shown in Figure 3.

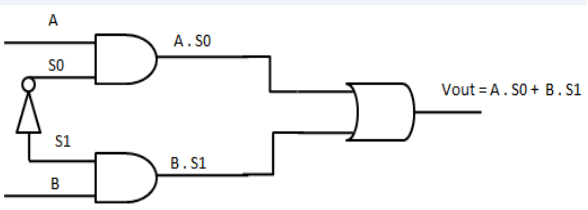

Figure 1. Symbol Diagram of 2:1 MUX

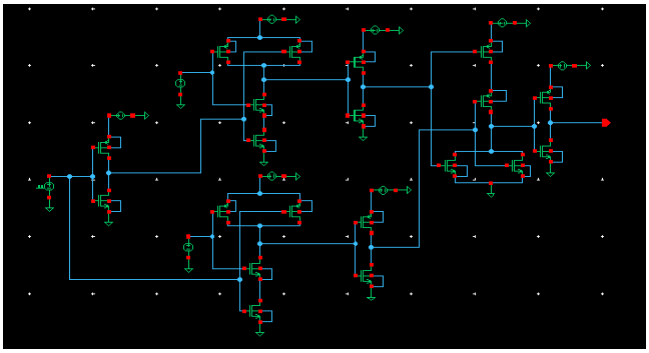

Figure 2. Schematic of Conventional 2:1 MUX

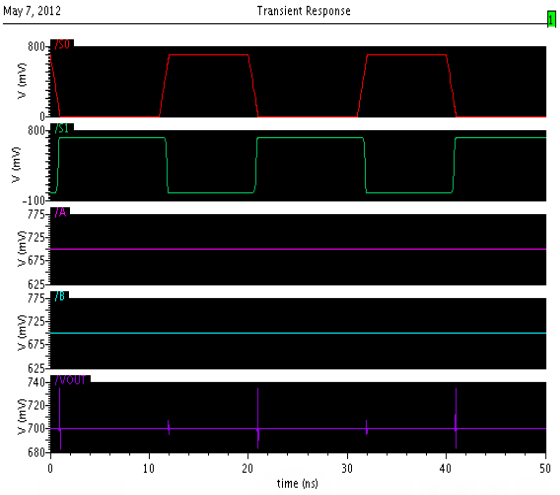

Figure 3. Ouput Waveform of Conventional 2:1 MUX

III. SVL Technique Applied in 2:1 MUX

The standby leakage power and the leakage current reduction circuit is known as self controlable voltage level (SVL).The SVL circuit consists of an upper SVL (U-SVL) circuit and a lower SVL (L-SVL) circuit, Where 2:1 MUX has been used as the load circuit.

There are three types of Self Controllable Voltage Level(SVL):

A. Upper SVL Circuit

Upper SVL consists of a single pmos1v (PM13) and m- nmos1v (NM12,NM14) connected in series. The "on- pmos1v" connects a power supply (V_{DD}) and the MUX circuit is in active mode on demand, and "on nmos1v" connect power supply (V_{DD}) and the MUX circuit is in standby mode.The schematic of Upper SVL (U-SVL) is shown in Figure 4 and the Otput waveform of 2:1 MUX with U-SVL is shown in Figure 5.While

gate voltage (VG) of the stand-by MUX circuitis kept at "0", the pmos1v is turned on while the nmos1v is turned off. When control signal (USVLin) turns on nmos1v (NM12) and turns off pmos1v, $V_{DD}$is supplied to the MUX circuit through m-nmos1v. Thus, a drain-to-source voltage (Vdsn),that is, a drain voltage (V_D) of the "off nmos1v", can beexpressed as

$$Vdsn = V_{DD} - mv \quad (1)$$

Where vis a voltage drop of the single nmos1v and Vdsn can be changed by varying mor v(or both). Reducing Vdsnbyrisingmvwill increase the barrier height of the "off nmos1v"; that is, it will reduce the draininduced-barrier-lowering (DIBL) effect and, as a result, increase Vthn. This results in a decrease inthe subthreshold current of the nmos1v (Istn); that is, the leakage current through the MUX circuit decreases.

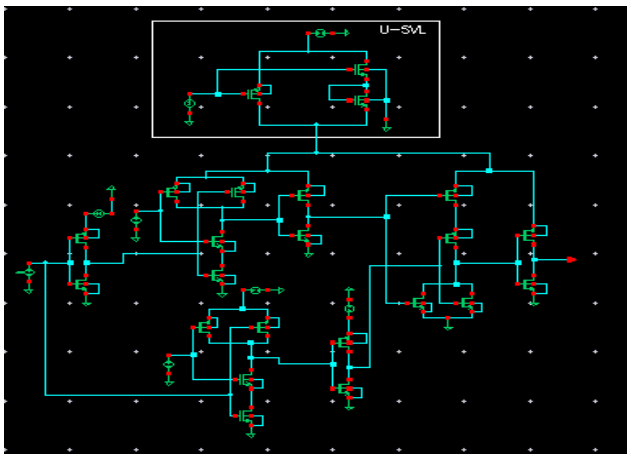

Figure 4. Schematic of 2:1 MUX with USVL Circuit

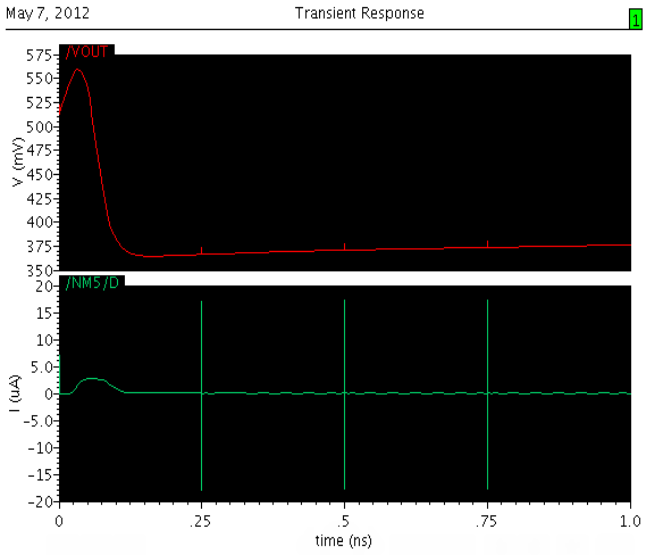

Figure 5. Output Waveform of 2:1 MUX with U-SVL Circuit

B. Lower SVL Circuit

The Lower SVL circuit, which incorporate a single nmos1v (NM3) and m-pmos1v (PM1, PM3) connected in series, is positioned between a ground-connection (V_{SS}) and the MUX circuit. The L-SVL circuit not only ground connection V_{SS} to the active MUX circuit through the "on nmos1v" but also supplies V_{SS} to the standby MUX circuit through the use of the " on pmos1v".The schematic of 2:1 MUX with L-SVL Circuit is shown in Fig6 and

the output waveform of 2:1 MUX with L-.SVL is shown in Figure 7. A negativecontrol signal (LSVLin) turns on pmos1v (PM1) and turns off nmos1v so that V_{SS} is supplied to the stand-by MUX circuit with VG of "0" (*i.e.*, mv) through m-pmos1v. Thus, according to Equation (1), reduced Vdsn reduces Istn. Furthermore,source voltage (VS) is increased by mv, so the substrate bias (*i.e.*, back-gate bias) (Vsub), expressed by

Vsub = – mv (2)

Both the reduction in the DIBL effect and the increase in the back-gate bias (BGB) effect lead tofurther increase in Vthn.

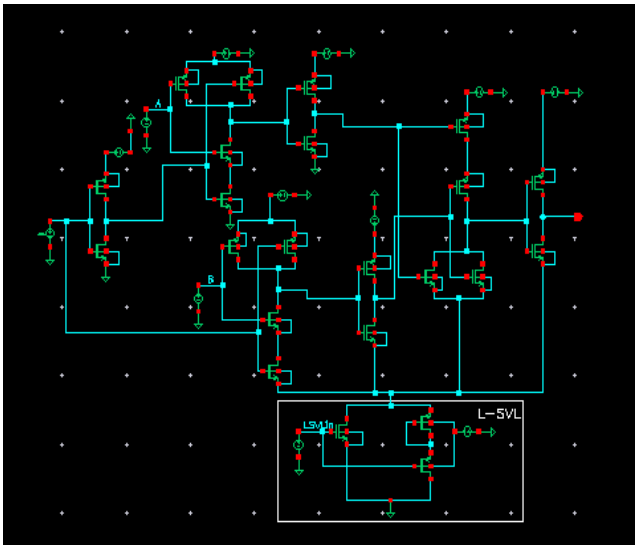

Figure 6. Schematic of 2:1 MUX with LSVL Circuit

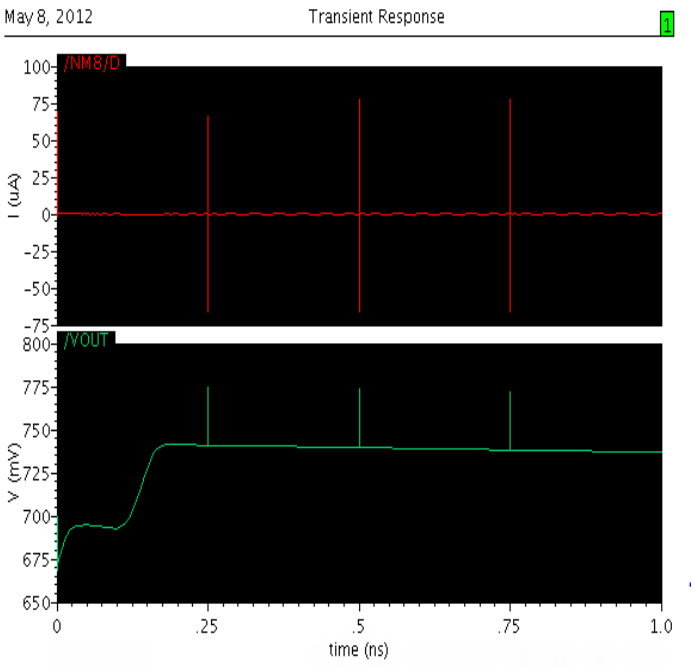

Figure 7. Output Waveform of 2:1 MUX with LSVL Circuit

C. SVL Circuit

While the MUX circuit is in the active mode, the built-up SVL circuit supplies the maximum DC voltages (V_{DD}& V_{SS}) to them through U-SVL and L-SVL circuits both are

turned on simultaneously. Thus the 2:1 MUX circuit can operate quickly. On the other hand, when the MUX circuit is in standby mode, it supplies to some extent lower V_{DD} and relatively higher V_{SS} to them through "on SVL", so the drain source voltages of the "off MOSFET" in the standby MUX circuit decreases and Vsub increases. Thus, Vth increases and consequently, sub threshold current decreases, so (standby power) Pst is reduced, While data are retained and noise immunity is high. In the "cut-off" MOSFETs the increase in VBGs will increase the Vts. The schematic of 2:1 MUX with SVL circuit is shown in Figure 8 and Output Waveform of 2:1 MUX with SVL Circuit is shown in Figure 9. The DIBL effect on nmos1v in the stand-by MUX circuitincorporating the SVL circuit is further decreased,since Vdsn in this case can be expressed as

$Vdsn = V_{DD} – 2mv.(3)$

The BGB effect due to Vsubwhich is given in equation (2) also occurs.

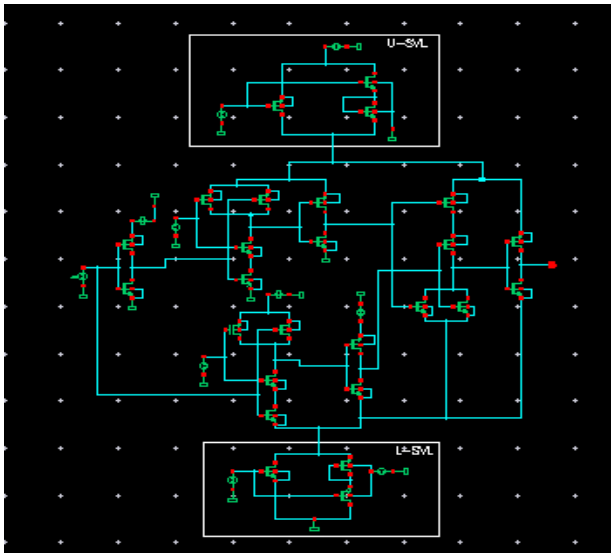

Figure 8. Schematic of 2:1 MUX with SVL Circuit

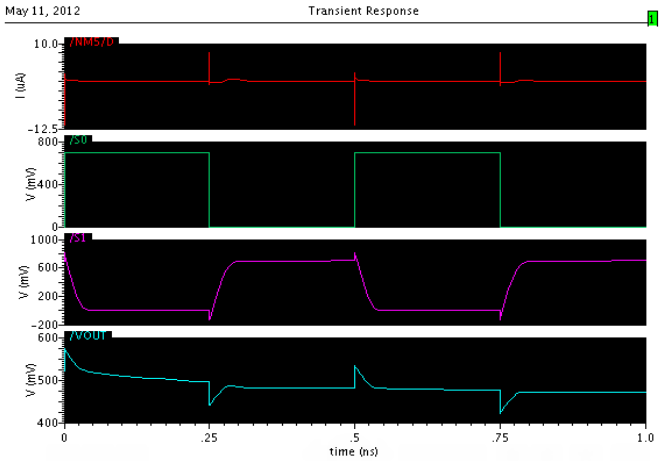

Figure 9. Output Waveform of 2:1 MUX with SVL Circuit

IV. Simulation Result

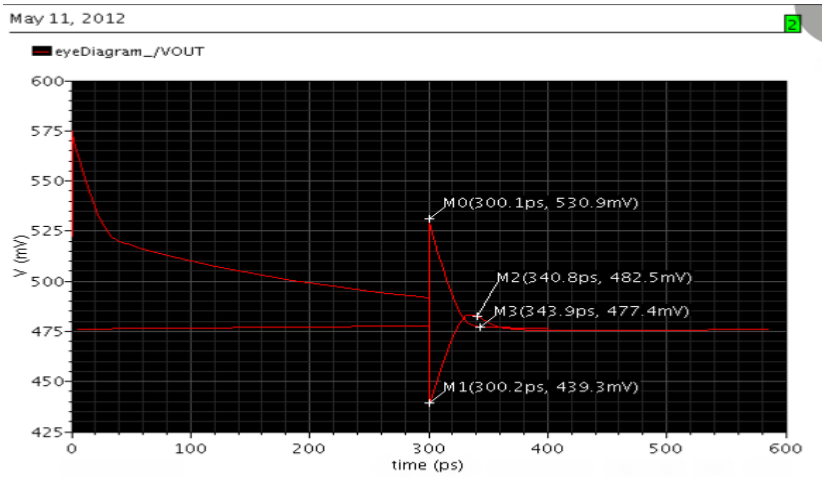

Figure 10. Measured 0.4Tb/s Eye Diagram

Furthermore, accuracy of the circuit is validated by measurements in [11]. It is shown that the measured energy is in the near locality of the simulated energy dissipation. The MUX circuit often limits the operation speed of the whole system. This is the reason why high-speed circuits in communication system working at data bit rate higher than 0.4Tb/s are dominated by technologies such as SiGe, GaAs and InP. Eye diagram of the differential output signal at a data rate of 0.4Tb/s. The circuit shows a wide opened eye up to 0.4Tb/s. Measured eye diagram is shown in Fig10. Simulation result is measured by CANDENCE VIRTUOSO Tool .The Simulation result is summarized in TABLE 1.

a) SIMULATED RESULT SUMMARY

Table Head	**TECHNIQUE APPLIED TO 2:1 MUX**			**Compare with previous work**
	USVL	***LSVL***	***SVL***	***MUX***
Process technology	45nm CMOS	45nm CMOS	45nm CMOS	180nm CMOS
Supply Voltage	0.7V	0.7V	0.7V	1.8V
Rise time	100fs	100fs	100fs	-
Fall time	100fs	100fs	100fs	-
Power Dissipation	1.915nW	1.032nW	0.5nW	108mW
Leakage Current	1.09nA	1.028nA	1.020Na	-
Data bit Rate	-	-	0.4Tb/s	40-43Gb/s

V. Conclusion

The effect of the SVL circuit on the Leakage Current and Leakage Power through the 2:1 MUX Circuit (*i.e.*, reduction in current and power) were examined. The SVL circuit and the 2:1 MUX were designed using 45nm technology CMOS technology. A SVL circuit, which can significantly decrease (stand-by-power) Pst and noise immunity is high. While maintaining high speed performance, has been developed. A full-rate 0.4-Tb/s 2:1 MUX was fabricated and measured in 45- nm CMOS technology. The simulation proves that it operates well at 0.4 Tb/s less than 27^{o} temperatures with only about 0.5 nW power consumption. The same techniques and architectures are applicable for more advanced semiconductor technologies to push the speed even further. It is easy to tell that our 2:1

MUX achieve the highest data rate without increasing much power consumption as compared to previous work.

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