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Design FPGA-Based CL-Minimum Control Unit

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Abstract

Most of controllers need real time mobility operation so one of the most important devices which can be used to solve this challenge is Field Programmable Gate Array (FPGA). FPGA can be used to design a controller in a single chip Integrated Circuit (IC). To have higher implementation speed with good performance cMinimum Control Unit (MCU) is implemented on Spartan 3E FPGA using Xilinx software.

Design a 4 bits Field Programmable Gate Array (FPGA)- based carry lookahead MCU is the main challenging works. MCU is control unit to control of data transfer between input and output and process the input data. In this research, MCU is used to control the 4 bits, Arithmetic Logic Unit (ALU). Combinational logic characterized by its propagation delay and contamination delay. To reduce the delay hardware description language (HDL) type of programming is very important. To reduce the route delay and logic delay, type of HDL design is very important. In this research, we used lookahead design, which reduce about 10% delay in comparison with ripple carry.

Keywords: *Real-time operation, Field Programmable Gate Array (FPGA), improved partly sliding mode control, PUMA robot manipulator, VHDL, Xilinx, sampling time*

1. Introduction

The word digital has made a dramatic impact on our society. More significant is a continuous trend towards digital solutions in all areas – from electronic instrumentation, control, data manipulation, signals processing, telecommunications *etc*., to consumer electronics. Development of such solutions has been possible due to good digital system design and modeling techniques.

Digital ICs have become universally standardized and have been accepted for use. Whenever a designer has to realize a digital function, he uses a standard set of ICs along with a minimal set of additional discrete circuitry [1].

Field programmable Gate Arrays (FGPAs) are reconfigurable devices that can be electrically programmed to implement a wide variety of logic circuits. An FPGA consists of a uniform array of programmable logic structures that are interconnected by a configurable routing grid. Originally designed to serve as prototyping devices for testing and demonstrating the functionality of digital circuits, FPGAs are now an integral part of high performance systems that include digital, analog and RF components. The revolutionary success of these reconfigurable devices can be attributed to Flexibility in design implementation. The ability to instantly reprogram the FPGA with various circuits at no extra cost promotes reusability of the device, allows rapid design verification and reduces non recurring expenditure. The uniform logic and interconnect structures along with modern CAD tools simplify back-end tasks such as placement and routing [2].

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- The availability of high performance FPGA based IP cores for popular applications. This allows FPGAs to function as plug and play devices in System on Chip (SoC) platforms
- Enhanced performance due to the incorporation of specialized hardware like multipliers, high speed memories *etc.*, into the FPGA. Additionally, the specialized blocks are also optimized for area and power which making the FPGA more competitive with custom chips.

Figure 1 shows the island style of FPGA architecture.

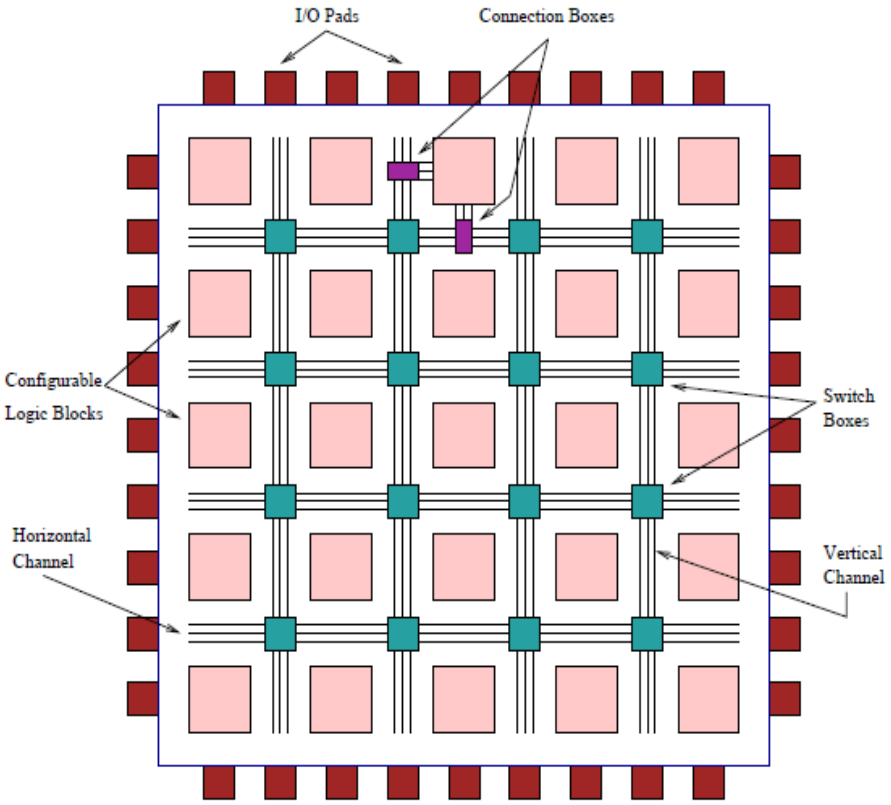

Figure 1. Island Style of FPGA Architecture

The island style FPGA (as shown in Figure 1) is so named as it consists of a uniform two-dimensional array of logic blocks surrounded by a sea of interconnect. The FPGA interfaces with other devices through programmable input output blocks that line the periphery of the chip. The routing fabric is divided into horizontal and vertical channels interconnected through switches. Logic blocks or Configurable Logic Blocks (CLBs) as they are more commonly known, consist of a set of internally interconnected basic logic elements (BLEs) [3-4]. As shown in Figure 2, each BLE comprises of a Lookup table (LUT), a flip-flop and a multiplexer. A k input LUT has 2^k SRAM bits and can implement a k input truth table with 2^k entries. If the BLE is to implement sequential logic, the output of the LUT is stored in the flip-flop. In the case of combinational functions, the output bypasses the flip-flop and is sent through to the programmable multiplexer. Depending on the FPGA architecture, n BLEs are clustered to form a single CLB through local interconnects. To provide maximum flexibility, all inputs to the CLB and all outputs of the n BLEs are connected to each BLE through the local interconnect and decoding logic [5-6].

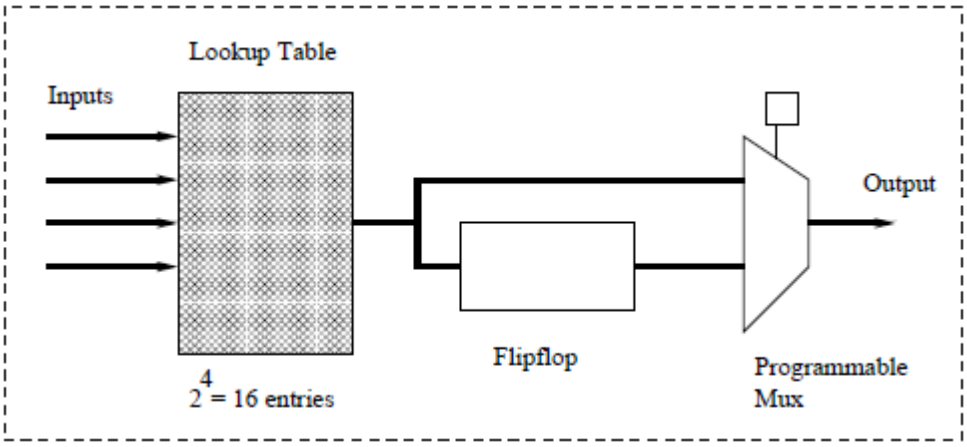

Figure 2. Basic Logic Elements (BLE) Architecture

Figure 3 illustrates an example of a CLB consisting of 4 BLEs. The CLB has 10 inputs, which, along with the outputs of the 4 BLEs can be configured as inputs to the LUTs of the BLEs.

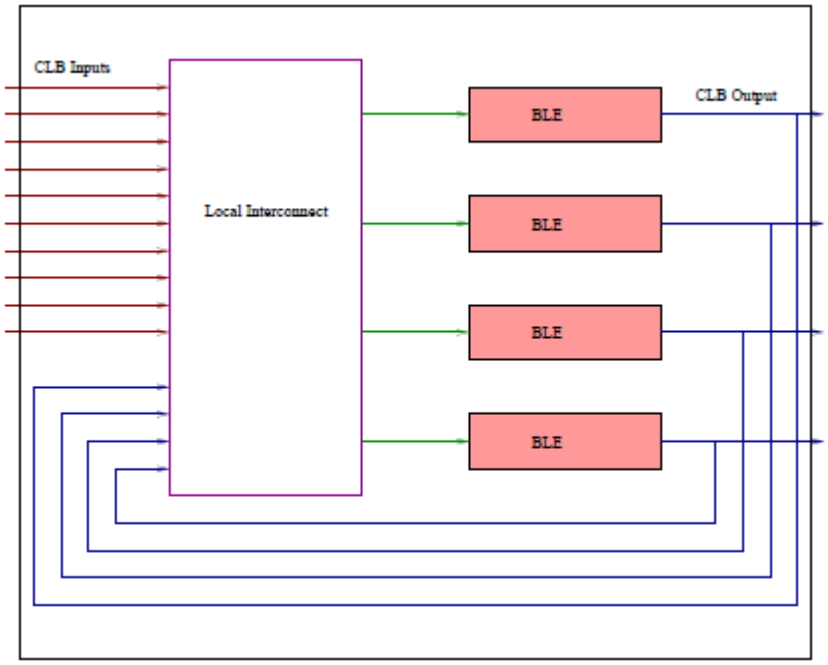

Figure 3. Configurable Logic Block (CLB): Hierarchical Representation

Connectivity between CLBs is achieved through horizontal and vertical routing segments (tracks or wires) that run in channels between CLBs. The number of segments in each channel is known as the channel width (Wc). In the single segment architecture all routing channels consist of tracks of the same length (spanning one CLB). However, most commercial FPGAs adopt a more complex routing structure in which channels consist of tracks of varied lengths. We refer to such architectures as multi segment routing architectures. Figure 4 shows a sample multi segment routing architectures with track lengths of 1 and 4, *i.e.*, each track spans either 1 or 4 CLBs [7].

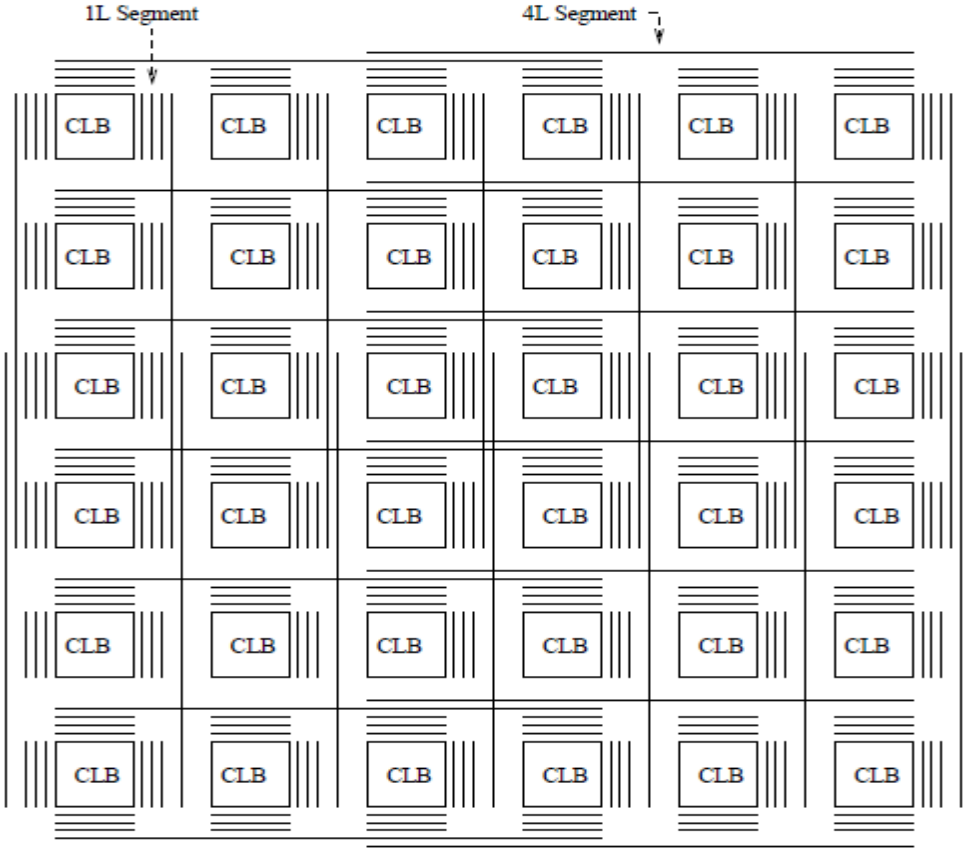

Figure 4. Multi Segment Routing Architecture

2. THEORY

The first part to design Minimum Control Unit is adders. The Table 1 shows the two bits half adder.

Table 1. Two Bits Half Adder Truth Table

A_1	A_0	C	S
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

$$S = A_0 \oplus A_1$$
$$C = A_0 A_1 \quad \textbf{(1)}$$

Figure 5 shows the half adder circuit.

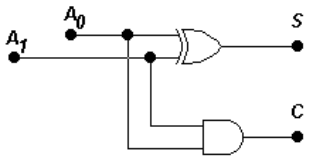

Figure 5. Half Adder

Full Adder: A full adder adds binary numbers and accounts for values carried in as well as out. A one-bit full adder adds three one-bit numbers, often written as $A, B, and\ Cin$; A and B are the operands, and Cin is a bit carried in from the previous less significant stage. Table 2 shows the truth Table.

Table 2. Full Adder Truth Table

A	B	C_{i-1}	C_i	S_i
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

Figure 6 shows the block diagram of full-adder.

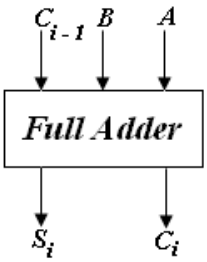

Figure 6. Full Adder

$$S = A \oplus B \oplus C_{i-1}$$
$$C_i = AB + (A \oplus B).C_{i-1} \quad \textbf{(2)}$$

Ripple-Carry Adder: It is possible to create a logical circuit using multiple full adders to add $N - bit$ numbers. Each full adder inputs a Cin, which is the $Cout$ of the previous adder. This kind of adder is called a ripple-carry adder, since each carry bit "ripples" to the next full adder. Note that the first (and only the first) full adder may be replaced by a half adder. Figure 7 shows the parallel full adder.

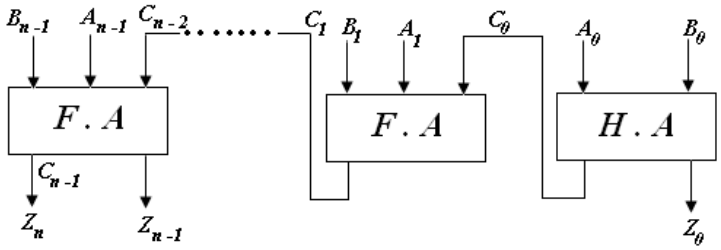

Figure 7. Ripple-Carry Adder

The delay time in ripple carry computed as:

$$T_{ripple} = N \times t_{FA} \quad (3)$$

Carry-Lookahead Adder: By combining multiple carry lookahead adders even larger adders can be created. This can be used at multiple levels to make even larger adders. Carry lookahead adders use generate (G) and propagate (P) signals that describe how a column or block determines the carry out.

$$C_i = A_i B_i + (A_i + B_i) C_{i-1} = G_i + P_i C_{i-1} \quad (4)$$

$$G_{n:0} = G_n + P_n(G_{n-1} + P_{n-1}(G_{n-2} + p_{n-2})G_{n-3} + \cdots \quad (5)$$

$$P_{n:0} = P_n P_{n-1} \cdots \quad (6)$$

The delay in this method is:

$$T_{CLA} = t_{pg} + t_{pg-block} + \left(\frac{N}{K} - 1\right) t_{AND-OR} + K t_{FA} \quad (7)$$

Decoder: A decoder is a circuit that changes a code into a set of signals. It is called a decoder because it does the reverse of encoding, but we will begin our study of encoders and decoders with decoders because they are simpler to design. Figure 8 shows the decoder.

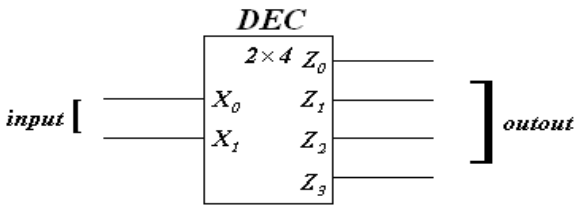

Figure 8. Digital Decoder

Table 3 shows the truth Table for digital encoder.

Table 3. Digital Decoder Truth Table

input's		output's			
X_1	X_0	Z_3	Z_2	Z_1	Z_0
0	0	0	0	0	①
0	1	0	0	①	0
1	0	0	①	0	0
1	1	①	0	0	0

Multiplexer: In electronics, a multiplexer (mux) is a device that selects one of several analog or digital input signals and forwards the selected input into a single line. A multiplexer of 2^n inputs has n select lines, which are used to select which input line to send to the output. Figure 9 shows 4:1 Mux.

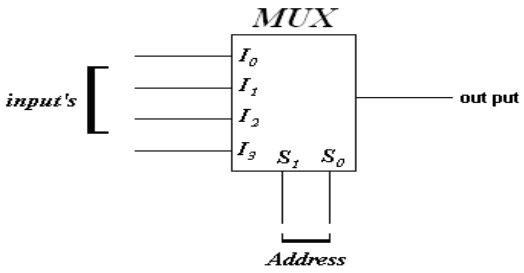

Figure 9. 4:1 Multiplexer

Register: Registers are data storage devices that are more sophisticated than latches. A register is a group of binary cells suitable for holding binary information. A group of cascaded flip flops used to store related bits of information is known as a register. Figure 10 shows T flip-flop.

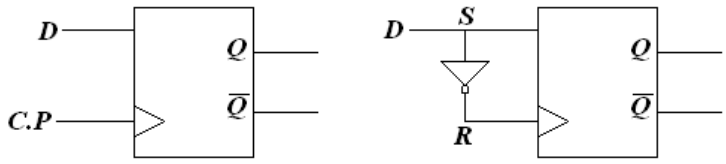

Figure 10. T Flip Flop

3. Methodology

Design 4 bits FPGA based Arithmetic Logic Unit: A typical ALU performs the following functions:

1. 4 bits full adder
2. 4 bits subtractor
3. 4 bits exclusive OR
4. 4 bits Exclusive NOR.

To design arithmetic unit (AU) first, FPGA-based ripple carry adder is design. Figure 11 and 12 show FPGA-based ripple carry adder and FPGA based carry lookahead.

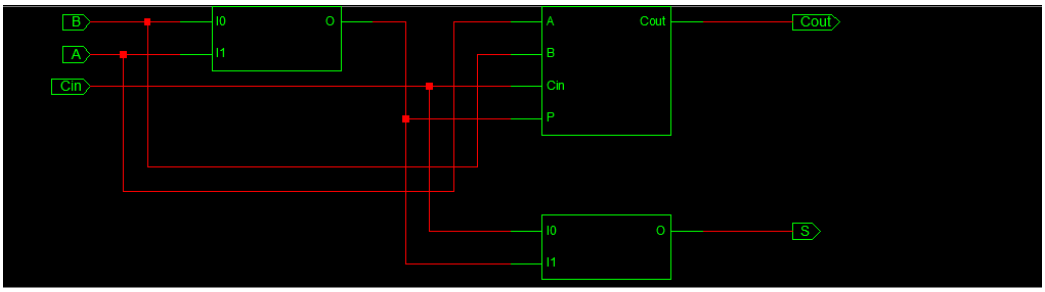

Figure 11. FPGA-based Ripple Carry Adder

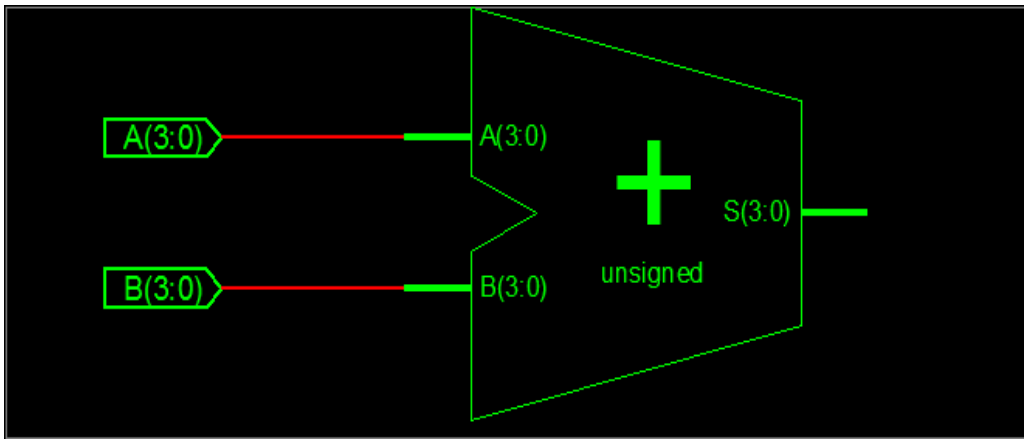

Figure 12. FPGA-based Carry-lookahead Adder

In second step, FPGA-based sub-tractor is design. Figure 13 and 14 shows FPGA-based ripple carry and lookahead sub-tractor.

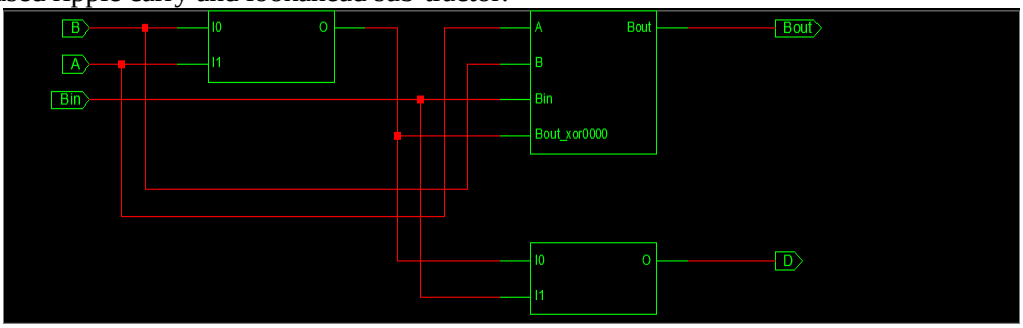

Figure 13. FPGA-based Ripple Carry Sub-Tractor

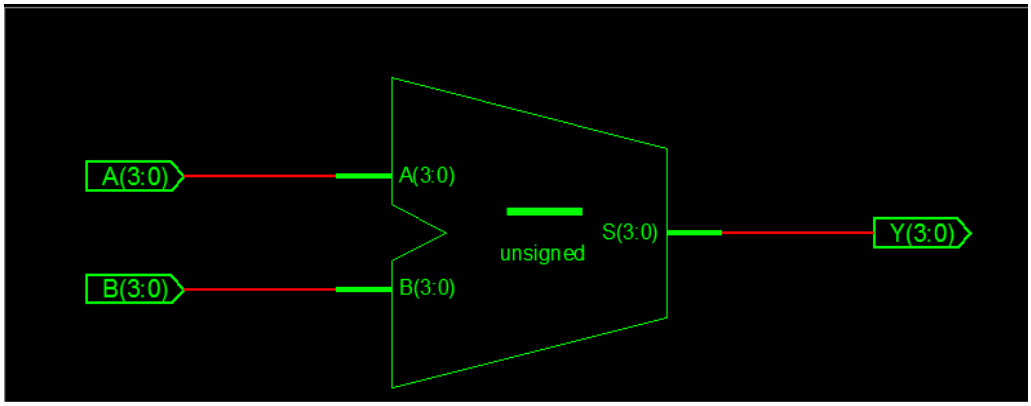

Figure 14. FPGA-based Carry Lookahead Sub-Tractor

The FPGA-based ripples carry and carry lookahead arithmetic unit (AU) is design in the next step. The Figure 15 and 16 show these circuits.

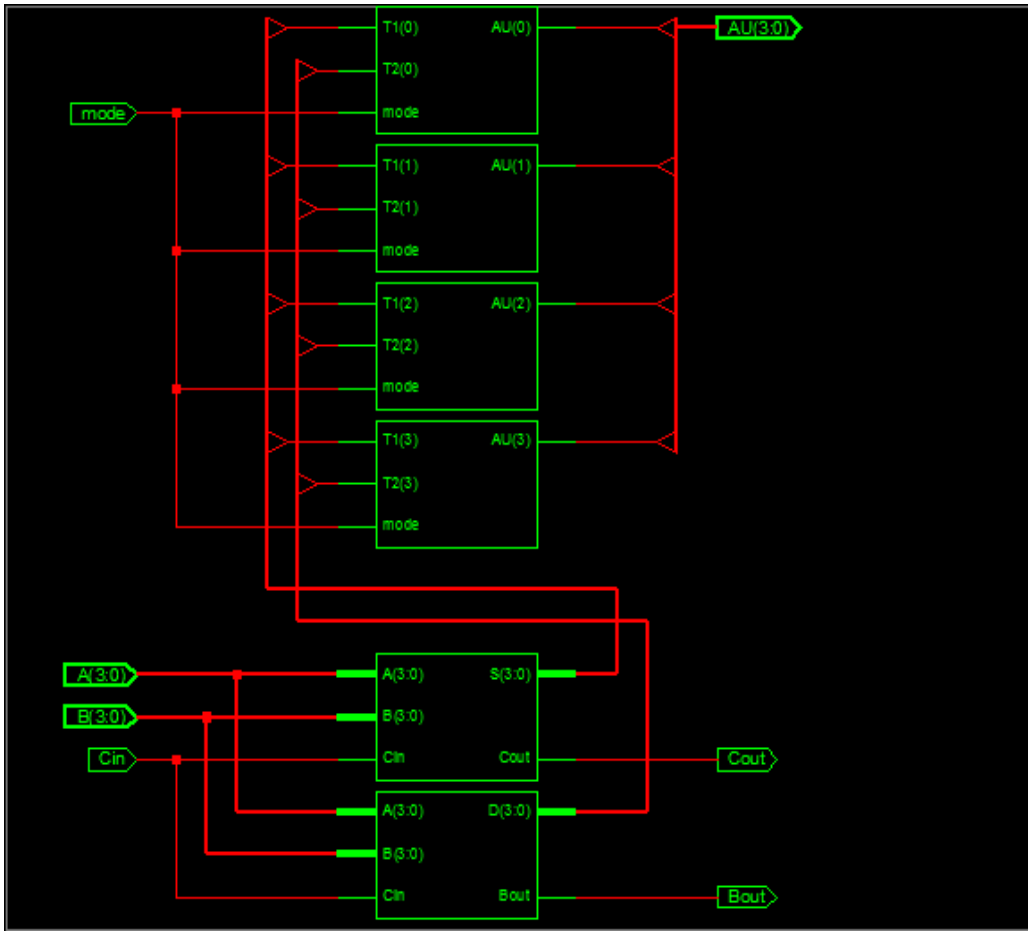

Figure 15. FPGA-based Ripple Carry AU

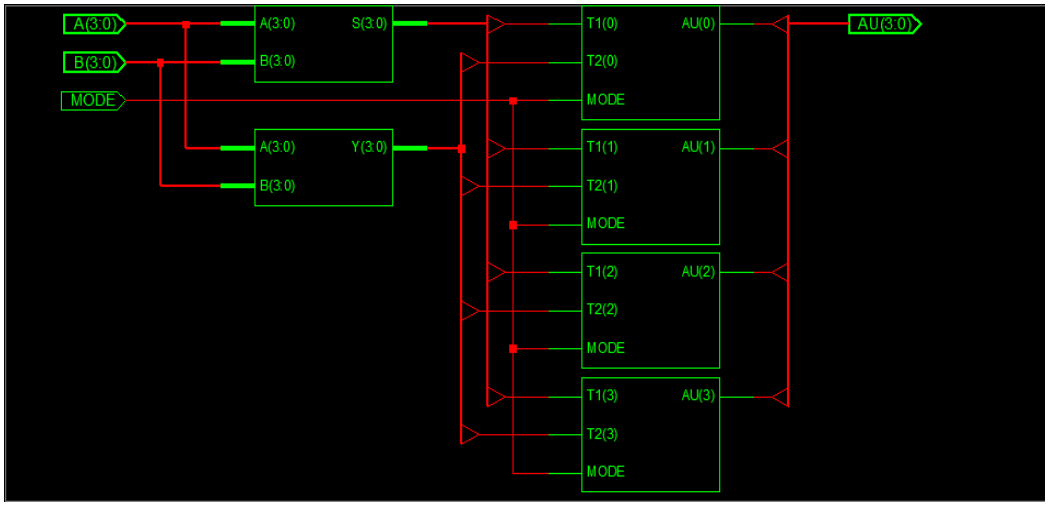

Figure 16. FPGA-based Carry Lookahead AU

Figure 17 and 18 illustrate FPGA-based ripple carry and carry lookahead arithmetic logic unit (ALU).

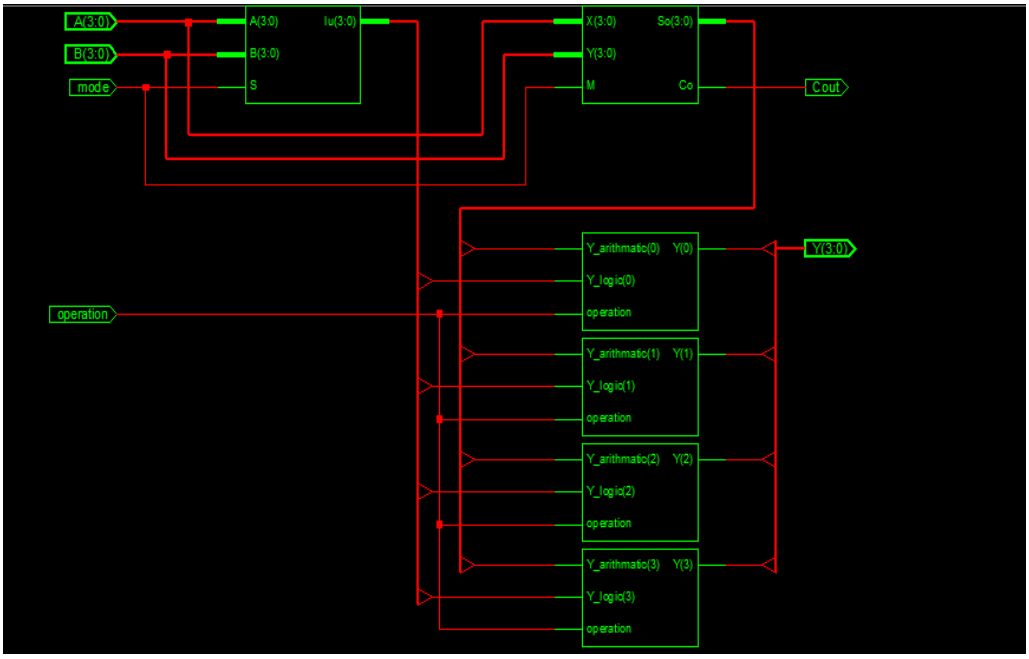

Figure 17. FPGA-based Ripple Carry ALU

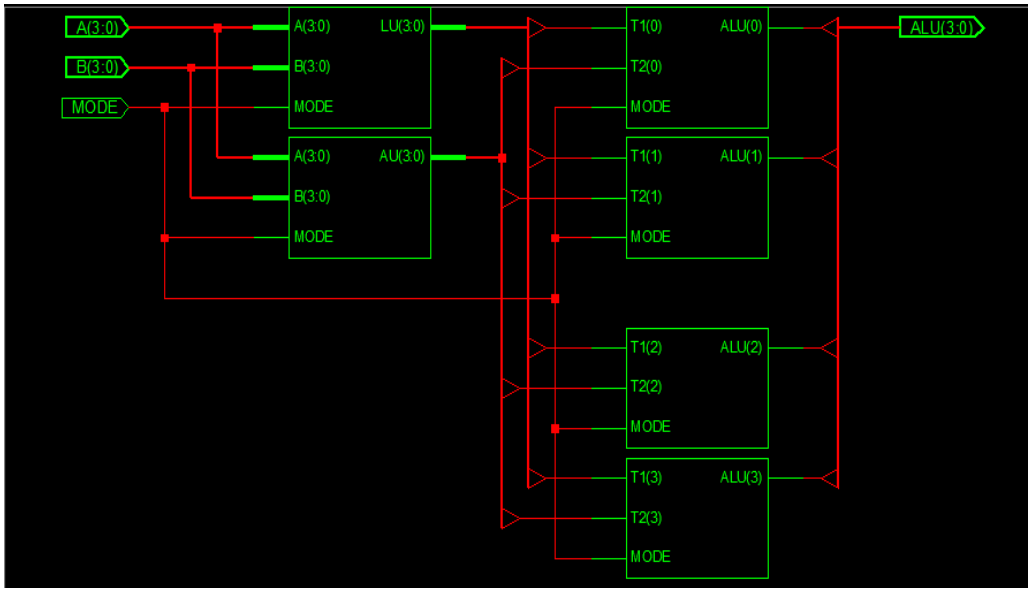

Figure 18. FPGA-based Carry Lookahead ALU

MCU=MIPS (originally an acronym for Microprocessor without Interlocked Pipeline Stages) is a reduced instruction set computer (RISC) instruction set architecture (ISA) developed by MIPS Technologies (formerly MIPS Computer Systems, Inc.). The early MIPS architectures were 32-bit, with 64-bit versions added later. Multiple revisions of the MIPS instruction set exist, including MIPS I, MIPS II, MIPS III, MIPS IV, MIPS V, MIPS32, and MIPS64. The current revisions are MIPS32 (for 32-bit implementations) and MIPS64 (for 64-bit implementations). Figure 19 shows 4 bits MCU.

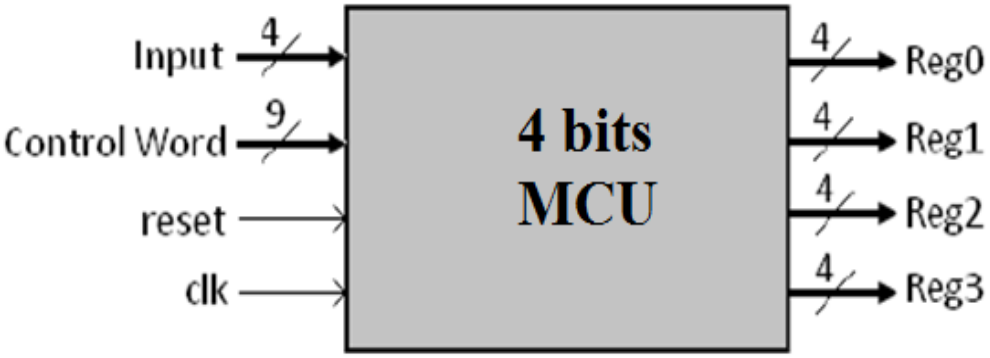

Figure 19. 4 Bits MCU

The controller details are illustrated in the following Figure (Figure 20).

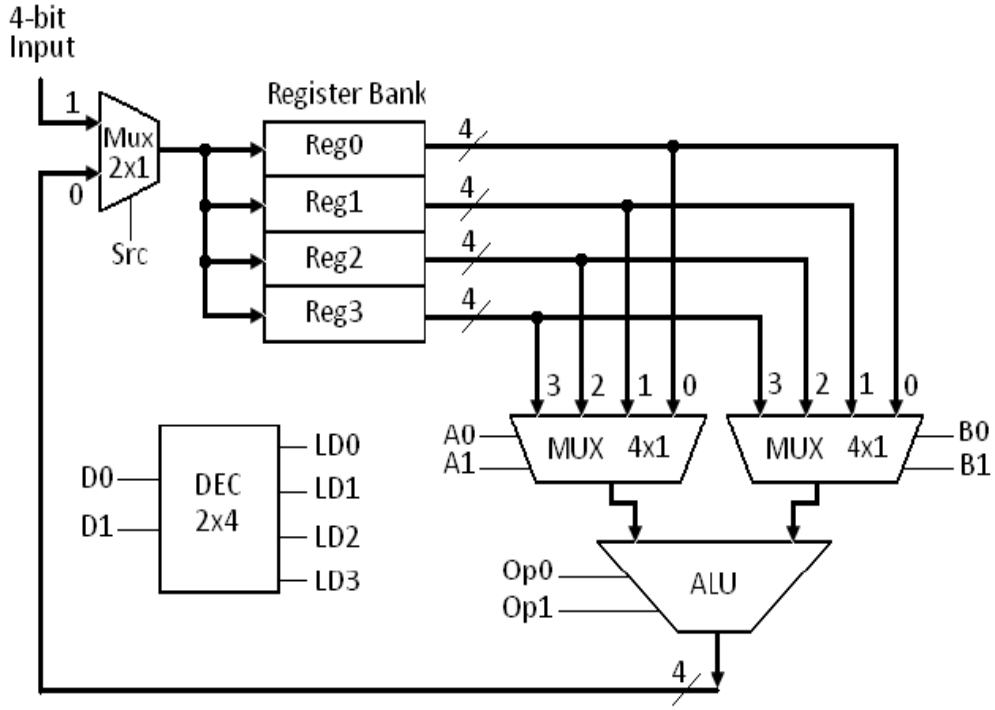

Figure 20. Minimum Control Unit Details

In this research we have 9 bits control words as follows: $D0, D1, OP0, Op1, A0, A1, B0, B1, Src$. Table 4 illustrates the location of control bits.

Table 4. Location of Control Words

8								0
Src	D1	D0	B1	B0	A1	A0	Op1	Op0

The FPGA-based MCU shows in Figure 21.

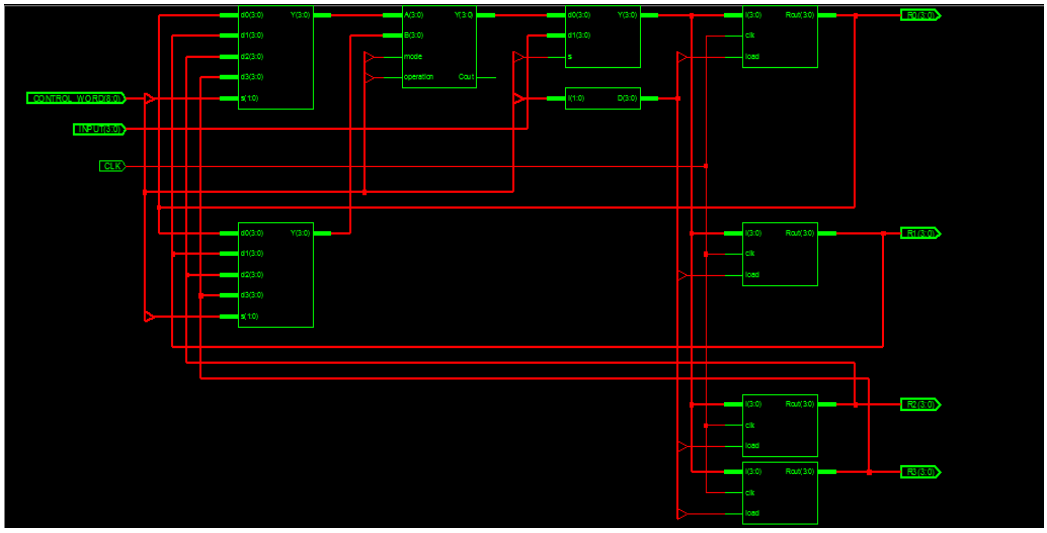

Figure 21. FPGA-Based Minimum Control Unit

4. RESULT

Timing Report: FPGA-based algorithms reduce the process time as well improve stability and flexibility. Figures 22 and 23 show the table of timing report in ripple carry adder and carry lookahead adder. These two adders are the main parts of ALU in two types of MCU.

```
--------------------------------------------------------------------------------
Delay:               10.531ns (Levels of Logic = 4)
  Source:            A<1> (PAD)
  Destination:       S<3> (PAD)

  Data Path: A<1> to S<3>
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O             2   0.821   1.216  A_1_IBUF (A_1_IBUF)
     LUT4:I0->O            2   0.551   0.877  Madd_RESULT_add0000_cy<1>11 (Madd_RESULT_add0000_cy<
     MUXF5:S->O            1   0.621   0.801  Madd_RESULT_add0000_xor<3>11_f5 (RESULT<3>)
     OBUF:I->O                 5.644          S_3_OBUF (S<3>)
    ----------------------------------------
    Total                     10.531ns (7.637ns logic, 2.894ns route)
                                       (72.5% logic, 27.5% route)
```

Figure 22. FPGA-Based Ripple Carry Adder

```
--------------------------------------------------------------------------------
Delay:               9.926ns (Levels of Logic = 6)
  Source:            B<0> (PAD)
  Destination:       Cout (PAD)

  Data Path: B<0> to Cout
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O             2   1.218   0.622  B_0_IBUF (B_0_IBUF)
     LUT3:I0->O            2   0.704   0.526  Inst_ADDI0/Cout1 (T1)
     LUT3:I1->O            2   0.704   0.526  Inst_ADDI1/Cout1 (T2)
     LUT3:I1->O            2   0.704   0.526  Inst_ADDI2/Cout1 (T3)
     LUT3:I1->O            1   0.704   0.420  Inst_ADDI3/Cout1 (Cout_OBUF)
     OBUF:I->O                 3.272          Cout_OBUF (Cout)
    ----------------------------------------
    Total                     9.926ns (7.306ns logic, 2.620ns route)
                                       (73.6% logic, 26.4% route)
```

Figure 23. FPGA-Based Carry Lookahead Adder

Regarding to Figures 22 and 23, the delay time in ripple carry adder is 10.531 ns and in carry lookahead adder is 9.926 ns.

Figures 24 and 25 show the Table of timing report in ripple carry subtractor and carry lookahead subtractor.

```
--------------------------------------------------------------------------------
Delay:               10.531ns (Levels of Logic = 4)
  Source:            A<1> (PAD)
  Destination:       Y<3> (PAD)

  Data Path: A<1> to Y<3>
                              Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O             2   0.821   1.216  A_1_IBUF (A_1_IBUF)
     LUT4:I0->O            2   0.551   0.877  Msub_Y_cy<1>11 (Msub_Y_cy<1>)
     MUXF5:S->O            1   0.621   0.801  Msub_Y_xor<3>11_f5 (Y_3_OBUF)
     OBUF:I->O                 5.644          Y_3_OBUF (Y<3>)
    ----------------------------------------
    Total                     10.531ns (7.637ns logic, 2.894ns route)
                                       (72.5% logic, 27.5% route)
```

Figure 24. FPGA-Based Ripple Carry Subtractor

```
--------------------------------------------------------------------------------
Delay:               9.077ns (Levels of Logic = 3)
  Source:            Cin (PAD)
  Destination:       Bout (PAD)

  Data Path: Cin to Bout
                              Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O             5   0.821   1.260  Cin_IBUF (Cin_IBUF)
     LUT3:I0->O            1   0.551   0.801  Inst_SUB3/Bout1 (Bout_OBUF)
     OBUF:I->O                 5.644          Bout_OBUF (Bout)
    ----------------------------------------
    Total                     9.077ns (7.016ns logic, 2.061ns route)
                                       (77.3% logic, 22.7% route)
```

Figure 25. FPGA-Based Carry Lookahead Subtractor

Figure 24 and 25 illustrate that, the delay time in ripple carry algorithm for sub-tractor is 10.531 ns but in carry lookahead algorithm is 9.077 ns.

Figures 26 and 27 show the table of timing report in ripple carry ALU and carry lookahead ALU.

```
--------------------------------------------------------------------------------
Delay:               12.208ns (Levels of Logic = 5)
  Source:            A<1> (PAD)
  Destination:       ALU<3> (PAD)

  Data Path: A<1> to ALU<3>
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O             3   0.821   1.246  A_1_IBUF (A_1_IBUF)
     LUT4:I0->O            2   0.551   1.216  Inst_AUblock/Inst_SUB/Msub_Y_cy<1>11
     LUT3:I0->O            1   0.551   0.827  ALU<3>_SW0 (N16)
     LUT4:I3->O            1   0.551   0.801  ALU<3> (ALU_3_OBUF)
     OBUF:I->O                 5.644          ALU_3_OBUF (ALU<3>)
    ----------------------------------------
    Total                     12.208ns (8.118ns logic, 4.090ns route)
                                       (66.5% logic, 33.5% route)
```

Figure 26. FPGA-Based Ripple Carry ALU

```
--------------------------------------------------------------------------------
Delay:               9.159ns (Levels of Logic = 3)
  Source:            Cin (PAD)
  Destination:       Bout (PAD)

  Data Path: Cin to Bout
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O             6   0.821   1.342  Cin_IBUF (Cin_IBUF)
     LUT3:I0->O            1   0.551   0.801  Inst_AU11/Inst_SUBB4/SUBTRACT3/Bout1 (Bout_OBUF)
     OBUF:I->O                 5.644          Bout_OBUF (Bout)
    ----------------------------------------
    Total                     9.159ns (7.016ns logic, 2.143ns route)
                                       (76.6% logic, 23.4% route)
```

Figure 27. FPGA-Based Carry Lookahead ALU

Based on timing report for ripple carry ALU and carry lookahead ALU, the ALU which design by carry lookahead algorithm is faster ($9.159\,ns$) than ripple carry algorithm ($12.208\,ns$).

Regarding to these comparison we are looking that, carry lookahead algorithm is faster than ripple carry algorithm and to design MCU we use carry lookahead algorithm. Figure 28 illustrates control words timing reports for MCU based on carry lookahead algorithm.

```
--------------------------------------------------------------------------------
Delay:               4.470ns (Levels of Logic = 4)
  Source:            CONTROL_WORD<8> (PAD)
  Destination:       Inst_loadreg3/Inst_regtype23:D (PAD)

  Data Path: CONTROL_WORD<8> to Inst_loadreg3/Inst_regtype23:D
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O             8   1.218   0.932  CONTROL_WORD_8_IBUF (CONTROL_WORD_8_IBUF)
     LUT4:I0->O            1   0.704   0.000  Inst_MUXX2/Y<3>1 (N86)
     MUXF5:I1->O           4   0.321   0.591  Inst_MUXX2/Y<3>_f5 (LOAD_BUS<3>)
     LUT4:I3->O            0   0.704   0.000  Inst_loadreg3/DI_3_or00001 (Inst_loadreg3/DI<3>)
    regtype2:D                 0.000          Inst_loadreg3/Inst_regtype23
    ----------------------------------------
    Total                     4.470ns (2.947ns logic, 1.523ns route)
                                       (65.9% logic, 34.1% route)
```

Figure 28. FPGA-Based Carry Lookahead Timing Report for Control Word of MCU

5. Conclusion

Higher execution speed versus small chip size is achieved by designing MCU with carry lookahead algorithm. Minimum Control Unit used in many application such as control and signal processing. This device has many suparts such as ALU, multiplexer, register and decoder. To have high-speed controller, carry lookahead algorithm is used to design ALU in proposed MCU. By compare between carry lookahead ALU and ripple carry ALU, proposed method can 25% timing improvement.

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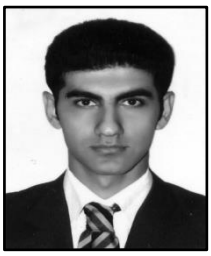

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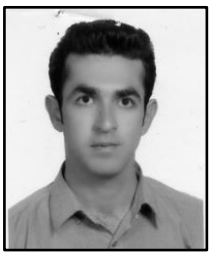

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