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Effect of Temperature & Supply Voltage Variation on the Stability of Existing 7T SRAM Cell

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Abstract

In this paper an existing seven transistor (7T) CMOS SRAM cell stability is measured. N-curve method is used to find the stability of the cell. The stability parameters i.e. Static Voltage Noise Margin (SVNM), Static Current Noise Margin (SINM), Write Trip Voltage (WTV) and Write Trip Current (WTI) are measured by varying temperature and supply voltage. The existing cell has an inbuilt mechanism for charge sharing. This technique .for the write operation. The existing 7T SRAM cell has achieved 22.71% increase in stability as compared to reference cell, which validate the desired design approach.

Keywords: *Stability, N-curve, static voltage noise margin, static current noise margin, write trip voltage, write trip current.*

1. Introduction

For many years CMOS devices have been scaled down in order to achieve higher speed [1]. According to Moore's Law, the number of transistors built on a single chip is doubled in every two years [2]. As process technology is scaled down, the leakage current variations is increased. The main components of power consumption for a transistor are switching power and leakage power [3]. Dynamic power consumption can be reduced by reducing the supply voltage. But reduction in supply voltage leads to a reduction in performance [4]. A small Vdd causes increased circuit delay and SRAM cell becomes less stable at low Vdd [5].

There are many applications in which power is supplied by battery, i.e. mobile, watches, war equipment etc. [6]. In these applications battery lifetime should be more. For long life power supply we require large battery, and it is awkward to place a large battery with small equipment's [1]. Hence power management is very important, reducing static power and dynamic power by improving the performance of the circuit [5].

This paper is organized as follows: Section 2 describes the existing architectures of conventional 6T and earlier 7T SRAM cell. Section 3 discusses the stability metrics using N-curve. Section 4 describes the existing 7T SRAM cell. Section 5 discusses the analyses and simulation work on existing 7T SRAM cell and to end with the conclusion in Section 6. Work is done in 90nm technology.

2. Present Architectures

There are many existing cell architectures; these cells provide high data stability, low power consumption and small memory cell.

2.1. Conventional SRAM cell [7]–[10]

Conventional 6T SRAM cell consists of two pass transistor and two inverters which are connected back to back. The SNM (Static Noise Margin) of conventional 6T SRAM cell is enhanced by Supply Voltage, Cell Ratio (CR) and Pull-Up Ratio (PR). If CR increases,

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then size of the driver transistor also increases, hence current increases. This improvement enhances speed of SRAM cell, as a result more read margin achieve. Similarly, PR enhances the current capability of SRAM cell, as a result more write margin achieved.

2.2. Other Existing 7T SRAM cell [9], [10]

7T Dual Vt SRAM cell simultaneously reduces active and standby mode power consumption and enhances the circuit speed and data stability. In this read operation is separated from the WL which provides stability to cell. Write power is reduced by using of single bit line. Two isolated signals WL and R lines are used to control write and read state. It reduces area overhead of the 7T SRAM as compared to existing 8T SRAM cell.

3. Stability Metrics using n-curve [11]–[17]

There are two methods to find the stability of the SRAM cell i.e. Butterfly curve and N-curve method. The drawback of butterfly curve method is the absence of inline tester [11]–[15]. N-curve provides the complete information of the voltage and current.

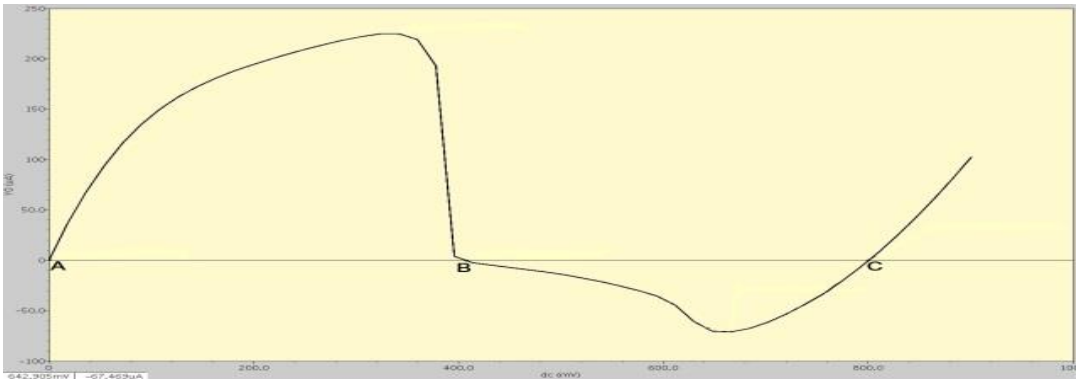

Figure 1. N-curve of 6T SRAM Cell (modified form [11]–[17])

The voltage difference between point A and B in figure 1 is SVNM (Static Voltage Noise Margin); it indicates the maximum tolerable DC noise voltage at the input of the inverter of the cell before its content changes. The peak current located between point A and B, can be used to characterize the cell read stability. The voltage difference point C and D is WTV (Write Trip Voltage). WTV is the voltage drop needed to flip the internal node "1" of the cell with both the bit lines clamped at Vdd. The negative current peak between point C and B or the write-trip current (WTI) is the amount of current needed to write the cell when both bit-lines are kept at Vdd [15]–[17].

For better read stability, the values of SVNM should be larger. For better write ability the value of WTV must be smaller [12]–[16].

4. Existing 7T SRAM Cell

The diagram of the existing 7T SRAM cell is shown in Figure 2. In the proposed circuit, the charge is transferred from the read to the write bitline. There is no need to use the pre-charge circuit for the write operation. The read and the write operations are controlled by Write Word Line (WWL) and Read Word Line (RWL) which is explained in ref [18].

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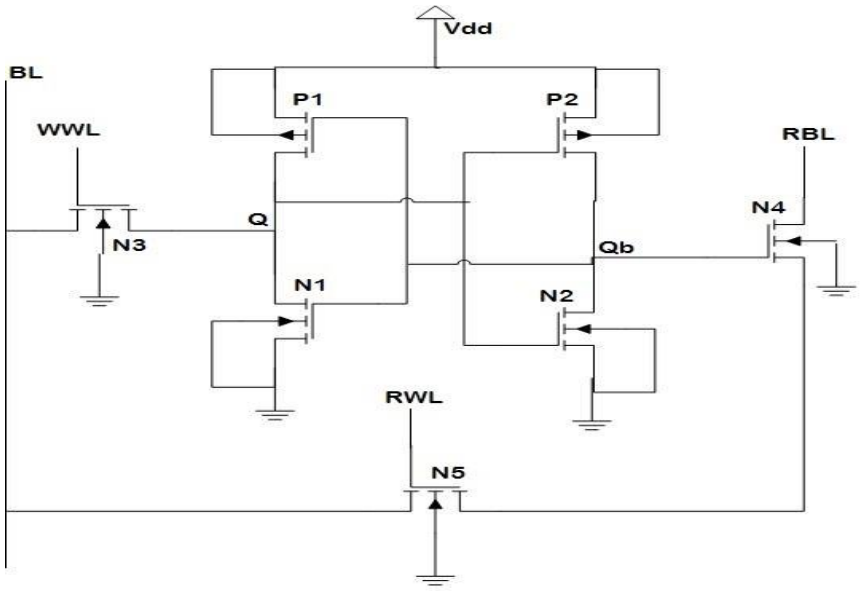

Figure 2. Existing 7T SRAM Cell

5. Analysis and Simulation Work

N-curve [14]–[17] analysis has been done at 90nm technology, various factors of stability has been analysed with different supply voltage (Vdd). N-curve parameter of existing 7T SRAM cell [18] at different Vdd cell is shown in Table 1.

Figure 3(a), (b), (c) and (d) shows the N-curve parameters of existing 7T SRAM cell. Existing7T cell shows improved results in terms of SVNM, SINM, WTV, WTI and N-curve parameters of this cell have high value as compared to reference cell [10, 18], which results high SNM.

Table 1. N-curve of Existing 7T SRAM Cell

Parameter	Existing Cell at 0.6 V	Existing Cell at 0.7V	Existing Cell at 0.8 V	Existing Cell at 0.9 V
SVNM (mV)	286.6	339.9	389.8	445.6
SINM (µA)	22.84	63.54	158.4	284.9
SPNM (µW)	2.69	11.43	28.92	63.47
WTV (mV)	312.5	359.8	409.8	454.5
WTI (µA)	–1.96	–6.59	–15.89	–30.09
WTP (µW)	0.31	1.11	3.25	6.84

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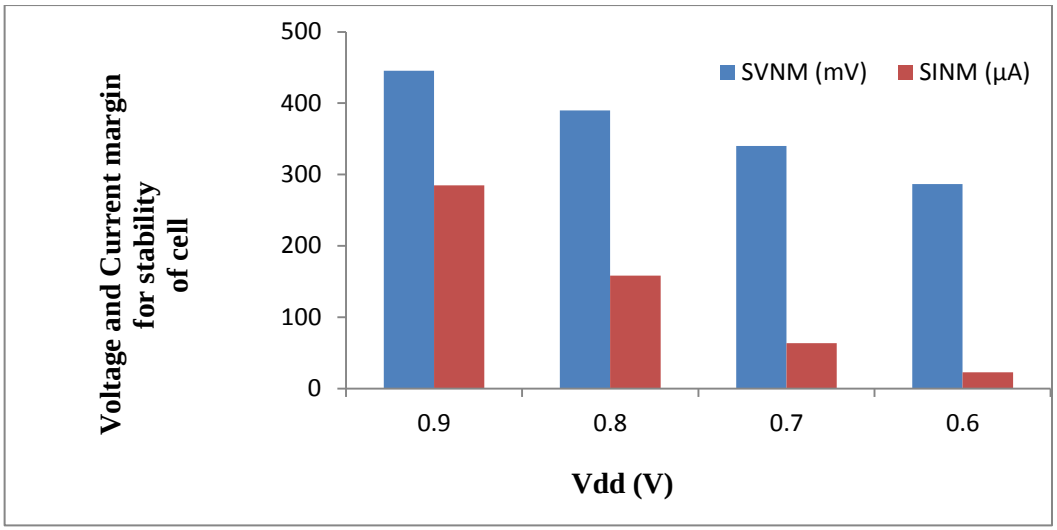
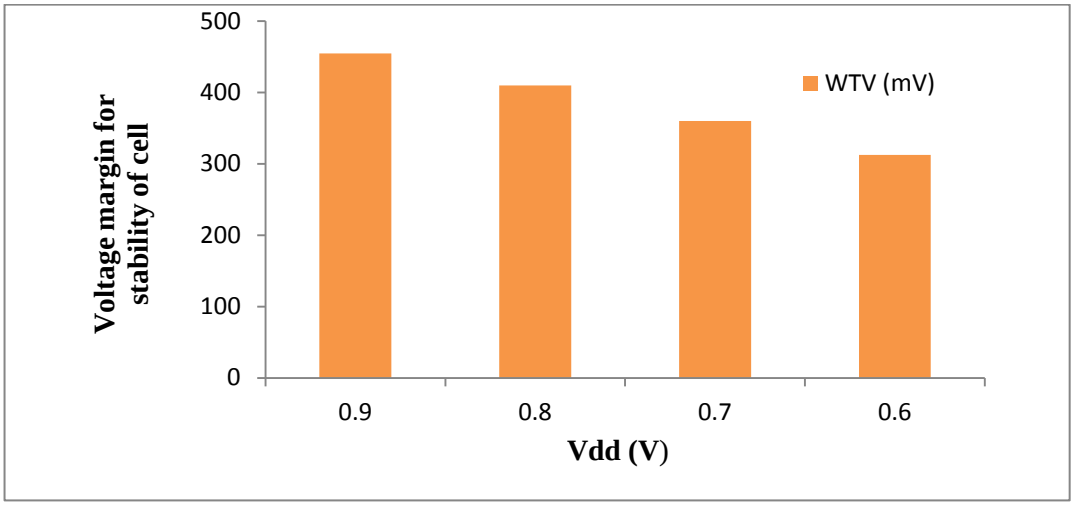
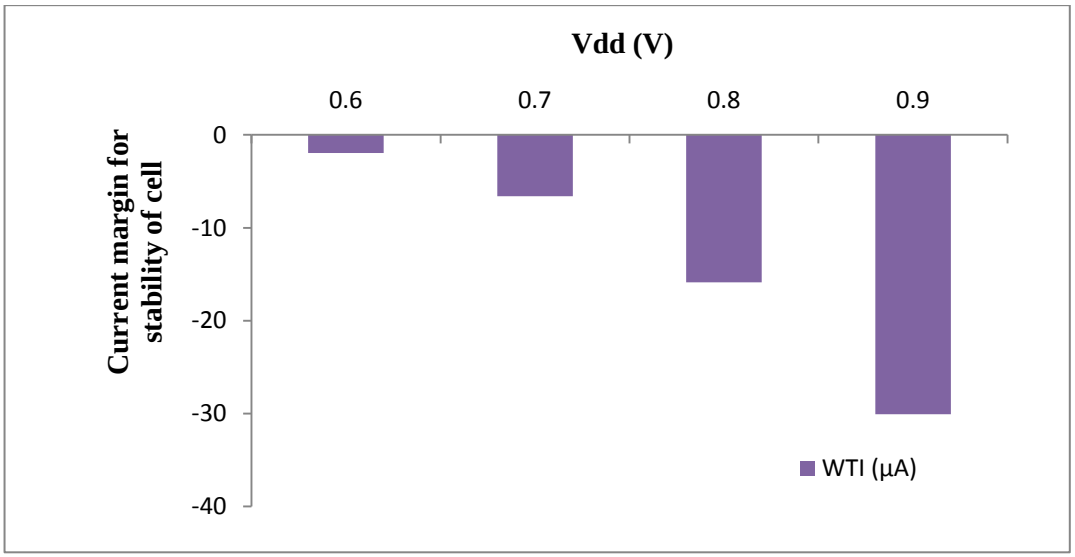


(a)



(b)



(c)

Figure 3. (a), (b) and (c) Show the N-curve Parameters of Existing 7T SRAM Cell

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Figure 4 shows the N-curve of existing 7T SRAM cell at different Vdd. As the Vdd increases the stability increases. This has also been observed that as the Vdd increases the four parameters *i.e.*, SVNM, SINM, WTV and WTI also increases. This shows the stability of the cell is limited by the Vdd scaling.

In this paper temperature has varied from –50°C to 200°C. We have seen that the SVNM and WTV is unaffected by the temperature variation but the currents *i.e.*, static noise margin current and the write trip current is affected by temperature variation. As temperature increases both the SINM and WTI decreases *i.e.*, shown in Figure 5 respectively.

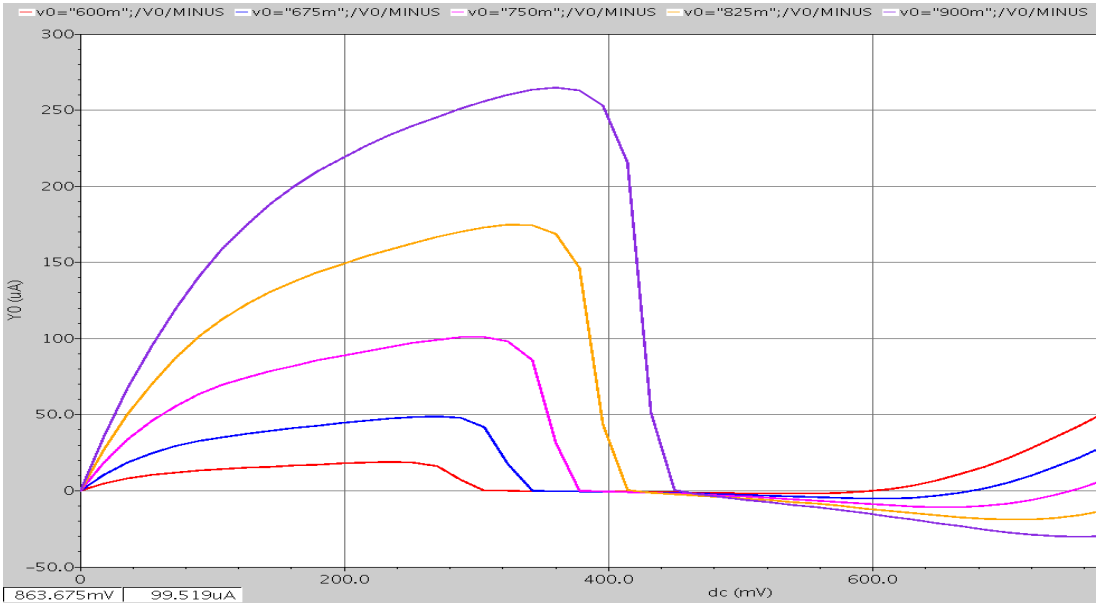

Figure 4. N-curve of Proposed 7T SRAM cell at different Vdd (0.6V, 0.68V, 0.75V, 0.83V & 0.9V)

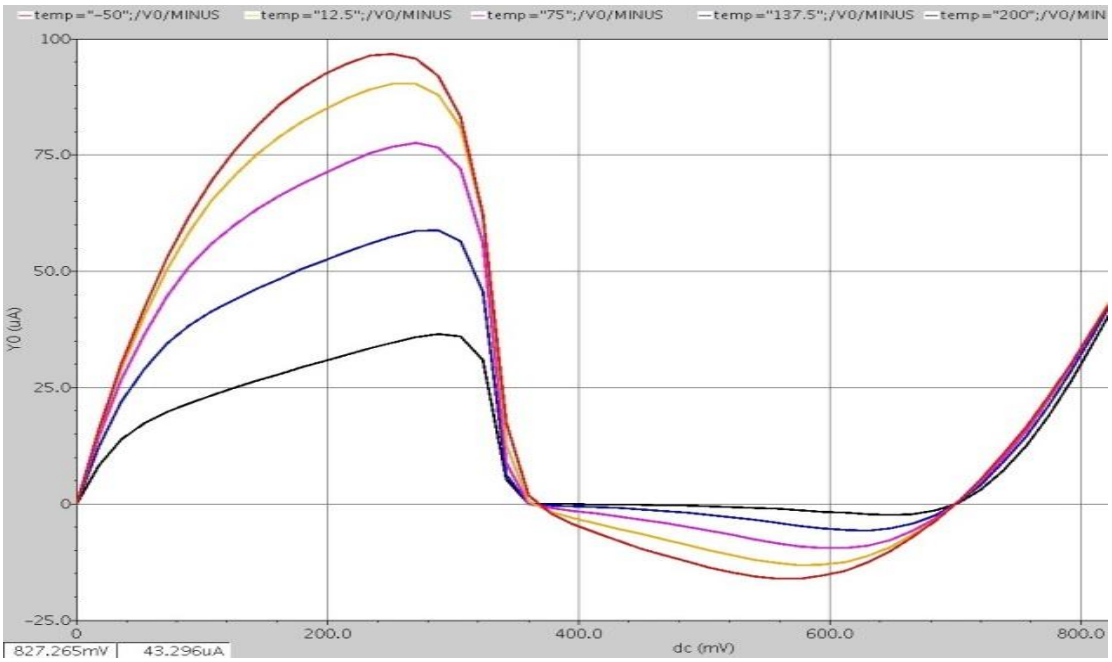

Figure 5. Effect of Temperature (–50°C to 200°C) on N-curve of Existing 7T SRAM Cell (at Vdd = 0.7V)

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6. Conclusion

A 7T SRAM cell has been presented with an inbuilt mechanism for charge sharing. For stability N-curve is used which gives the information about read stability and write stability. Simulated results show 22.71% increase in SVNM compared to reference cell. It is observed that as temperature increases the read & writes stability decreases and as Vdd decreases the read & writes stability decreases, hence SNM decreases. The compared results show the effect of temperature and supply voltage on stability of existing 7T design approach. With this existing 7T SRAM cell dynamic power and leakage power are also reduced.

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