International Journal of Hybrid Information Technology
Vol.8, No.8 (2015), pp.209-214
http://dx.doi.org/10.14257/ijhit.2015.8.8.21

Research on Simulation and Experiment of Chip Shape for Machining High Temperature Alloy

Fengyun Yu[*,1], YuanTu[2], He Wang[3] and Yunliang Fu[4]

Heilongjiang University of Science and Technology, Harbin, 150027, China
[1]1578415766@qq.com, [2]851607016@qq.com,
[3]346786233@qq.com, [4]772370969@qq.com

Abstract

For superalloy GH4169poor processing, tool wear serious, affecting the surface quality of the workpiece and other issues, using the finite element software AdvantEdge to simulate the formation process of superalloy GH4169 chip in two-dimensional, and researching the characterization of serrated chip. Take the single factor experiment and conduct finite element simulation for superalloy GH4169 in changing the rake angle and tip arc radius of the situation. The simulation and the chip shape taking from experiments will be compared to prove the feasibility of the simulation. And find out changes of rake angle and tiparc radius; make clear the influence of degree of serrated chip. The results show: with the rake angle increases, serrated degree increases, and with tiparc radius increases, serrated degree increases. The study provides a reference for reasonable choice of optimized cutting tool geometric parameters.

Keywords*: superalloy GH4169; chip shape; serrated degree; finite element analysis*

1. Introduction

Superalloy has high melting point, heat resistance, thermal fatigue resistance, stable organization performance, anti-oxidation, can withstand the high operating temperature and pressure, so the superalloy is widely used in high-temperature components in aerospace [1]. But at the same time the superalloy has high cutting temperatures, friction coefficient, the big unit area cutting stress and other characteristics, resulting in poor processability, the tips badly worn[2]. In the cutting process of the superalloy, serrated chip isa typical characteristic. The shape of the chip affects tool life, while reducing the quality of the machined surface. So there are important implications for the development of superalloy machining to research characteristics of serrated chip and geometric parameters of tool [3].

The author uses finite element software AdvantEdge to simulate characteristics of superalloy serrated chip and discusses the influence of tool geometric parameters for serrated chip. In the situation of changing rake angle and tip radius, to conduct the finite element simulation of superalloy. Find out changes of rake angle and tip radius which how to influence degree of serrated chip, and provide a reference for reasonable choice of optimized cutting tool geometric parameters.

2. Cutting Finite Element Model

2.1. Setting up Finite Element Model

The software of AdvantEdge can simulate the milling, turning, broaching and other processing methods, which is used to analysis the shape of superalloy chip. In this paper, take 2D turning, 2mm default value for height of working face and 5mm cutting length. Select superalloy as workpiece material from the material library and select Carbide-

ISSN: 1738-9968 IJHIT
Copyright ⓒ 2015 SERSC

General from Tool Material to set carbide tool materials. Establish 2D geometric model, as shown in Figure 1 [4].

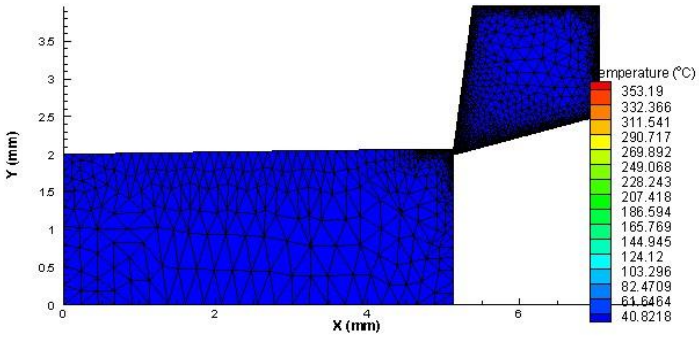


Figure 1. Two Dimensionalfinite Element Model of Cutting

2.2. The Finite Element Mesh Generation

AdvantEdge FEM software uses adaptive meshing generation technology. The non-cutting areas take coarse grids and cutting areas grids conduct layered encryption. This way improves the accuracy of the simulation results, shortens the simulation time and improves the simulation efficiency [5]. The change gradient of grid size decides the near from the tip contact with the workpiece to the degree of grid conversion away from the contact surface. It also affects the stability of the simulation.

(1)The division of tool grid. The maximum tool grid cell size is 1mm, the smallesttool grid cell size is0.02mm and the change gradient of grid size is 0.5 [6].

(2)The division of workpiece grids. The maximum non-cutting grid cell size is0.2mm, the smallest grid cell size is0.02mm and the change gradient of grid size is 0.5.

(3)The adaptive grid redraw coefficient. The cutting tool grid refinement coefficient is 1, the workpiece grid refinement coefficient is5 and the chip grid refinement coefficient is 1[7].

3. Comparison Simulation of cutting chip shape with Test Results of Cutting

3.1. Characterization of Serrated Chip

The geometric characterization and the physical characterization make up the characterization of serrated chip. The geometric characterization of serrated chip is the geometry features which include the serrated degree of chip, the width, pitch, frequency of serrated chip inside adiabatic shear band and so on [8]. The physical characterization includes the deformation, micro hardness, microstructure of serrated chip and so on.

3.1.1. The Geometric Characterization of Serrated Chip: Often use serrated degree G_S and pitch P to quantitatively expression serrated chip deformation, as shown in Figure 2. Pitch$P$ is the distance between two adjacent corresponding points, the size may also be related to the periodic fluctuation of cutting force [9].

$$G_S = (H - h_1)/H$$

where, G_s—Chip serrated degree;

H—The maximum thickness of the chip, μm;

h_1—The height of the chip continuous part, μm.

 Copyright ⓒ 2015 SERSC

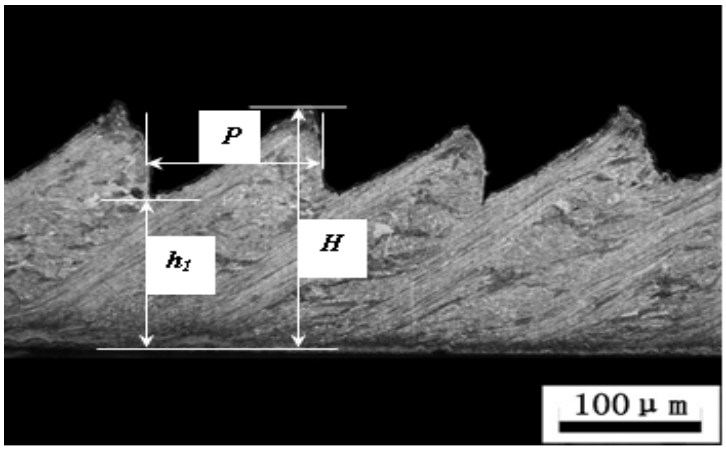
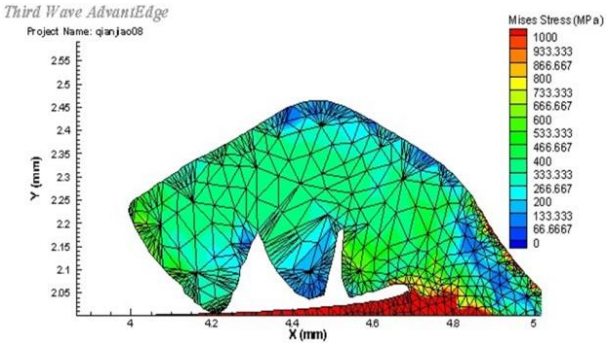
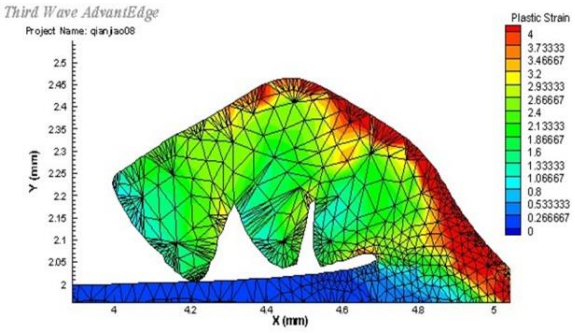


Figure 2. Geometric Characterization of Serrated Chip

3.1.2. The Physical Characterization of Serrated Chip: The physical characterization of serrated chip includes organizational structure between chips, physical properties, various parts of the chip strain, temperature distribution and so on. The physical characterization study of serrated chip includes serrated chip strain, micro hardness, microstructure and so on. As shown in Figure 3 is the physical characterization of serrated chip obtained by computer simulation software. Figure 3(a) is a chip equivalent stress distribution. Figure 3(b) is a chip equivalent strain distribution.



(a)Equivalent Stress Distribution



(b)Equivalent Strain Distribution

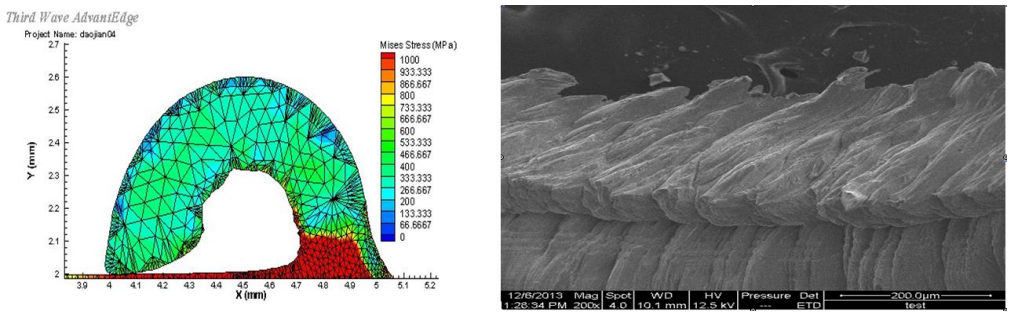
Figure 3. Physical Characterization of Serrated Chip

3.2. Turning Experiment

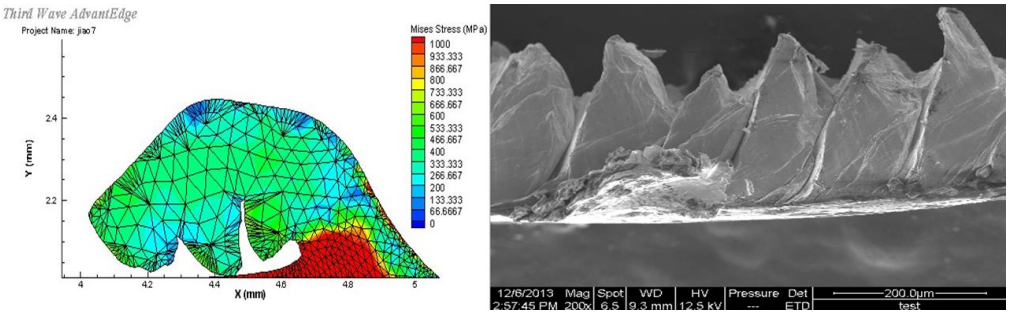
3.2.1 The Influence of Tool Rake Angle on Chip Morphology: The simulation and experiment conditions: the cutting speed v_c is 50m/min, cutting depth a_p is 0.4 mm. Feeds f is 0.15 mm/r. Tool relief angle α is 3°.The tip arc radius r_ε is 0.4 mm. Research tool rake

angle γ, when it is3°, 7°, 10° or 12°, the chip morphology change rule. Using AdvantEdge software to complete the establishment of simulation model, arithmetic, the post-treatment process, visualization and quantitative simulation results are obtained. Compare the chip morphology of simulation with experiment of chip morphology, as shown in Fig. 4. The left chip morphology is obtained by simulation and the right side is chip morphology by experiment after 200 times magnification SEM treatment.

The study found that compare the chip morphology obtained from simulation to the chip morphology obtained from experiment when the rake angle is 3°, the gross morphology obtained by experiment is the ribbon, cutting upper surface is furry. The morphology obtained by AdvantEdge software is the ribbon, cutting upper surface is furry but it is not very smooth. When the rake angle is 7°, compares the chip morphology obtained from simulation to the chip morphology obtained from experiment, the chip morphology obtained by experiment is serrated, serrated surface passivation is more serious, as the rake angle increases, the degree of serrated increases. The chip morphology obtained by simulation is serrated which is agree with experiment. When the rake angle is10°, compare the chip morphology obtained from simulation to the chip morphology obtained from experiment, the chip morphology obtained by experiment is serrated. Compared with the previous serrated degree of angle 7°, it significantly increased. The chip morphology obtained by simulation is serrated which is agree with experiment. When the rake angle is 12°, compares the chip morphology obtained from simulation to the chip morphology obtained from experiment, the chip morphology obtained by experiment is serrated. Compared with the previous serrated degree of angle 10°, it significantly increased. The chip morphology obtained by simulation is serrated which is agree with experiment.

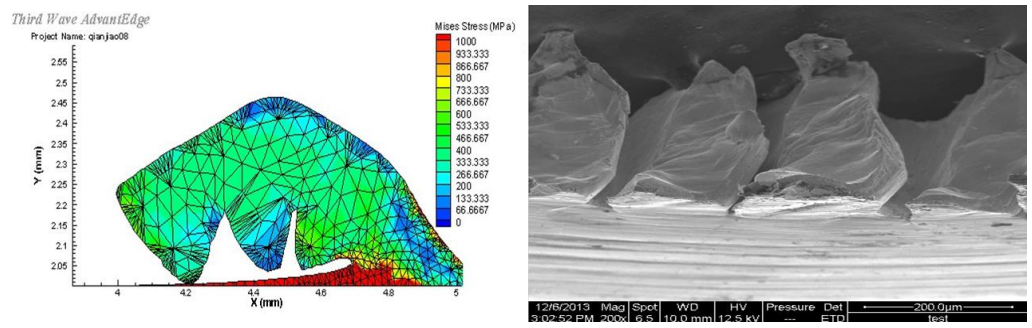


(a) Cutting tool rake Angle is 3 °

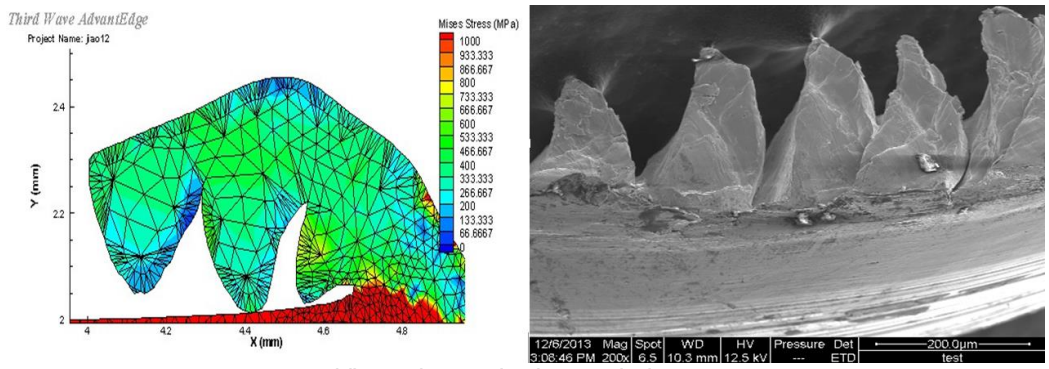


(b) Cutting tool rake Angle is 7 °

 Copyright ⓒ 2015 SERSC



(c) Cutting tool rake Angle is 10 °



(d) Cutting tool rake Angle is 12 °

Figure 4. Comparative Analysis of Simulation and Test Chips

3.2.2. The Influence of Tip Arc Radius for Chip Morphology: The simulation and experiment conditions: the cutting speed v_c is 50m/min. cutting depth a_p is 0.4 mm. Feeding f is 0.15mm/r. Cutting tool rake Angle γ is 10°. Tool relief angle α is 3°. Research tip arc radius r_ε, when it is 0.2mm, 0.4mm, 0.8mm or 1.2mm the chip morphology change rule. Using AdvantEdge software to complete the establishment of simulation model, arithmetic, the post-treatment process, visualization and quantitative simulation results are obtained. Compare the chip morphology of simulation to experiment of chip morphology as shown in Figure 5. Due to space Figure 5 only lists the tip arc radius of 0.4 mm。 When the tip arc radius is 0.8mm, the chip morphology obtained by experiment is serrated. The result is similar with the previous serrated degree angle 0.4mm. The chip morphology obtained by simulation is serrated which is agree with experiment in serrated degree and serrated frequency.

As shown in Figure 5, the left chip morphology obtained by simulation, the right chip morphology is by experiment after 200 times magnification SEM treatment. When the tip arc radius is 0.2mm, compares the chip morphology obtained from simulation to the chip morphology obtained from experiment, the chip morphology obtained by experiment is serrated, but the serrated degree is increased, the serrated frequency is low. The chip morphology obtained by simulation is serrated which is agree with experiment in serrated degree and serrated frequency. When tip arc radius is 0.4mm, the chip morphology is serrated by the experiment, comparing with the corner radius is 0.2mm, which serrated degree and the frequency of producing chip is reduced. The results from simulation are similar to it. When tip arc radius is 1.2mm, the chip morphology is serrated by the experiment, which serrated degree and serrated frequency of producing chip is reduced, while comparing with the tip arc radius is 0.4mm and 0.8mm, serrated degree is increased and serrated frequency is reduced. The chip morphology obtained by simulation is serrated which is agree with experiment in serrated degree and serrated frequency.

Copyright ⓒ 2015 SERSC

4. Conclusion

(1)In this paper, establish superalloy GH4169 cutting 2D model. Through computing the simulation model, get the serrated chip morphology. Compare and analysis the AdvantEdge simulation of chip morphology to validate the accuracy of the finite element simulation model.

(2)Through the comparison the results of simulation with experiment research, found that with the increase of cutting tool rake angle, the experiment of chip morphology from the ribbon gradually to serrated, and serrated degree increased gradually. When cutting tool rake angle is 3°, the simulation of chip morphology is strip, as the cutting tool rake angle continues to increase, the chip morphology transformation to serrated, and serrated degree increased gradually.

(3)Through the comparison the results of simulation with the experiment research, found that with the increase of tip arc radius, chip morphology serrated degree by experiment increases and the generated frequency of the serrated is reducing. The simulation of chip morphology chip serrated degree increases the generated frequency of the serrated is reducing and the generated frequency of the serrated is reducing.

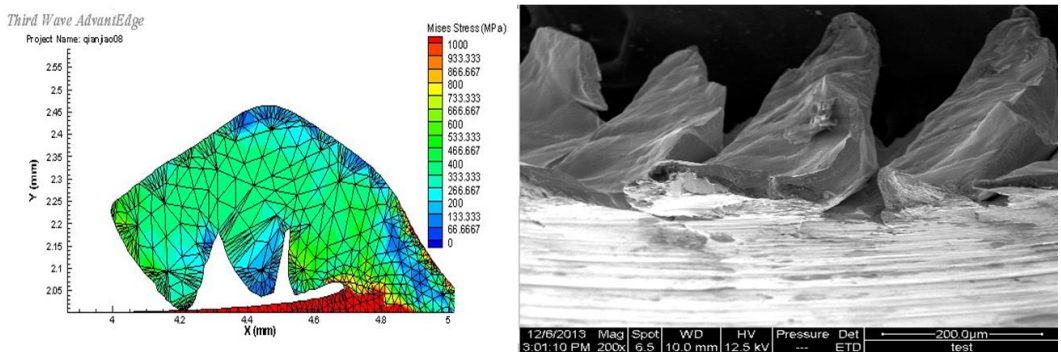


Figure 5. Comparative Analysis of Simulation and Test Chips

Acknowledgements

This work was supported by Heilongjiang Provincial Education Department Project "Thin-walled high-speed milling technology research and multi-objective optimization" (12541691).

References

[1] L. Weiwei, "Turning Technology of SuperalloyGH4169", Aeronautical Manufacturing Technology, vol. 14, no. 51, **(2012)**.
[2] H. Zhaobin, "Cutting GH4169 Related Mechanisms and Efficient Cutting Technology Based Research", Harbin Institute of Science, vol. 6, **(2013)**.
[3] Y. Chonghui, "Finite Element Simulation and Analysis of Superalloy GH4169 High-speed Machining", Qingdao Technological University, vol. 12, **(2011)**.
[4] L. Xinmiao, "Research Blade Shape and Emulsion Processing of GH4169 Machinability", Harbin Institute of Science, vol. 5, **(2011)**.
[5] D. G. Thakur, B. Ramamoorthy and L. Vijayaraghavan, "Study on the Machinability Characteristics of Superalloy Inconel 718 During High-speed Turing", Materials and design, vol. 5, no. 30, **(2009)**.
[6] Y. Gang, "Experimental study of Ni base superalloy cutting", Engineering Master Thesis, **(2010)**.
[7] G. Zhi Feng, "Experimental study on cutting nickel-based superalloy", Engineering Master Thesis, vol. 8, **(2012)**.
[8] L. Xinyuan, "Research nickel-based superalloy and efficient cutting quality control", Harbin Institute of Technology, vol. 7, no. 10, **(2010)**.
[9] G. Lize, "Experimental study of high speed milling cutting force of nickel-based alloy GH4169", Mechanical Engineer, vol. 3, no. 4, **(2011)**.

 Copyright ⓒ 2015 SERSC