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Research on SOC Test Bus Allocation Algorithm under the Constraint of Temperature

Xiaomin Li and Shuanghua Huang

Department of Electronic Engineering, Navy University of Engineering, Wuhan 430033, China
lxm_h@163.com

Abstract

The main concern is over rising temperature during the testing of complex system-on-chip (SOC), this paper studies SOC wrapper and test access mechanism (TAM), and proposes an improved algorithm of TAM assignment under the constraints of temperature. The algorithm uses temperature superposition method and adds compression process. This algorithm can find the test structure that uses shorter test time.

Keywords: *TAM, thermal constraint, temperature superposition method, compression process*

1. Introduction

Many challenges are proposed in chip design, test and validate along with the enhancing of SOC integration and complexity. First of all, because the IP core is generally buried deep inside the chip, it can not be accessed, tested directly. This requires a properly designed test structure for accessing the internal IP. Secondly, due to the power dissipation rises and temperature sharp rise during the test, the temperature is taking into account when test structures are designed. The design must be constrained by temperature.

SOC test architecture includes TAM and Wrapper. TAM is often specifically designed the test bus for test, it provides a test drive, test response, and test control signal transmission channel. Wrapper offers IP core interfaces with the outside world, TAM must pass through it to access the IP core [1].

General test case is designed conform to the IEEE 1500 standards. IEEE 1500 standard provides a series circuit as IP core test case basic structure. It has four main components: interface pins, including the serial input/output WSI-WSO, parallel input/output WPI-WPO, control interfaces such as WIP, control orders generally offered by WSI and WSO transmission ,test data can be transmitted over the WPI-WPO, can also be transmitted through the WSI-WSO serial; Shell instruction register WIR are used to control the test case work mode; WBY the bypass register are used to bypass other data registers, providing a fast data transmission channel; the testing boundary unit WBR are used to input stimulus and output response to achieve controllability and absorbability of IP core [2]. Test case design's main job was to divide the shell scan chains, which correspond to different TAM width, find the shortest test vectors transfer time.

In order to conduct parallel testing, test bus is usually to be grouped. The IP core in different groups can be tested at the same time. They can be grouped according to the fixed width, can also be grouped according to the variable width [3]. In the fixed-width testing bus structures, private bus is divided into more than one group, each group the bus width is same, and can be tested simultaneously, enabling parallel testing. When the same group of IP core for testing, other IP core test case to bypass them, without prejudice to the current IP-core test. This structure although can achieved parallel test, but due to different optimal test width of each IP core, so bus utilization is lower. Figure 1 shows in

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the test bus width variable structure, bus distribution is according to optimal of principles, each group bus is distributed to different IP core and different bus width, that grouping is more flexible, and test bus can be used more efficient [4].

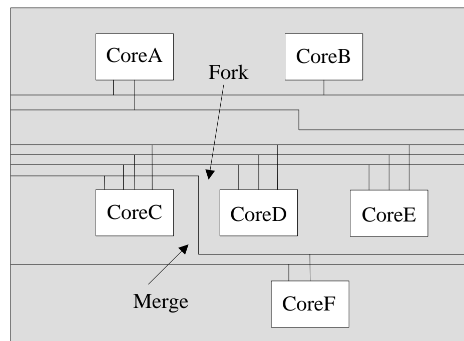

Figure 1. TAM Structure

2. Test Case and Test Access Mechanism for Joint Design Algorithm

Generally when the test case and test access mechanism for system-on-chip is designed according to the chip's design requirements, special test bus width is given, as well as IP core parameters, such as the number of inputs, outputs, and test vectors, and the internal scan chain number and length. Test structure design's goal is to complete each IP core wrapper design, identify the assigned TAM bus and determine the order of each IP core test, make the whole testing process of the shortest time, and restrict the test power and temperature in a specified range [5].

Designing algorithms can be divided into two main parts, the first part is the wrapper design algorithms, correspond to different TAM width designs test cases for each IP core in a different TAM bus width; the second part is the TAM bus assigned algorithm, according to the data obtained in the first part, bus are distributed and the IP core test orders is identified, the test design is completed. This paper mainly introduces the second part.

3. TAM Bus Allocation Algorithm

TAM bus allocation algorithm can effectively allocate bus to each IP cores, maximize bus utilization. The total time of the test is reduced by parallel testing. Thomas Edison proposed TAM bus distribution algorithm under temperature limit [6]: IP core test process can be represented by use of rectangle block, the width of rectangle block said test occupy of TAM width, and the length said test of time, each test process corresponds to a rectangle block. The problem of bus distribution can equivalent for II dimension boxing problem: given width of box for limited value, length for unlimited value. It requires all rectangular block to be assembled into the box, and temperature constraint must be satisfied during the packing process, so it takes up the Minimum length of the box. Figure 2 shows the algorithms assigned TAM bus example [7].

This paper improved Thomas Edison Yu packing algorithm. It replaced temperature transport model with temperature superposition model, and added the compression process in the allocation of test bus under temperature constraint. The algorithm is divided into four parts, beginning with defining TAM preferred widths [8]. The pseudo code is as follows:

Preferred TAM Widths PSEUDO-CODE
1 **for** each IPcore i
2 $T_p(i)=T_{min}(i) + (p/100)\cdot(T_{max}(i) - T_{min}(i))$;

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3 **find** w to make $t(i,w)$ closest $T_p(i)$;

4 $w_p(i) = w$;

// $w_p(i)$ is preferred widths of IP core

5 **If** $w_h(i) - w_p(i) < d$

6 $w_p(i)=w_h(i)$

// $w_h(i)$ is the widest Pareto-optimal

7 **End**

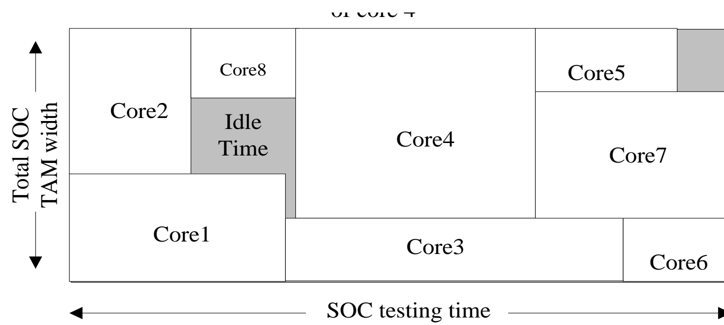

Figure 2. Boxing Problem

According to the wrapper design algorithms, we know that, when TAM width smaller, test time is a sharp drop along with the increase of TAM width, and when the width is increased, the decline was significantly reduced, as shown in Figure 3. In order to do not take up too much of bus resources and make the IP core cannot be tested in parallel, the algorithm do not use the widest Pareto - optimal point as the preferred width. It used constant P compromise choice test time TP (i), then found the closest width W between TP (i) and the test time, and set the width to its preferred width [9].

P value is usually between 1 to 10. When the difference between the IP core widest Pareto-optimal points and preferred width is less than d, set preferred width to widest Pareto-optimal point, which effectively reduces the overall testing time, especially when the IP-core test time is greater than the maximum test time for all IP core, the effect is particularly evident. The literature [10] gives a detailed description of example for the method of selecting the preferred width.

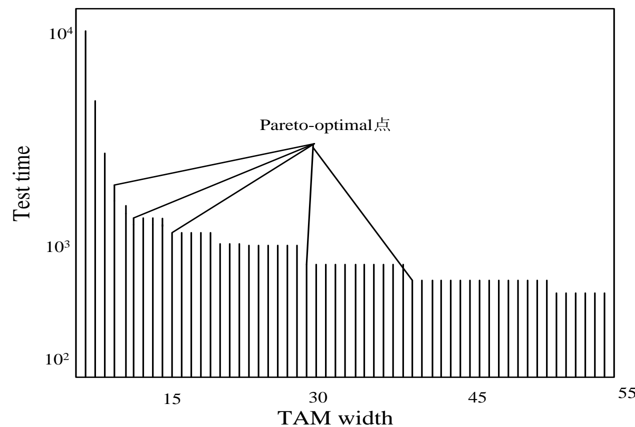

Figure 3. TAM Width and Test Time Relationship

The second part mainly is function block, TAM bus was assigned. The pseudo code is as follows:

TAM Width Assignment PSEUDO-CODE

```
1    while  each chip is assigned
2      current _ t = 0 ;
3      w _ avail = wmax ;
4      If w _ avail > 0
5        if  to find the IP core i satisfies: IP nuclear is not tested.
         AND w_p(i)<=w _ avail
         AND t(i, w_p(i)) max
         AND conflict() == 0
6        w(i) = w_p(i) ;
7            w_avail = w_avail - w(i) ;
8            set the IP core i start test;
9            begintime(i) = current_t ;
10           Return to line 4 ;
11       end
12       if  To find the IP core i satisfies: IP core did not start the test
         AND w_p(i) <= w _ avail + 3
         AND w_p(i) is minimum
         AND conflict() == 0
13         w(i) = w_pa(i) ;
14         w_avail(i) = w_avail(i) - w(i) ;
15       set the IP core i start test;
16         begintime(i) = current_t ;
17       Return to line 4 ;
18       end
19       If to find the IP core i : begintime(i) = current_t
         AND t(i,w(i)) - t(i,w(i) + w_avail) is maximum
         AND conflict() == 0 ;
20         w(i) = w_pb(i) ;
21         w_avail(i) = w_avail(i) - w(i) ;
22             Return to line 4 ;
23       end
24     else
25         current _ t = current _ t + t(e, w(e)) ;
26         w_avail(i) = w_avail(i) + w(e) ;
27         Return to line 4 ;
28     end
29   end
```

Secondly, The program is subject to while loops until the IP core are allocated, the loop body contains three kinds of distribution, and the first allocation methods is: In the present moment, the IP core that is not yet to be tested is found, its preferred width will be less than the current width available, and its testing time will be the longest time. The preferred width is distributed to that IP core. The second kind of allocation methods is: when the first allocation could not be found to meet the requirements of IP core, the second approach is performed. The IP core that its preferred width is less than or equal to

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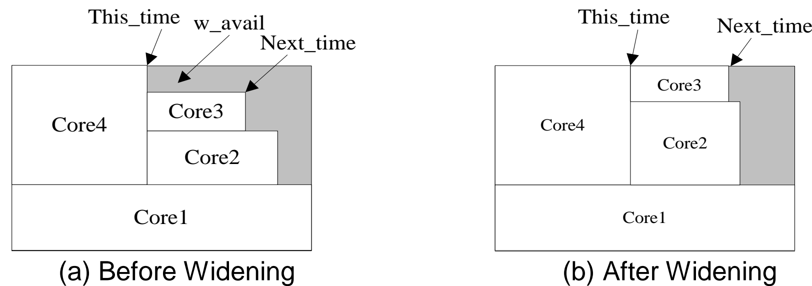
the current available TAM width plus three is found. And the widest Pareto-optimal points that meet the requirements are assigned to the IP cores. Constant three is the data of a large number of experiments result, can be modified appropriately according to actual condition, in order to achieve a better distribution effect. The third allocation is: when the IP core cannot be found to meet the requirements with above two methods and TAM width currently available was not all allocated, you can widen the assigned bus in order to reduce bus idle time, and find the IP cores that start a test at this moment, put the rest of the bus allocated to it, as shown in Figure 4.



(a) Before Widening (b) After Widening

Figure 4. Widen Process

It must be determined whether the temperature constraints are satisfied according to the actual situation in the allocation process. The conflict function is executed at each bus allocation. When conflict returns at 0, this means that distribution meet the requirements. If conflict returns at 1, this assignment should be given up.

According to the temperature superposition model, the conflict block that judges whether the allocation meets the temperature requirement is obtained. The pseudo code is as follows:

```
Conflict  PSEUDO-CODE
1    sum _ T = 45 ;
2    if execute Conflict the first time
3      Execute temperature simulation for each IP core, the power waste is P;
4      Set the temperature outside the chip at 45℃ ;
5    end
6    for i =1,2,...n
7          if    begintime(i)~=inf
8               According to the temperature superposition model, calculate the
     temperature T(i,w(i)) of the IP core i in the structure tam(i, w(i)) ;
9               sum_T = sum_T + T(i,w(i)) ;
10         end
11   end
12   if max(sum _ T) > max_ T ;
13     ret=1 ;
14   else
15     ret=0 ;
16   end
17   return ret ;
```

Temperature superposition model considers the temperature of several IP core to be tested at the same time equal to the temperature sum of each IP core to be tested separately [5]. When IP cores are verified in the parallel test, their temperature of parallel

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testing are equal to temperature sum of these IP core tested separately. Then it is determined whether the maximum temperature is outside the limits of temperature.

Due to the existence of constraints, the idle time of the bus is bound to produce during the test, such as the cooling process. Due to the existence of such free time, TAM bus utilization reduces and testing time increases. In order to reduce idle time during testing, this paper reduces idle time through the compression process, thereby shorten test time. In figure 2, by broadening bus width of core1, core8, and reducing the test bus width of core2, idle time behind Core2 can be compressed. This improvement process is known as compression process.

The compression process is executed before the update process of the main program. The update process is usually conducted after the completion of allocating the current bus or when all the IP cores to be distributed don't meet the restraints. If it is the second situation, the program will execute the compression process. The pseudo code is as follows:

```
Condense        PSEUDO-CODE
1   while  fail~=1
2     find   first ended IP core upz before the current moment；
3                  Widen upz；
4            find the IP core set tested at the same time with the upz and ended before it；
5     if     the assigned width of the upz is at maximum ( the Pareto- optimal point)
6                  break
7    end
8          wn(upz) =  the next Pareto- optimal point greater than w(upz) ；
9          wya=wn(upz) - w(upz) ；
10           update endtime(upz) ；
11           Adjust the bus of each IP core in "on", to make sure that the width of every
    moment doesn't exceed the maximum width；
12           Update the begintime ,endtime ,wa of each IP core in "on";
13  end
```

The compression process is to first find the IP core UPZ that its bus width needed to be widening, and determine UPZ bus width by Comprehensive available bandwidth and TAM width of IP core testing simultaneously with the UPZ. Then the IP core set based on that IP core that its bus width needs to be reduced is found. In chronological order, bus allocation is adjusted from UPZ start times, which makes each moment total width does not exceed the maximum limit. Last the start time and distribution of all IP core bus should be updated.

4. Simulation Results and Analysis

The d695 and p93791 circuit is the ITC 02 standard circuit. The test shell design and TAM assignment for d695 and p93791 circuit is used the algorithm proposed in this paper, and the test time required is compared with fixed width structure and Reference [3] shown in Table1. The unit of test time is a test cycle.

When the temperature is lower, the test time of the three methods is infinite. This indicates when the temperature constraint is too strict, no feasible solution. Comparison of testing time of three methods, Table 1 shows the result of the algorithm in this paper under temperature constraint is much better than the algorithm proposed in Reference [3], it can effectively reduce the test time.

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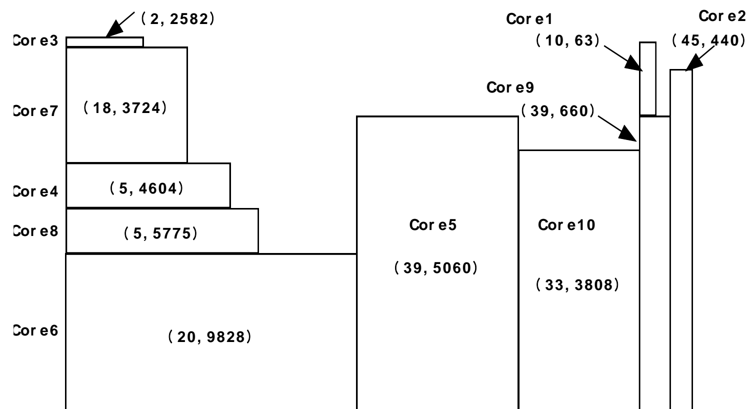
Table 1. Design Results

chip	Max width	Temperature limit℃	Test cycle in fixed width	Test cycle in Reference [3]	Test cycle in this paper
d695	16	93.3	Inf	Inf	Inf
		97.8	51506	48532	46987
		103.9		44135	44135
		Inf		44135	44135
	24	92.7	Inf	Inf	Inf
		99.6	43441	38467	35514
		105.3		38637	35514
		110.4		37022	34123
		114.2		35338	32385
		Inf		34314	32385
	32	92.5	Inf	Inf	Inf
		98.7	37475	29430	25535
		109.2		27151	23648
		115.4		25491	23164
		Inf		21106	21106
p93791	16	124.2	Inf	Inf	Inf
		135.3	1978027	Inf	1837789
		Inf		1837789	1837789
	32	105.2	Inf	Inf	Inf
		113.3	1207081	1145267	1009529
		125.6		1145267	997889
		136.7		1045213	991609
		Inf		967134	920656
	64	103.4	Inf	Inf	Inf
		112.5	750476	685412	642793
		127.7		641397	561810
		135.6		591347	543743
		Inf		529651	529651

We perform the following experiment to illustrate the effectiveness of the compression process to reduce the test time: Set the maximum width of 50, the highest temperature of 98.2 ℃, Design result of d695 in ITC 02 standard circuit is shown in Figure 5. The Figure (a) shoes the case by use of the compression process, and the Figure (b) is the case before compression process. The testing time is 19796 in Figure (a), and 22594 in Figure (b), reduces 2798 after compression process. The total testing time reduced by 12.4%.



(a) After Compression

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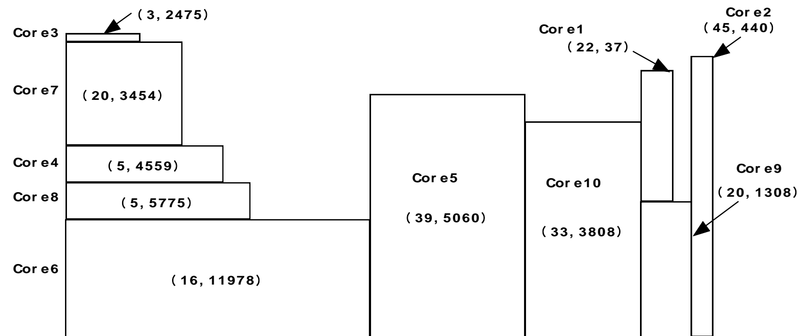

(b) Before Compression

Figure 5. The Effect of Compression

5. Conclusion

This paper had introduced the design of IP core wrapper and testing accessing mechanism TAM, and proposed a improve bus allocation algorithm. It reduced the temperature simulation time by use of power simulation and temperature superposition model. It is more accurate compared to transfer models. Because the compression was added to the algorithm, the time that the structure of algorithm design in the test is used is shorter.

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Author

Xiaomin Li, associate Professor, received the M. Eng. degree from the the school of Electronic Engineering, Naval University of Engineering, China in 2003. She has published more than 15 technical journal papers and international conference papers. Her research interests include (1) condition monitoring, fault diagnosis, and aviation equipment maintenance; (2) and virtual instrument.

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