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A Novel Hybrid Clamped Three-level Converter

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Abstract

A novel hybrid clamped dual-PWM three-level converter topology is proposed for induction motor drives in this paper. The switching states of hybrid clamp three-level converters increase to sixty-four from twenty-seven switching states of diode clamp three-level converters. In order to realize optimization of its redundant voltage space vectors by detecting voltage of clamp capacitor and difference of capacitor voltage in DC side, Generating an optimized switching pattern, The hybrid clamped three-level converter increases the voltage levels number, reducing the harmonics associated to the commutation frequency and limiting the dv/dt by all the switches . It can quickly balance the DC voltage, Realized system of 4-Quardant Running. the control circuit and main circuit was designed with DSP and CPLD, experimentation results proved it is very effective and practicability.

Keywords: *Dual-PWM, Three Level Converter, Hybrid Clamped, Voltage Space Vector*

1. Introduction

In recent years, multilevel converters has been widely studied for high power and medium voltage applications because of their advantages of low voltage stress for power semiconductors, low voltage harmonics and less electromagnetic interference. Many topologies and modulation strategies have been proposed and researched extensively for utility and drive applications[1-6], such as active power filters, static VAR compensators, and high voltage motor drives due to their ability to obtain waveforms with better harmonic spectrum and achieve higher voltages with a lower maximum device rating, The output waveforms of the multilevel converters are smoother than those of a two-level converters as the output voltage is synthesized from multiple levels of dc voltage. The topologies of multilevel converters can be classified into neutral-diode-clamp (NPC) converter, capacitor-clamped converter and series-connected H-bridge converter. NPC topologies have been proposed and successfully used in high-power motor drive and utility applications, The advantages of the NPC converters are the improvement of waveform devices, It is very difficult to keep the upper and lower DC-link capacitor voltages balanced to guarantee the multilevel operation of the converter[7-10]. Capacitor-clamped topologies were proposed for high-voltage motor and active power filters, The capacitor- clamped converter is an alternative structure used to obtain multi-level waveforms on the AC terminals, The flying capacitor multilevel converter does not require isolated DC sides and additional clamping diodes, Snubberless operation is possible and easy to expand to multilevel. However, It is serious problem to be quite limited by the voltage unbalancing of flying capacitors [11-16]. Series connection of H-bridge converter is an alternative method of achieving multilevel waveforms because of their modularity and simplicity of

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control, the H-bridge cascade converter has been used in several practical instance for broadcasting amplifier, plasma, industrial drive as well as STATCOM applications [17-19], The main limitation of the H-bridge cascade converter consists in the provision of an isolated power supply for each individual H-bridge cell when real power transfer is demanded. Hybrid multilevel converters with different switching frequencies were proposed in [18], however, the disadvantage of multi-level converters is that many power devices require to be used in the circuits. If the voltage level is more than five, the implementation of control strategy is complicated [21].

Pulse Width Modulation (PWM) for AC drives has been studied extensively during the past decades. Many different PWM methods have been developed to achieve the following aims: wide linear modulation range; less switching loss; less total harmonic distortion (THD) in the spectrum of switching waveforms; and easy implementation as well as less computation time. For a long period, carrier-based PWM methods were widely used in most applications [20]. The earliest modulation signals for carrier-based PWM are sinusoidal. The use of an injected zero-sequence signal for a three phase inverters initiated the research on nonsinusoidal carrier-based PWM. With the development of microprocessors, in recent years, Space Vector Modulation (SVM) has become one of the most important PWM methods for three phase converters. It uses the space vector concept to compute the duty cycle of the switches. It is simply the digital implementation of PWM modulators. An aptitude for easy digital implementation and wide linear modulation range for output line-to-line voltages are the notable features of space vector modulation. However, the implementation of conventional SVPWM is not an easy work even being based on DSP. With the help of lookup Table, computation of DSP could be simplified. But, lookup Table tends to give reduced pulse width resolution unless it is very large [23]. In recent years, many attempts have been made to unite the two types of PWM methods [31-32], because the comprehensive relation of the two types of PWM methods will provide a platform not only to transform from one to another, but also to develop different performance PWM modulation[24]. Another interesting research subject for SVPWM has been focusing on the simplification of SVPWM on line computation that has very important significance for real implementation in industry.

In this paper, we proposed a novel hybrid clamped dual-PWM three-level circuit topology for induction motor drives. The principle of the hybrid clamped circuit topology is discussed in detail, the switching states of hybrid clamp three-level converters increase to sixty-four from twenty-seven switching states of diode clamp three-level converters. Generating an optimized switching pattern of its redundant voltage space vectors by detecting voltage of clamp capacitor and difference of capacitor voltage in DC side, reducing the harmonics associated to the commutation frequency and limiting the dv/dt by all the switches. The control circuit and main circuit was designed with DSP and CPLD, experimentation results proved it is very effective and practicability.

2. Hybrid Model Reference Adaptive System

The Figure 1 shows a new multilevel converter topology in this paper, Note that there are the inner clamping capacitor which is not found in a conventional multilevel converter structure. It is DC-link voltage sources that supply power to the loads. The branch diodes are connected to the neutral point “o” of dc capacitors. switching states of each phase of the converter are listed in Table 1.

Table 1. Switching States Of Hybrid Clamped Topology and Output Level (As A Phase)

Output voltage	S_{a1}	S_{a2}	S_{a3}	S_{a4}
p	on	on	off	off
oA	off	on	off	on
oB	on	off	on	off
n	off	off	on	on

At each switching mode, there are four equivalent circuit of output state in this topologies,

The current paths are formed as following:

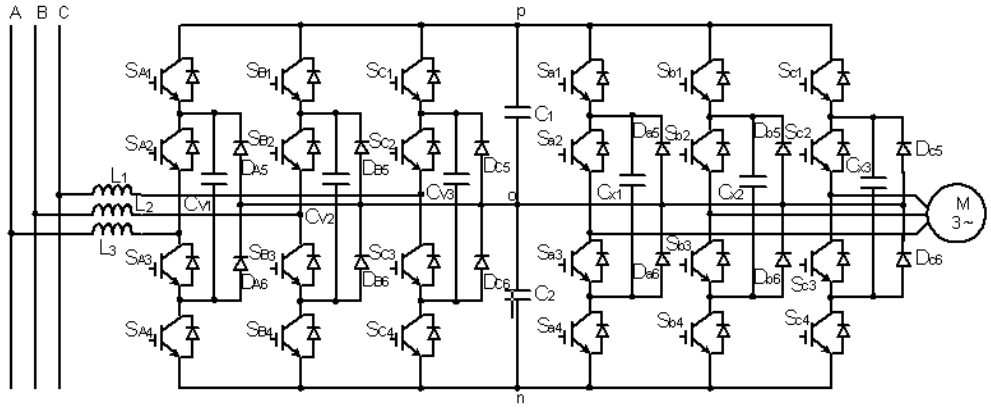

Figure 1. The Topology of Hybrid Clamp Three Level Three Phase Converter

1) p vector: the operating principle is shown in Figure 2, output voltage becomes $V_{dc}/2$ through S_{a1}-S_{a2} turned on and a bidirectional current path for ac load is achieved through freewheeling diode D_1- D_2, as shown by solid paths. That is process of p vector, If the voltage of capacitor C_{x1} is lower than $V_{dc}/2$, it will be charged to $V_{dc}/2$ by discharging capacitor C_{d1}, as shown by dotted path ①. On the contrary, if the voltage of C_{x1} is higher than $V_{dc}/2$, the voltage of C_{x1} will not be changed and discharged to $V_{dc}/2$ along with the load current in next switching period.

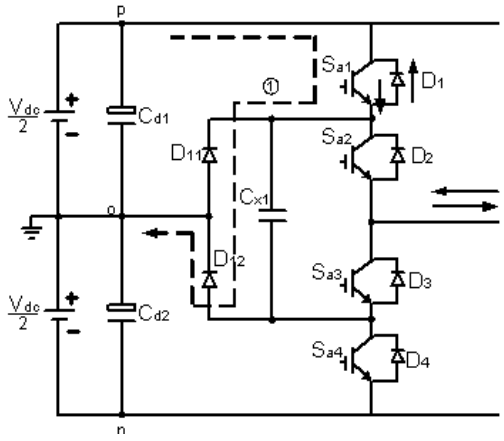

Figure 2. P Vector Current Circuit

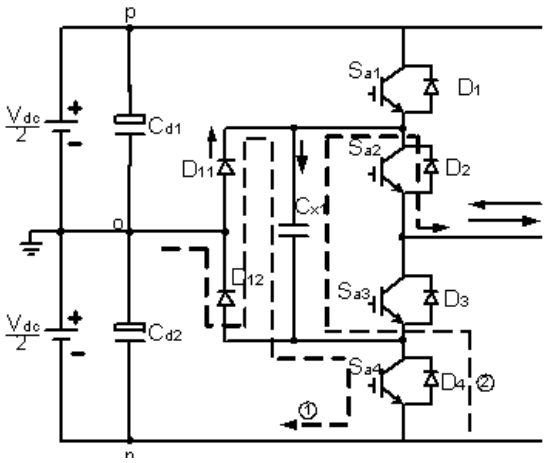

Figure 3. oA Vector Current Circuit

2) oA vector: current paths are shown in Figure 3, the switching $S_{a2}$and S_{a4} are turned on, $S_{a1}$and S_{a3} are turned off in the whole process. Output voltage zero is formed by the capacitor C_{d2} voltage that is discharged through branch diode D_{11} and S_{a2}, and a bidirectional current path for ac load is D_2、C_{x1} and S_{a4}, as shown by solid paths. That is process of oA vector, If the voltage of capacitor C_{x1} is lower than $V_{dc}/2$, it will be charged to $V_{dc}/2$ by current path of D_{11}-C_{x1}-S_{a4}, as shown by dotted path ①. On the contrary, if the voltage of C_{x1} is higher than $V_{dc}/2$, the voltage of C_{x1} will be discharged along with current path of D_4-C_{x1} -S_{a2}. as shown by dotted paths②. It will decrease waving amplitude of DC capacitor voltage when required output voltage is obtained.

3) oB vector: current paths of oB vector are shown in Figure 5, the switching $S_{a1}$and S_{a3} are turned on, $S_{a2}$and S_{a4} are turned off in the whole process. Output voltage zero is achieved through a current path C_{d2} -C_{d1}-S_{a1}-C_{x1}-D_3 , and a bidirectional current path for ac load is S_{a3}-D_{12}-C_{d2}, as shown by solid paths. If the voltage of capacitor C_{x1} is lower than $V_{dc}/2$, it will be charged to $V_{dc}/2$ by current path of S_{a1}-C_{x1}-D_{12}, as shown by dotted path ①. On the contrary, if the voltage of C_{x1} is higher than $V_{dc}/2$, the voltage of C_{x1} will not be changed and discharged to $V_{dc}/2$ along with the load current in next switching period.

4) n vector: current paths of n vector are shown in Figure 6, the switching $S_{a3}$and S_{a4} are turned on, $S_{a1}$and S_{a3} are turned off in the whole process. Output voltage is $-V_{dc}/2$ and D_3-D_4 forms bidirectional current path, as shown by solid paths, If the voltage of capacitor C_{x1} is lower than $V_{dc}/2$, it will be charged to $V_{dc}/2$ by current path of D_{11}-C_{x1}-S_{a4}, as shown by dotted path ①. On the contrary, if the voltage of C_{x1} is higher than $V_{dc}/2$, the voltage of C_{x1} will not be changed and discharged to $V_{dc}/2$ along with the load current in next switching period.

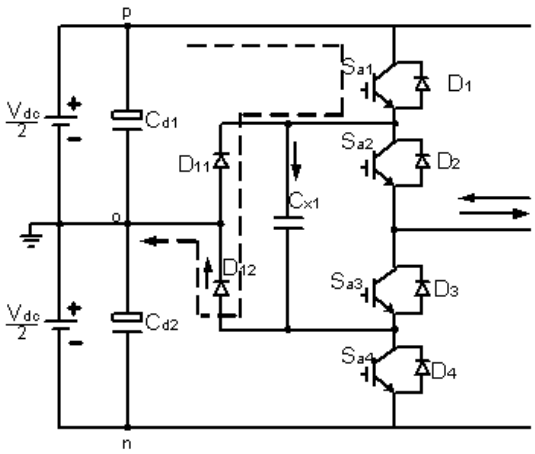

Figure 4. oB Vector Current Circuit

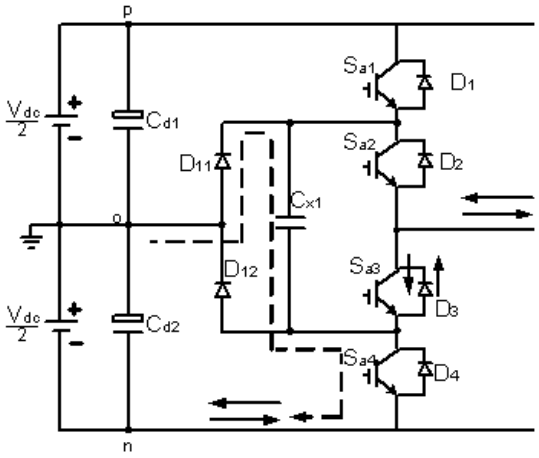

Figure 5. n Vector Current Circuit

From Figure 2-5, we can see that the voltage C_{x1}charged to the voltage $V_{dc}/2$ at the beginning can always be kept to $V_{dc}/2$ by charging or discharging action with C_{d1} and C_{d2}, Bidirectional current is achieved through C_{x1}, It is added a clamp capacitor in each bridge, this capacitor clamped the voltage when the switch is turned off. It can reduce unbalance of DC capacitor by proceed of capacitor charged and discharged. Clamp capacitor can realize bidirectional flow; The flexibility of vector synthesize is increased because of increased switching state, The switching states of hybrid clamp three-level converters is increased to sixty-four from twenty-seven switching states of diode clamp three-level converters, It can realize the more complicated and more accurate control, The operational principle of rectifier is similar.

3. Voltage Space Vector PWM Algorithm

3.1. Review of SVPWM in Undermodulation

Figure 6 explains SVPWM operation in the undermodulation and overmodulation regions, The operation in undermodulation or overmodulation is determined by the modulation factor, which is defined as:

$$m = \frac{V^*}{V_{1sw}} \quad (1)$$

where V^* is the magnitude of command or reference voltage vector and V_{1sw} is the fundamental peak value ($2V_d/\pi$) of the square (or six step) phase voltage wave [26].

In the undermodulation as shown in Figure 6(a), 0<m<0.907. In overmodulation Mode-1 as shown in Figure 6(b), 0.907<m<0.9514. In overmodulation Mode-2 as explained in Figure 6(c), 0.9514<m<1.0.

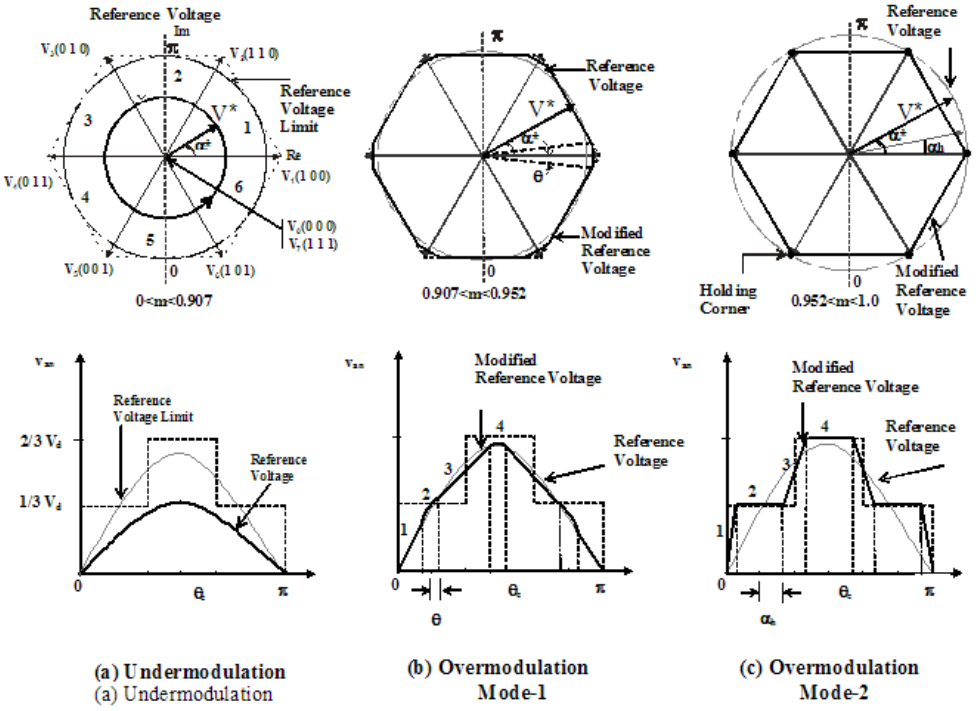

Figure 6. Voltage Trajectories in Undermodulation and Overmodulation Regions and the Corresponding Phase Voltage

3.2. Review of SVPWM in Undermodulation

Figure 7 shows the three reference sinusoidal command voltages in naturally sampled SPWM. It has been proved that when a kind of zero sequence component is added to the sinusoidal reference waveform as listed in Table 2, The naturally sampled SPWM will become naturally sampled SVPWM with exactly the same output voltage as that of the conventional SVPWM [22-24].

Table 2. Zero Sequence Components

ωt	$0 \sim \frac{\pi}{6}$	$\frac{\pi}{6} \sim \frac{\pi}{2}$	$\frac{\pi}{2} \sim \frac{5\pi}{6}$	$\frac{5\pi}{6} \sim \frac{7\pi}{6}$	$\frac{7\pi}{6} \sim \frac{3\pi}{2}$	$\frac{3\pi}{2} \sim \frac{11\pi}{6}$	$\frac{11\pi}{6} \sim 2\pi$
v_0	$v_a^*/2$	$v_b^*/2$	$v_c^*/2$	$v_a^*/2$	$v_b^*/2$	$v_c^*/2$	$v_a^*/2$

Figure 8 shows the corresponding three pole command voltages v_{ao}^*, v_{bo}^*, v_{co}^* in naturally sampled SVPWM.

When pole command voltage v_{xo}^* (x stands for a,b or c) reaches to $0.5V_d$ (limit of undermodulation), the peak value of line-to-neutral phase command voltage v_{xn}^* will be: $V^* = V_d/\sqrt{3}$, so, the maximum modulation factor that naturally sampled SVPWM in undermodulation can achieve will be:

$$m_{\max} = \frac{V_d / \sqrt{3}}{2V_d / \pi} = 0.907 \qquad (2)$$

If the magnitude of reference voltage v_{xo}^* increase further, peak value will exceed $0.5V_d$, then, inverter will be working in overmodulation region.

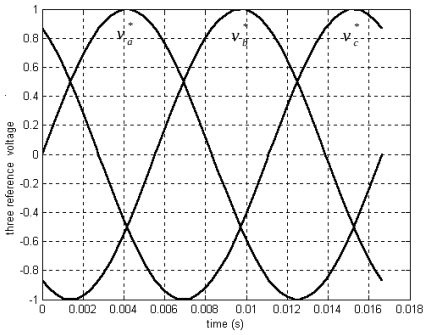

Figure 7. Waveform of Three Reference Voltages of Naturally Sampled SPWM

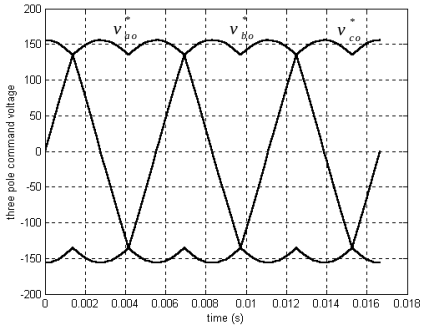

Figure 8. Waveform of Three Pole Command Voltages of Naturally Sampled

3.3. The Novel SVPWM Algorithm

Table 3 shows the summary of selected switching sequence of phase voltage for all the regions in the six sectors. Note that the sequence in opposite sectors is selected to be of a complimentary neutral-point voltage balancing. Voltage vectors switching states of each phase shows in Table 3. There are three switching states for the zero voltage vector V_0 and two switching states for the middle voltage vectors corresponding to the apexes of the smaller hexagon(V_1 ,V_4 ,V_7 ,V_{10} ,V_{13} ,V_{16})and one switching states for the large voltage vectors(V_2 , V_3 , V_5 , V_6 , V_8 , V_9 , V_{11} , V_{12} , V_{14} , V_{15} , V_{17} , V_{18}). The middle voltage vectors V_{1p} and V_{4p} is concerned with charging or discharging of upper DC capacitor C_{d1} in Figure 1, on the other hand, the voltage vector V_{1n} and V_{4n} are concerned with charging or discharging of the lower DC capacitor C_{d2}.

Figure 9 shows the voltage space vector representation of hybrid clamped three-level converter, Figure 10 shows the vector A triangle formed by the voltage vectors V_0、 V_2 and V_5, this triangle can be divided into four smaller triangles 1, 2, 3, 4. The apexes of these smaller triangles correspond to the voltage vectors in Table 1. In the space vector PWM technique, generally three voltage vectors corresponding to the apexes of the triangle which includes the reference voltage vector are selected in order to minimize the

harmonic components of the output line-to-line voltage. Duration of these three voltage vectors is obtained as follows.

Table 3. Three Level Vector Table of Hybrid Clamped Converter

Vector type	Voltage vector
Large vector	PPN, PNN, PNP, NNP, NPP, NPN
Middle vector	PAN, PBN, PNA, PNB, ANP, BNP, NAP, NBP, NPA, NPB, APN, BPN
Small vector	NAN, NBN, APB, BPB, APA, BPA, NAA, NAB, NBA, NBB, APP, BPP PPA, PPB, ABN, BBN, BAN, AAA, PAA, PAB, PBB, PBA, ANN,BNN PAP, PBP, BNA, BNB, ANA, ANB, NNA, NNB, AAP, ABP, BAP, BBP
Zero vector	PPP, NNN, AAA, AAB, ABA, ABB, BAA, BAB, BBA, BBB

Table 4. Voltage Vectors Switching States Of Hybrid Clamped (( )=Switching Mode, Y=A,B)

Voltage $\vec{V}^*$ Vector		A phase	B phase	C phase
V_0	V_{0n}	-E/2	-E/2	-E/2
	V_{0o}	0(2y)	0(2y)	0(2y)
	V_{0p}	E/2	E/2	E/2
V_1	V_{1n}	0(2A)	-E/2	-E/2
	V_{1p}	E/2	0(2B)	0(2B)
V_2		E/2	-E/2	-E/2
V_3		E/2	0(2A)	-E/2
V_4	V_{4n}	0(2A)	0(2A)	-E/2
	V_{4p}	E/2	E/2	0(2B)
V_5		E/2	E/2	-E/2

For example, if the reference voltage vector V* falls into the triangle A, the duration of the voltage vectors Vo, VI and V4 which correspond to the apexes of the triangle A can be calculated by the following equations.

$$V_1 \cdot t_a + V_3 \cdot t_b + V_4 \cdot t_c = V^* \cdot T \qquad t_a + t_b + t_c = T \qquad (1)$$

Table 5. Analytical Time Expressions of Voltage Vectors in Six Different Regions and Sectors

sector		t_a	t_b	t_c
A	1	$2kT\sin(\pi/3-\theta)$	$T[1-2k\sin(\theta+\pi/3)]$	$2kT\sin\theta$
	2	$2T[1-k\sin(\theta+\pi/3)]$	$2kT\sin\theta$	$T[2k\sin(\pi/3-\theta)-1]$
	3	$T[1-2k\sin\theta]$	$T[2k\sin(\theta+\pi/3)-1]$	$T[1+2k\sin(\theta-\pi/3)]$
	4	$T[2k\sin\theta-1]$	$2kT\sin(\pi/3-\theta)$	$2T[1-k\sin(\theta+\pi/3)]$
B	1	$2kT\sin(\theta-\pi/3)$	$T[1-2k\sin\theta]$	$2kT\sin(\theta+\pi/3)$
	2	$T[2k\sin(\theta+\pi/3)-1]$	$2kT\sin(\theta-\pi/3)$	$2T[1-k\sin\theta]$
	3	$T[1-2k\sin(\theta+\pi/3)]$	$T[2k\sin\theta-1]$	$T[1-2k\sin(\theta-\pi/3)]$
	4	$2T[1-k\sin\theta]$	$2kT\sin(\theta+\pi/3)$	$T[2k\sin(\theta-\pi/3)-1]$
C	1	$2kT\sin\theta$	$T[1-2k\sin(\theta-\pi/3)]$	$-2kT\sin(\theta+\pi/3)$
	2	$2T[1-k\sin(\theta-\pi/3)]$	$-2kT\sin(\theta+\pi/3)$	$T[2k\sin\theta-1]$
	3	$T[1+2k\sin(\theta+\pi/3)]$	$T[2k\sin(\theta-\pi/3)-1]$	$T[1-2k\sin\theta]$
	4	$-T[1+2k\sin(\theta+\frac{\pi}{3}]$	$2kT\sin\theta$	$2T[1-k\sin(\theta-\pi/3)]$
D	1	$-2kT\sin\theta$	$T[1+2k\sin(\theta+\pi/3)]$	$2kT\sin(\theta-\pi/3)$
	2	$T[2k\sin(\theta+\pi/3)-1]$	$-2kT\sin\theta$	$2T[1+k\sin(\theta+\pi/3)]$
	3	$T[1-2k\sin(\theta-\pi/3)]$	$-T[1+2k\sin(\theta+\frac{\pi}{3}]$	$T[1+2k\sin\theta]$
	4	$2T[1+k\sin(\theta+\pi/3)]$	$2kT\sin(\theta-\pi/3)$	$-T[1-2k\sin\theta]$
E	1	$-2kT\sin(\theta+\pi/3)$	$T[1+2k\sin\theta]$	$2kT\sin(\pi/3-\theta)$
	2	$2T[1+k\sin\theta]$	$2kT\sin(\pi/3-\theta)$	$-T[1+2k\sin(\theta+\frac{\pi}{3}]$
	3	$T[1+2k\sin(\theta-\pi/3)]$	$-T[1+2k\sin\theta]$	$T[1+2k\sin(\theta+\pi/3)]$
	4	$T[2k\sin(\theta-\pi/3)-1]$	$-2kT\sin(\theta+\pi/3)$	$2T[1+k\sin\theta]$
F	1	$2kT\sin(\theta+\pi/3)$	$T[1+2k\sin(\theta-\pi/3)]$	$-2kT\sin\theta$
	2	$-T[1+2k\sin\theta]$	$2kT\sin(\theta+\pi/3)$	$2T[1+k\sin(\theta-\pi/3)]$
	3	$T[1+2k\sin\theta]$	$T[2k\sin(\pi/3-\theta)-1]$	$T[1-2k\sin(\theta+\pi/3)]$
	4	$2T[1+k\sin(\theta-\pi/3)]$	$-2kT\sin\theta$	$-T[1+2k\sin(\theta+\frac{\pi}{3}]$

The calculation results are as follows：

$$t_a = T(1-2k\sin\theta) \quad t_b = T[2k\sin(\theta+\frac{\pi}{3})-1] \quad t_c = T[2k\sin(\theta-\frac{\pi}{3})+1] \quad (2)$$

Where $k = 2V/\sqrt{3}$, modulation amplitude $0 \le k \le 1$.

The duration of the voltage vectors corresponding to the apexes of the triangles B, C, and D can be calculated in the same way.

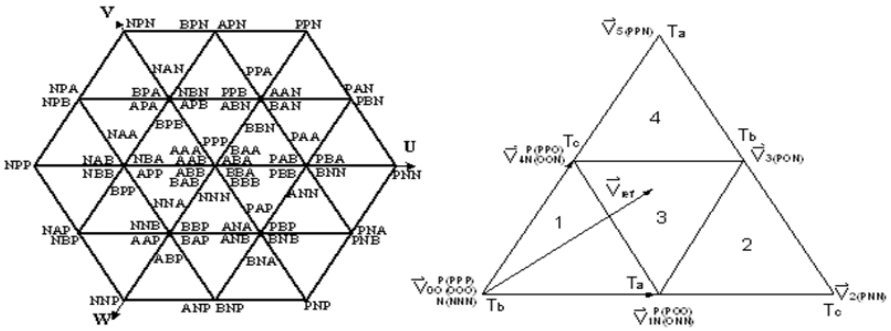

Figure 9. Space Voltage Vectors of Hybrid Clamp Topology
Figure10. Space Voltage Vectors of Hybrid Clamp Topology

Table 5 shows the analytical time expressions for t_a 、 t_b and t_c in the regions in the six sectors. These time segments are then distributed in a certain sequence in the sample period(T_s) so that the PWM wave is symmetrical and the neutral point voltage remains balanced.

Referring to Figure 7, and using the space vector PWM technique, generally, three voltage vectors corresponding to the apexes of the triangle that includes the reference voltage vector are selected to minimize the harmonic components of output line-to-line voltage. The duration of these three voltage vectors is obtained as Table 6. Figure 11 The turn on and turn off sequence and it's last time.

Table 6. Algorithm of Optimal Vector and Pulse Sequence

State	Condition	A phase	B phase	C phase	Pulse sequence
$V_{cd1} > V_{cd2}$	$V_{X1} < V_{cd1}\ V_{X2} < V_{cd1}$ $V_{X3} < V_{cd1}$	B vector	B vector	B vector	[B N N][B B N] [P B N][P B B][P P B]
	$V_{X1} < V_{cd1}\ V_{X2} < V_{cd1}$ $V_{X3} > V_{cd1}$	B vector	B vector	A vector	[B N N][B B N] [P B N][P B A][P P A]
	$V_{X1} < V_{cd1}\ V_{X2} > V_{cd1}$ $V_{X3} < V_{cd1}$	B vector	A vector	A vector	[B N N][B A N] [B A A][P A A][P P A]
	$V_{X1} < V_{cd1}\ V_{X2} > V_{cd1}$ $V_{X3} > V_{cd1}$	B vector	A vector	A vector	[B N N][B A N] [B A A][P A A][P P A]
	$V_{X1} > V_{cd1}\ V_{X2} < V_{cd1}$ $V_{X3} < V_{cd1}$	A vector	B vector	B vector	[A N N][A B N] [P B N][P B B][P P B]
	$V_{X1} > V_{cd1}\ V_{X2} < V_{cd1}$ $V_{X3} > V_{cd1}$	A vector	B vector	A vector	[A N N][A B N] [P B N][P B A][P P A]
	$V_{X1} > V_{cd1}\ V_{X2} > V_{cd1}$ $V_{X3} < V_{cd1}$	A vector	A vector	B vector	[A N N][A A N] [P A N][P A B][P P B]
	$V_{X1} > V_{cd1}\ V_{X2} > V_{cd1}$ $V_{X3} > V_{cd1}$	A vector	A vector	A vector	[A N N][A A N] [P A N][P A A][P P A]
$V_{cd1} < V_{cd2}$	—	A vector	A vector	A vector	[A N N][A A N] [P A N][P A A][P P A]

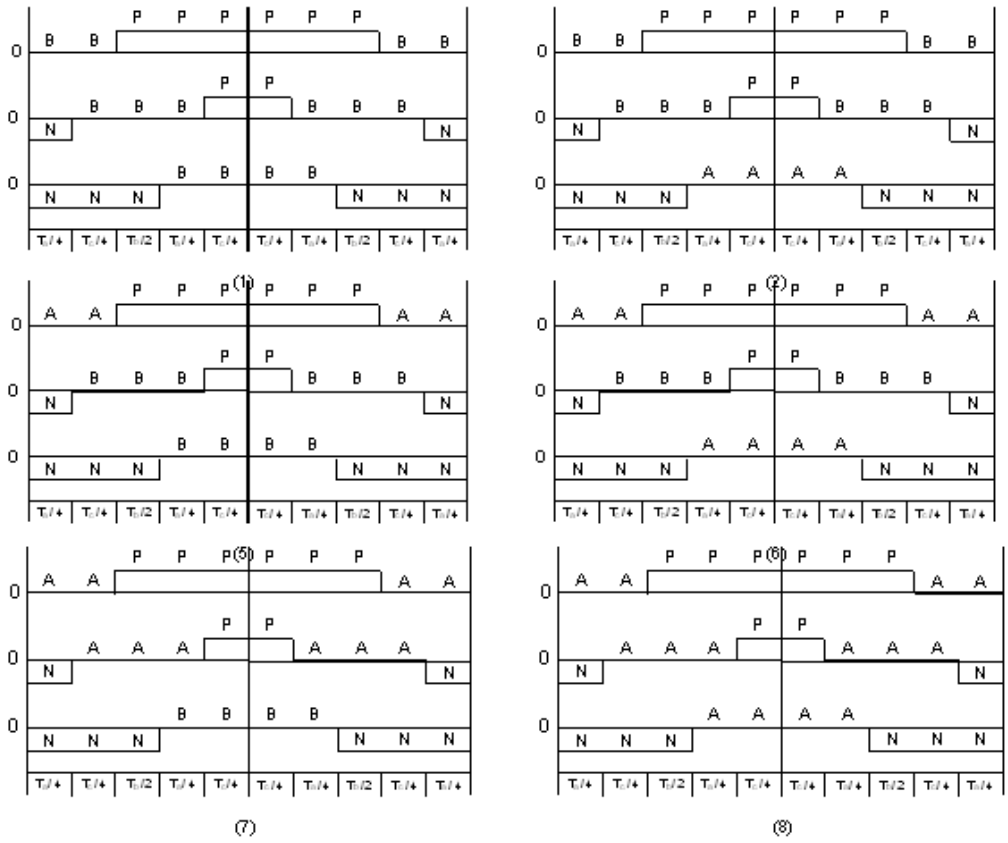

Figure 11. The Turn on and Turn off Sequence and It's La

4. Simulation and Experimental Results

Figure 12 is the simulation waveform of phase Voltage Ua and line voltage Uab in switch mode according to the space vector algorithm of the hybrid clamped three level converter. Figure13 is the simulation waveform of 3-phase output currents.

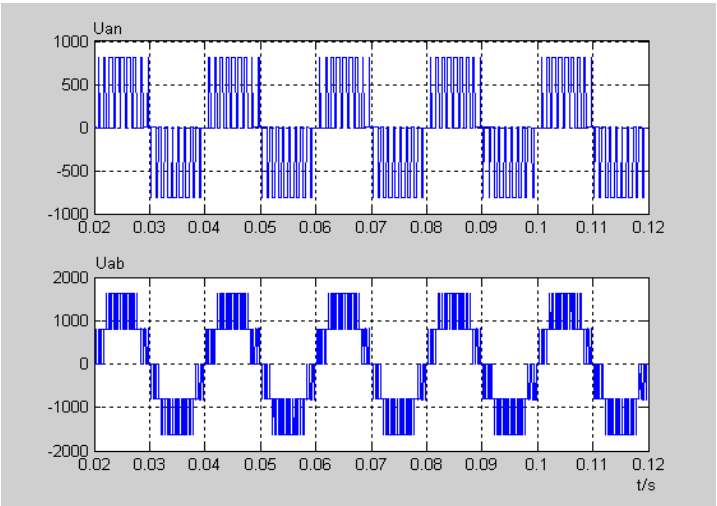

Figure 12. The Simulation Waveform of Phase Voltage Ua and Line Voltage Uab in Switch Mode

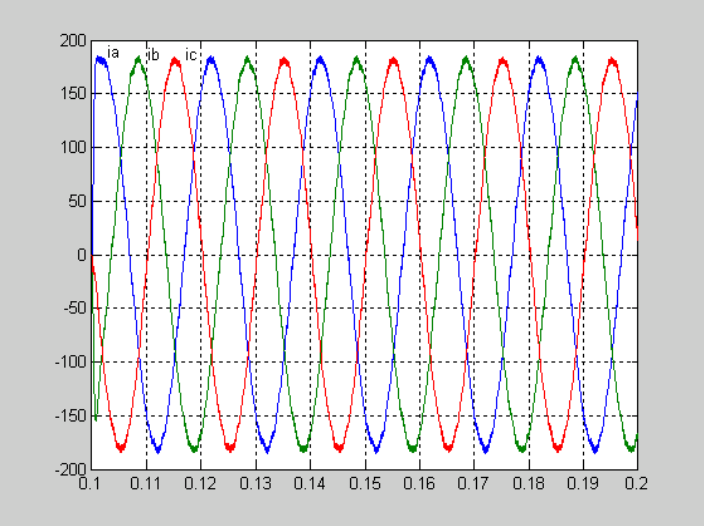

Figure 13. The Simulation Waveform of 3-Phase Output Currents

In order to validate the proposed hybrid clamped three level converter topology and space vector PWM algorithm, a dual PWM three-level converter was constructed in the laboratory. Figure 14 shows a block diagram of how the balancing algorithm was implemented. The modulation is programmed in 1# DSP+CPLD which generates desired switching states of rectifier, 2# DSP+CPLD achieved desired switching states of inverter, as described above, this information along with the desired switching state forms the address of the desired state in the redundant state selection Table 6.

The flying capacitor was set to $470\ uF\ /\ 450\ V$. A 2.2kW induction motor of 1460rad/min with the same parameter in steady-state study was used as a load. The dc voltage was supplied from an isolated rectified three-phase source. All the other operation conditions are the same as in the three-level steady state simulation study. As can be seen, the voltages and currents exhibit typical three-level inverter performance.

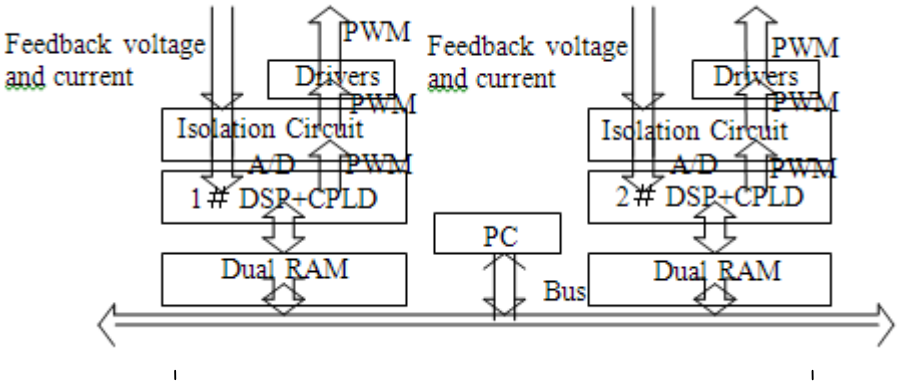

Figure 14. Control System of Dual Pwm Hybrid Clamp Topology

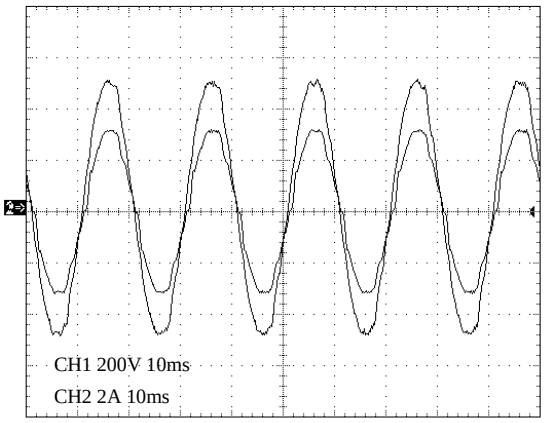

Figure 15. Single Input Voltage and Current Wave in Rectifier

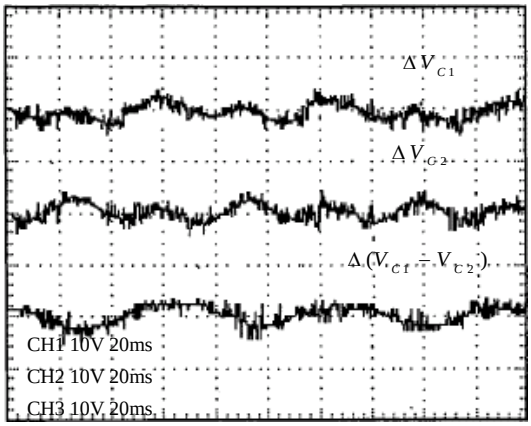

Figure 16. Voltage Error between Dual Dc Capacitor

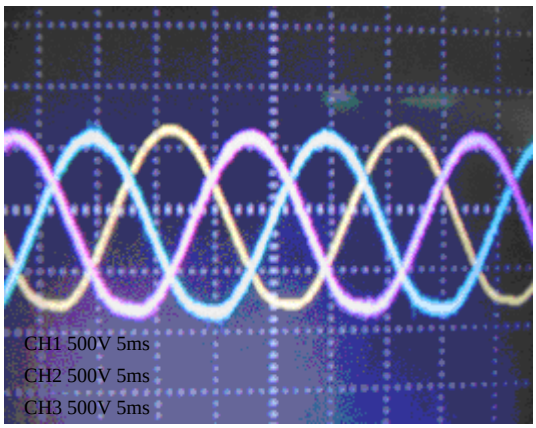

Figure 17. Three Phase Output Voltage in Inverter

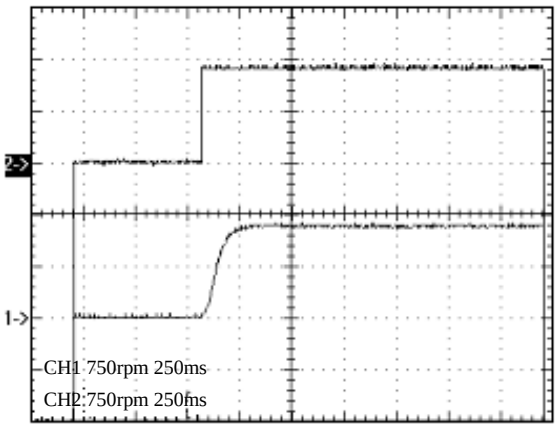

Figure 18. Ch1: Speed Response Sign Ch2: Speed Given Sign

The Figure 16 shows the wave of difference of capacitor voltage in DC side, It can achieve the balancing demand of DC side capacitor voltage because the neutral point voltage distortion becomes small, The Figure 17 shows output voltage wave of inverter which The low frequency harmonics seen in the current waveform. The Figure18 shows that motor have can be achieved rapid dynamic response with the speed given sign. It is verified that the algorithm mentioned in this paper is accurate by simulation and experimentation results.

Acknowledgements

This paper focuses its researches on dual-PWM three-level hybrid clamped converters and the novel space vector PWM Algorithm. Theory analysis, simulation and experimentation were made to investigate its character. A novel hybrid clamped dual-PWM three-level circuit topology was discussed, Analyzed the work principle of this converters and built up the mathematical model of the converter, The switching states of hybrid clamped three-level converters increase to sixty-four from twenty-seven switching states of diode clamp three-level converters. In order to realize optimization of its redundant voltage space vectors by detecting voltage of clamped capacitor and difference of capacitor voltage in DC side. This system was simulated by Matlab, In the last, the control circuit and main circuit was designed with DSP and CPLD, The simulation and experimentation results proved it was very effective and practicability.

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