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Clock Gated Multi Coding Technique for the Estimation of Transition Activities in Digital Circuits

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Abstract

In this paper, estimation of transition activity in multi coding technique with the help of hamming code estimator is done and power consumption is reduced using clock gating technique. The VLSI technology allows thousands of transistors in a single chip. In order to integrate more functions in a single chip and to improve their performance, the feature size of the transistors are continue to shrink. This results in maximum power dissipation of the circuit followed by heat removal and cooling of the circuit. The charging and discharging of the internal node capacitance due to transition activity highly contributes to dynamic power dissipation. Mainly the power dissipation occurs due to the transition activity and this can be estimated using hamming code estimator. Coded data is given to the hamming code estimator from each coding type. Estimated code is compared with the help of comparator, this result in analysis of the minimum transition activity for the code in appropriate coding technique. Also clock gating is used to minimize the unnecessary power consumed in the idle state.

Keywords: *Transition activity, hamming code estimator, clock gating, power dissipation*

I. Introduction

Encoding is the process of converting the data into a coded format by adding some codes which includes character, digits, and special symbols with the data. The reverse process of retrieving the original data from the coded data is decoding. This type of coding are employed for security purpose in the transmission process. These coding techniques are achieved by different ways and these are used in wide range of applications. The high dimensional data is converted to a reduced data by dimensional reduction is a coding technique. This can improve the computational efficiency, also the accuracy of the analysis and reduces the storage space [1]. The vertebra coding along with the convolution coding is effective in error checking. It is used in wireless communication in order to improve the limited channel capacity in communication [2]. The Viterbi decoder is used to decode the data, after the encoded data is passed through an additive white Gaussian noise (AWGN) channel and quantize. The original stream is obtained by either hard or soft vertebra decoder [3]. Turbo coding (encoders and decoders) is an error correcting technique used in communication system to achieve high throughput and reduced latency [4]. When compared to fault free encoder and decoder circuit which does not use the clock gating technique, the circuits with clock gating consumes only half of the power [5].

In digital circuits, the energy dissipation is the major constraint while the feature size is reduced. Among the power dissipation, dynamic power dissipation plays a vital role which is contributed by the switching activity on the interconnect lines. In coding schemes, an extra bit is added to the information to code it. This can be eliminated with a

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modified embedded transition coding scheme by inserting the inversion information in phase difference between the encoded data and the clock [6]. Several methods are used to encode the information which includes bus invert coding [7], swap coding, shift invert coding [8], circular shift coding, rotate coding [9] etc. By using the multi coding technique and estimating and comparing the hamming distance of coded data for different coding techniques are analyzed and hence the transition activity is minimized [10].

1.1. Clock Gating

Clock gating is the optimization technique to reduce power consumption. The RTL clock gating reduces the ASIC power consumption in synopsis power compiler. Generally the circuit consumes power even the values are not changing. Clock gating results in reducing the power consumption by inserting some logicwhenever the values at a particular node changes. The RTL clock gating allows easy configuration with minimum design and without any software involvement.

Also it preserves the timing of the design and performs the entire design without any change. Clock gating optimization adds some logic to the RTL design to deselect or disable the unnecessary sequential elements or registers. Adding this kind of logic to the design faces important challenges. To reduce the transition activity in the logical circuit by clock gating technique, it requires complete understanding of the RTL logic [11].In a sequential circuit, the design of clock behavior using gated clocks to generate the derived clock by the relationship between the triggering transition of the clock and clock cycles of flip flops. This reduces the power dissipation in the clock behavior [12].

Clock signals are high frequency signals, they are not carrying any information, they do not perform any computation and used for synchronization. But due to the high frequency, clocks are the major sources of power dissipation. Clock gating reduces the power dissipated by the clock signals. Clock gating is achieved by AND, NOR gates, Latch based AND gate, Latch based AND gate, Mux based clock gate [13].

1.2. Hamming Distance

Transition activity is the change in logic from logic 0 to logic 1 or from logic 1 to logic 0. While transmitting the information, the information is transmitted in the form of binary values as 0 and 1. In order to secure the information, it is coded with some extra bits. There must be a change in the bits before and after coding. The change in number of bits between two code vectors is the hamming distance. The hamming distance should be as small as possible to reduce the transition activity. The hamming distance is measured with the help of 1-bit full adder circuit.

1.3. Some Coding Techniques

Encoding and decoding makes changes in the bits of information. These coding can be done in several ways. Bus-invert coding uses a control bit along with the data called invert. The number of transitions (Hamming distance) between the present value and next data value is determined and based on the invert the data is inverted or not. If the Hamming distance is greater than n/2, then the data value is inverted. Otherwise the data value is transmitted as it is. In partial bus-invert coding, the entire bus is divided into two sub buses. The bus is partitioned based on the lower and higher transition activity or correlation. Then the partition which is having higher transition activity is bus-inverted. This reduces the hardware usage and also the transition activity.

In Universal rotated invert bus coding [14], the data value is encoded with using rotate right by one bit and rotate left by one bit. The Hamming distance between the data value and data on bus is calculated. The hamming code distance is compared with n/2, n is the width of the bus. If the hamming distance is greater than n/2 then the data value is encoded with invert code. The Hamming distance between the data rotated right by one

bit and data on bus is calculated. The hamming code distance is compared with n/2, n is the width of the bus. If the hamming distance is greater than n/2 then the data value rotated right by one bit is inverted. The Hamming distance between the data rotated left by one bit and data on bus is calculated. The hamming code distance is compared with n/2; n is the width of the bus. If the hamming distance is greater than n/2 then the data value rotated left by one bit is inverted.

2. Proposed Work

Consider a code vector of length n, n is the number of bits. Let 'a_n' be the data value transmitted on the bus or interconnects. Before applying the multi coding technique to the data value, the data is allowed to a AND gate named clock gating. Because of clock gating is employed, the power is consumed only for the transmitted data. Multi coding techniques includes invert data (INV data), swap data (SW data),invert the even position of data (INV even position of data), invert the odd position (INV odd position of data), rotate left and invert (RLWI), rotate right and invert (RRWI), circular left shift (CLS) and circular right shift (CRS). To select the coding type to code the data, control bits are assigned and shown in table 1. The 8 coding techniques are partitioned as four sets. In set1, it consists of two coding techniques inverting and swapping. In invert data (INV data), the bits are inverted by NOT gate and in swap data (SW data) the adjacent bits in the data are interchanged.

Table 1. Multi Coding Techniques and their Control Bits

S.No	Coding technique	Control bits
1	INV data	000
2	SW data	001
3	INV even position of data	010
4	INV odd position of data	011
5	RLWI	100
6	RRWI	101
7	CLS	110
8	CRS	111

Set2 consists of two coding techniques, inverting the even and odd position of data. In invert the even position of data (INV even position of data), the bits positioned at even place are inverted and in invert the odd position (INV odd position of data) the bits positioned at odd place are inverted. Set3 consists of two coding techniques, rotate left and invert (RLWI), the bit is shifted left by one bit then it is inverted and in rotate right and invert (RRWI), the bit is shifted right by one bit then it is inverted. Set4 consists of two coding techniques, rotate left and invert (RLWI), the bit is circulated left and in rotate right and invert (RRWI), the bit is circulated right.

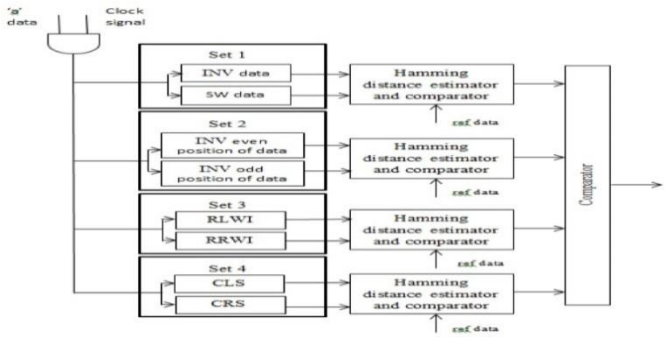

Figure 1. Block Diagram for the Clock Gated Multi Coding Technique

3. Methodology

Each data value is coded with multi coding technique and each coding is padded with control bits. The coding block is followed by the hamming distance estimator and comparator block. Each set contains two coding techniques and they are compared by single hamming distance estimator and comparator. Totally four comparator block are employed to compare the hamming distance of the entire multi coding technique. This type of comparison is used to identify the least hamming distance. After the hamming distance estimator calculates the hamming distance, the comparator identifies the coding technique which produces the least number of transitions for a particular data. Once the least number of transitions is identified for a particular bit, again that same coding technique is used for that bit. The block diagram for the clock gated multi coding technique is shown figure 1.

4. Simulation Results

The simulation results for the bits 'a_n'=11010111 and 'a_n'= with the three bit coded data are shown in figure 2 & 3. The Table 2, 3 & 4 shows the least hamming distance and its coding technique for the transmitted data a_n=11010111, a_n=01011011 and a_n=10100111on the bus.

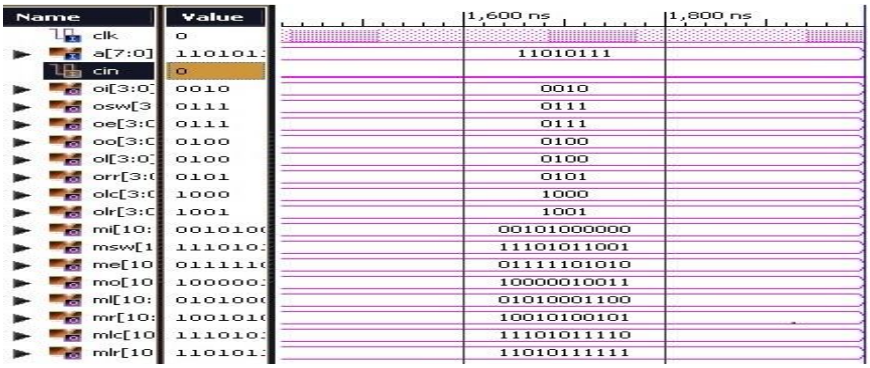

Figure 2. Simulation Output with Clock Gating for the Data 11010111

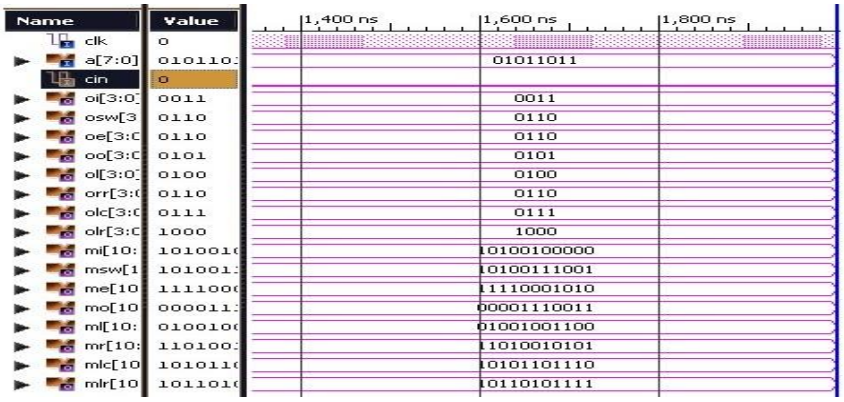

Figure 3. Simulation output with clock gating for the data 01011011

5. Conclusion

The hamming distance is estimated in the encoding and decoding process to reduce the power consumption with the help of clock gating technique. Most of the power dissipation occurs due to the transition activity on the logic level. The source of dynamic

power dissipation is charging and discharging activity of load capacitance because of the transition activity. So the hamming distance is estimated to determine the least transition activity among various coding techniques. By using the clock gating technique, the circuit consumes power only when the data is transmitted otherwise in the idle the power consumption is saved. Hence the clock gated multi coding technique along with hamming distance estimator reduced the power dissipation.

6. Future Work

In future by implementing the Dual Edge Triggered Flip Flop in the design instead of D Flip Flop Clock requirement can be reduce to 50% and operation speed also can be increased. This multi coding technique is used in all encoding and decoding process in the communication system.

References

[1] A. Anbarasi and K. Vivekanandan, "Encoding and DecodingTechniques for Distributed Data Storage Systems", Global Journal of Computer Science and Technology, vol. 11, Issue 13, **(2011)** August.
[2] V. S. L. Priya, V S and D. R. Rao, "Design and Implementation of Coding Techniques for Communication Systems Using Viterbi Algorithm", International Journal of Engineering Trends andTechnology (IJETT), vol. 4, Issue 10, **(2013)** October.
[3] H. L. Kumawat and S. Sharma, "An Implementation of a Forward Error Correction Technique using Convolution Encoding with Viterbi Decoding", International Journal of Soft Computing and Engineering (IJSCE), vol. 2, Issue 5, **(2012)** November.
[4] R. S. Singh, "Techniques for TurboDecoding Using Parallel Processing, Comparative Analysis", International Journal of Advanced Research in Computer Science and Software Engineering, vol. 3, Issue 4, **(2013)** April.
[5] N. Kapileswar and P. V. Santhi, "FAULT SECURE ENCODER AND DECODER WITH CLOCK GATING", International Journal of VLSI design & Communication Systems (VLSICS), vol. 3, no. 2, **(2012)** April.
[6] J. Jenifa, C. J. Ebbipeni, V. Monisha, "Bus Energy Minimization for a Serial Link by Modified Embedded Transition Inversion Coding", International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering, vol. 3, Issue 3, **(2014)** March.
[7] M. R. Stan and W. P. Burleson, "Bus-invert coding for low-power I/O", IEEE Trans VLSI, **(1995)**.
[8] J. Natesan and D. Radhakrishnan, "Shift inverts coding (SINV) for low power VLSI", Proceedings of the EUROMICRO Systems on Digital System Design, **(2004)**.
[9] M. S. B, Jahnavi and D. Y, "Universal rotate invert bus encoding for low power VLSI", International Journal of VLSI design &Communication Systems (VLSICS), **(2012)**.
[10] N. Vithyalakshmi and M. Rajaram, "A multi coding technique to reduce transition activity in VLSI circuits", Journal of Semiconductors, vol. 35, no. 2, **(2014)** February.
[11] F. Rivoallon and J. Balasubramanian, "Reducing Switching Power with Intelligent Clock Gating", White Paper: Virtex-6, Spartan-6, Kintex-7, and Virtex-7 FPGAs and Zynq-7000 AP SoCs, vol. 4, **(2013)** August 29.
[12] Q.Wu, M. Pedram and X. Wu, "Clock-Gating and Its Application to Low Power Design of Sequential Circuits", IEEE transactions on circuits and systems, fundamental theory and applications, vol. 47, no.103, **(2000)** March.
[13] J. Kathuria, M. Ayoubkhan and A. Noor, "A Review of Clock Gating Techniques", MIT International Journal of Electronics and Communication Engineering, vol. 1, no. 2, **(2011)** August.
[14] M. S. Bha, D. Y. Jahnavi, "Universal Rotate Invert Bus Encoding for Low Power VLSI", International Journal of VLSI design & Communication Systems (VLSICS), vol. 3, no. 4, **(2012)** August.

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