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Contribution to the Modeling and Simulation of Current Mode Pipeline ADC Based On Matlab

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Abstract

In this paper, a new version of non-ideal model 08-bit current mode pipeline ADC has been developed. It is based on Matlab and Simulink environment with special focus given to the analog building blocks. Those blocks are current Sample-and-Hold(S/H), current Sub-ADC and current Sub-DAC. In this model, the sub-ADC is implemented by two current comparators and encoder logic circuit. For the current S/H and sub-DAC, they are implemented by using a switch current and current source. The main advantage of current mode approach is its low power dissipation, low cost and high speed. However, there are some technical limitations; using the model and running the simulation with the introduction of the main non idealities components such as a current offset, clock feed through, charge injection, clock jitter, switching noise, mismatch errors and non idealities in current amplifier, demonstrated clear degradation of the performance of the ADC.

Keywords: *Analog to Digital Converter, Modeling, current mode, Current sample and hold, pipeline, Sub-ADC, Sub-DAC, switch*

1. Introduction

Due to the huge increase of the architecture and the complexity of mixed signal circuits, the use of behavioral model is necessary to design and simulate the performance of those circuits [1-4]. The complexities of mixed signal circuits require using faster and more complex mixed-signal testers. The behavioral models which use Matlab and Simulink environment are becoming good methods to design and simulate the performance of the complex circuits such as the data converter, Analog to Digital conversion (ADC). They provide a link between these two domains is an extremely important research area [5]. ADCs are categorized and classified by their performance characteristics. This includes resolution, bandwidth, sampling rate, power consumption, and the effective number of bits [6]. Compared with the other types of ADCs, the pipeline ADC structure is very attractive combination of speed, resolution, low power consumption and small die size. Furthermore, selection of the topology of the ADC needs to be chosen between the speed, resolution, smaller silicon area and power consumption. However, this will require a reduction in supply voltage causing an increase of parasitic components present. From where there is a growing need for new low voltage analogue circuit techniques.

Current mode approach [7] has many advantages in comparison with voltage-mode. One of the advantages is the current mode circuits do not need high precision passive components. So they can be designed almost entirely with transistors only. MOS transistors in particular are more suitable for processing currents rather than voltages. This makes the current-mode circuits compatible with typical digital processes and MOS transistors show also high performance in terms of speed, bandwidth and accuracy [8].

The current-mode (CM) ADC is advantageous because it can be implemented by standard CMOS technology only and it is also demonstrating excellent characteristics such as in particular, high resource efficiency (power and area) [9]. Furthermore, many signal

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processing systems are current-based, like biometrics and image sensors [10]. The CM ADC should be designed to accept current as the input signal.

In this paper, a new version of non-ideal model of 8 bit CM pipeline ADC has been developed. This was accomplished by using MATLAB and SIMULINK environment with a focus on detailing the major building blocks of CM pipeline ADC. Those building blocks are current Sample-and-Hold (S/H), current Sub-ADC and current Sub-DAC. The sub-ADC is implemented in our model by two current comparators and encoder logic circuit. The current S/H and sub-DAC are implemented by using a switched current [11] and current sources. By analyzing the simulation results of the model where the most important non idealities components are taken into account (such as clock feed through, charge injection, switching noise and mismatch errors), it has been clear how the parameters of the converter are affected by the non-idealities factors of the circuit.

The paper is organized as following: in the second section and after the introduction, the proposed system architecture and a description of behavioral model implemented in Matlab are presented. Section three describes the main non idealities errors in the ADC. The analysis and simulation results of the ADC model and comparisons with previously published works are provided in Section four. Finally, conclusion is drawn in section five.

2. The Behavioral Model of CM 8 Bits Pipeline ADC

There are several ADC architectures which are suitable for at least one or more specifications. The pipeline ADC is most suitable for low-power, high-speed medium-to-high resolution applications. This kind of the ADC employs several pipelined stages to achieve high speed and high resolution, Figure 1 shows the block diagram of 0 8-bit CM pipelined ADC.

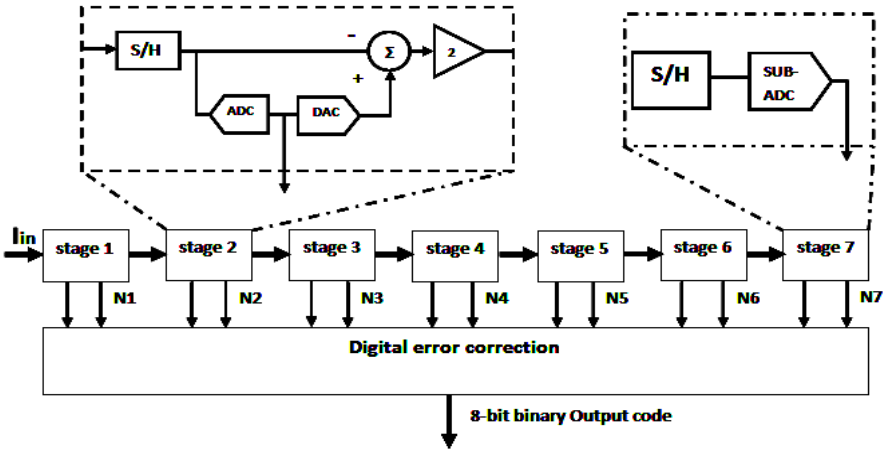

Figure 1. Block Diagram of 8-bit CM Pipelined ADC

The operation principle of CM pipeline ADC is similar to the conventional voltage mode ADC. It consists in each stage current S/H, current 1.5-bit Sub-ADC and a current Sub-DAC, except the last stage, which has a current S/H and a 2-bit current Sub-ADC, the Sub-ADC in each pipelined stage is flash type.

2.1 1. 5 Sub-ADC Model

In each stage as shown in Figure 2, the signal is first sampled and held, then converted by 1.5bit sub-ADC. The sub-ADC is implemented by using two symmetrical comparison current levels – Iref/4 and Iref/4 and an encoder logic circuit as it is shown in Figure 3. The bitM and bitL bits are applied to the digital error correction logic to generate the final bit. Three bits (outx, outy and outz) are converted back to analog value by Sub-DAC. The output current from sub-DAC is subtracted from the held input current. The difference is amplified by a

factor of two to produce an output residue current. The residue current is applied to the next stage as an input.

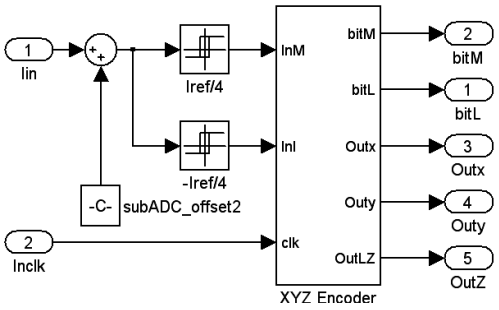

Figure 2. 1.5 Sub ADC Model

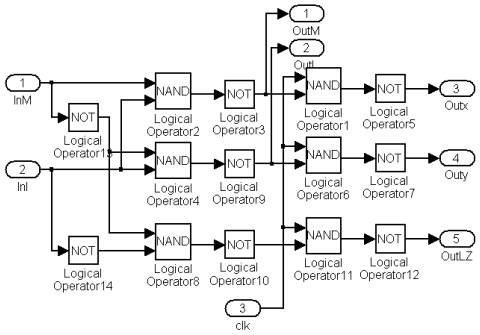

Figure 3. XYZ Encoder

2.2 1. 5 Sub-DAC Model

The current-mode approach (including the switched-current (SI) technique) has been proposed as a solution to many problems [12]. The most important and critical part of a pipelined stage is the multiplying digital-to-analog converter (MDAC). This part consists of S/H, sub-DAC, subtractor and residue amplifier. The current S/H and current sub-DAC are implemented by using a switch current and current source. The SI technique for analog signal processing has gained interest because of its advantages over the switched-capacitor (SC) technique [13]. This can operate at low voltages and high speed. It can be implemented in standard digital processes without precision capacitances or resistors. Since no capacitors or resistors are used in the MDAC, this will allow the current pipeline ADC to be made with small area implementation compared to the voltage mode data converter. Figure 4 illustrates the NMOS switching configuration and model of current sub-DAC, the current outputs are Iref/2, 0, –Iref/2 for the input codes 100, 010 and 001, respectively.

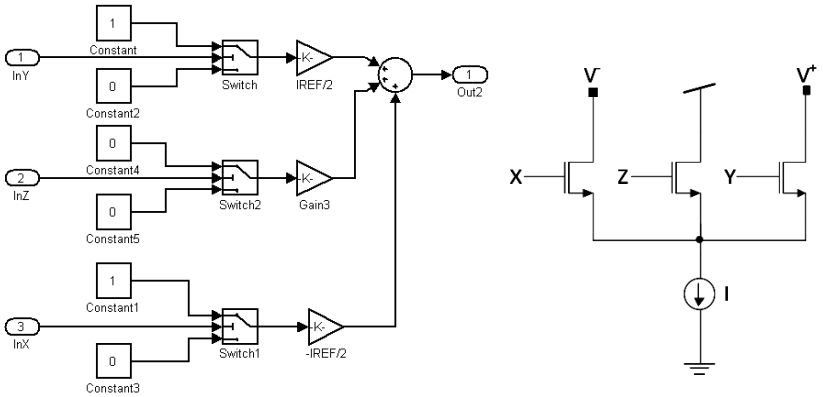

Figure 4. NMOS Switch Configuration and Its Model of Sub DAC

2.3 Digital Block Structure

The digital circuit in the converter pipeline fulfills the function of numerical correction of error combining the binary results of each stage in a final binary number with N bits. It contains logic of correction. The technique of numerical correction of error (DEC) is largely used to correct the errors of shift in the ADC pipeline. The logic of correction of numerical error made up mainly by full adders to compose the ripple carry adder.

3. Non Idealities Sources in CM Pipeline ADC

The non-ideal effects will worsen the overall ADC performance. In this section the most important effects in the CM pipeline ADC are discussed. The main non-ideals errors analysis discussed in this section are; the clock feed-though, charge injection, switching noise, clock jitter, components matching errors and OTA gain error.

3.1 Non Idealities in Current Sample and Hold

The model of the CM S/H is shown in Figure 5, the S/H circuit suffers from various non-ideality sources; such as components mismatch, charge injection, clock feed through, clock jitter, thermal noise, and flicker noise.

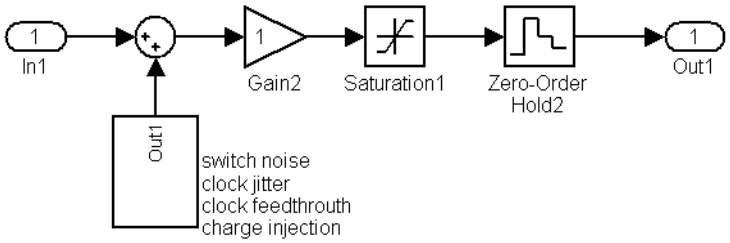

Figure 5. CM Sample and Hold Model

3.1.1 Charge Injection and Clock Feed-Through

The charge injection is becomes the main error source for switched-current circuits (current S/H, current Sub-DAC), because current is more sensitive to injected charge than voltage signal in switched-capacitor circuits [14], thus causing more error and degrading the performance of the circuits [15],caused by the amount of charge in MOS transistor channel and parasitic associated with the sampling switches while turning off, the charge under the gate oxide resulting from the inverted channel is approximated by

$$Q_{ch} = C_{ox} * W * L * (V_{GS} - V_{TH}) \qquad (01)$$

Where Cox is the thin-oxide capacitance per unit width, W and L are the channel width and length respectively, VGS is the gate-source voltage and VTH is the threshold voltage of the device. The charge injected via the drain does not introduce error. In contrast, the charge injected on the source, introducing an error in the charge stored on the sampling capacitor, the error voltage caused by the charge injection can be expressed as

$$\Delta V_{INJ} = \frac{Q_{ch}}{2*C} = \frac{C_{OX}*W*L*(V_{GS}-V_{TH})}{2*C_{gs}} \qquad (02)$$

Figure 6 presents the charge injection simulator module achieved by a derivative block. The random variable generator block generates outputs in a form of series of pulsed signal. After passing through the derivative block, the zero-order block is used to specify the time constant of charging and gain factor is used to adjust the amount of the charge injected

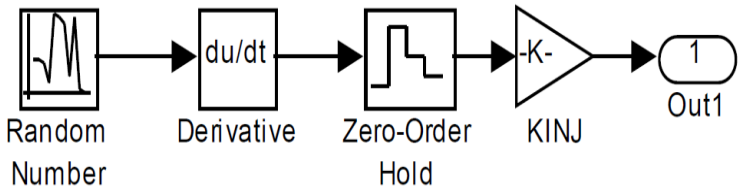

Figure 6. Charge Injection Model

The basic switched-current S/H circuit with parasitic capacitances, also named current memory cell (SI) is shown in Figure 7

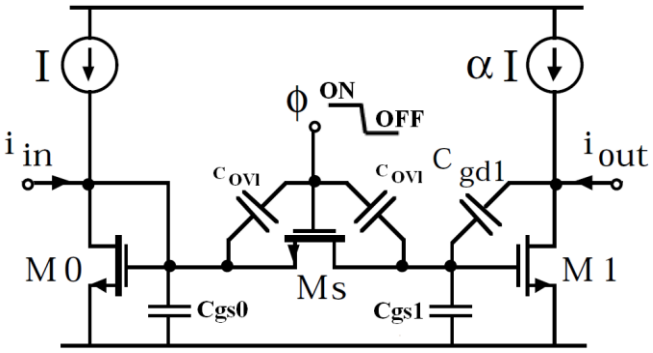

Figure 7. The Basic Switched-Current S/H Circuit

The other main factor of error in MOS switches is clock feed through, caused by the overlap capacitance (Covl) between the gate and source or drain terminals as shown in figure (04). When the gate voltage swings from high to low level, Covl conducts the transition and changes the voltage stored on holding capacitor (Cgs1), in the fast clock transition, the error can be expressed as

$$Eclk = \frac{3}{2} \times \Delta\phi_{clk} \times \frac{W_s}{W_1 \times L_1} \times \left(\frac{\eta}{2} \times L_{S1} + L_D\right) \qquad (03)$$

The $\Delta\phi$ is the amplitude of the control signal.

$\Delta\phi_{clk} = \phi_{low} - \phi$,

and $\eta = \frac{\phi_{high} -}{\Delta\phi_{cl}}$ is the lateral diffusion length.

3.1.2 Switching Noise

The noise in current-mode circuits (current comparator, current S/H and current Sub-DAC) is extremely depending on the noise sources that exist in CMOS transistor. The two important noise sources can be distinguished in a MOSFET transistor are thermal noise and flicker noise.

A. Thermal Noise

The noise in CMOS transistor is divided into current and voltage noise. The thermal noise is often the major device noise contribution limiting ADC resolution in CMOS circuits. It is caused by the thermal motion of the charge carriers in the channel of the device [15]. Figure 08 (a) shows simple model of the sampling. If the transistor MOS is operating in the linear region, it can be modeled as a voltage source in series with the device. It is basically identical to a passive resistor having Ron = 1/gds. As showing in Figure 8 (b) [16]

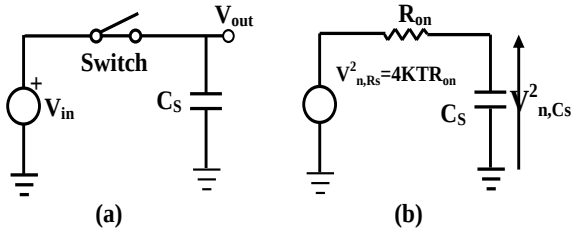

Figure 8 (a). Simple Model of a Sampling Switch, (b) Noise Equivalent Circuit

Thermal noise exhibits no frequency dependency. It has an uniform (or white.) power spectrum density (PSD), its estimated value is given by [15]

$$s_{th}(f) = 4 \times K \times T \times R_{on} \qquad (04)$$

Where k is the Boltzman constant, T is the absolute temperature.

The spectrum of Vn,cs is given by the 4KTRon spectrum multiplied by the square of the transfer function of the Ron Cs filter, the spectrum of Vn,Cs is given by [16]

$$V_{n,c_s}^2(w) = \frac{4 \times K \times T \times R_{on}}{1+(w \times R_{on} \times C_s)^2} \qquad (05)$$

The thermal noise voltage generated by the network in the frequency band from f1 to f2 is given by [17]

$$v_t = [4 \times K \times T \int_{f_2}^{f_1} R_e(z) df]^{1/2} \qquad (06)$$

Where Re(z) is the real part of z. they are given by

$$z = R_{on} // (1/j2\pi f C_S) \qquad (07)$$

and

$$R_e(z) = \frac{R_{on}}{[1+(2\pi f R_{on} C_S)^2]} \qquad (08)$$

The total noise power stored on Cs when the switch goes off is

$$v_t = [4 \times K \times T \int_0^{\infty} \frac{R_{on} \times df}{1+(2\pi f \times R_{on} \times C_s)^2}]^{\frac{1}{2}} = \sqrt{\frac{K \times T}{C}} \qquad (09)$$

In the saturation region, the PSD of the thermal noise current is given by [18]

$$I_d^2 = KT \frac{4}{3} g_m \qquad (10)$$

Where gm is the transconductance of the MOS transistor.

The thermal noise is usually modeled as an additive white noise source with Gaussian distribution [19]. Figure 09 presents the thermal noise model, it can be modeled as a random variable generator with zero-order block, the gain block is used to adjust the value of the total thermal noise.

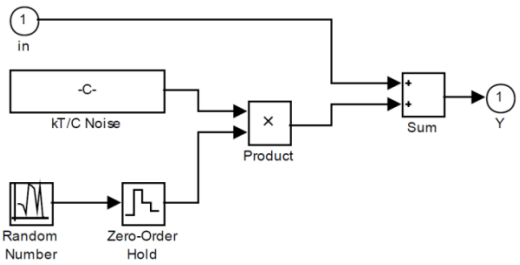

Figure 9. Thermal Noise Model

B. Flicker Noise

The flicker noise or 1/f noise phenomenon has been observed in almost all kinds of devices with resistive components. MOS transistor shows the highest 1/f noise due to its surface conduction mechanism. Other authors attribute this noise to mobility fluctuations. This noise component typically increases with technology scaling [20], The PSD of the flicker noise current is [21]

$$I_d^2 = \frac{K_f * g_m^2}{C_{ox} * W * L * f} \qquad (11)$$

Where Kf is a process dependent parameter, W and L are the width and the length of the transistor respectively and f corresponding frequency.

3.1.3 Clock Jitter

Sampling clock jitter is another phenomenon that has attracted attention in the design of ADCs [22]. Sampling of the analog input does not occur exactly at the desired time. This uncertainty Δt in the sampling instant is commonly called jitter. This non-ideal factor produces a conversion error proportional to the slope of the signal; the error result from clock jitter can be expressed as [23]

$$y(t + \Delta t) - y(t) = \Delta t * \frac{d}{dt} y(t) \qquad (12)$$

For sine wave, jitter can be introduced in general form input with sinusoidal input signal [24], as shown in Figure 10 , where A is the input signal amplitude, is the input signal frequency and is the time jitter error, The maximum amplitude error Δy_i of the jitter model can be expressed as

$$\Delta y(t)|_{\max} = \Delta t . A . \frac{d \cos(2\pi f_{in} t)}{dt}\Big|_{t=0} = A . \Delta t . 2\pi f_{in} \qquad (13)$$

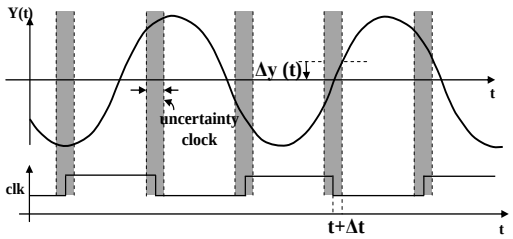

Figure 10. Clock Jitter Error Signal

Figure 11. Show the behavioral model clock jitter effect [24]

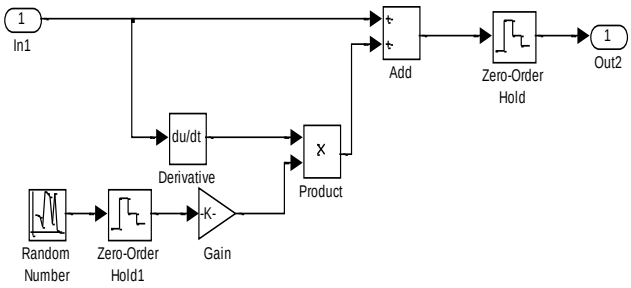

Figure 11. Clock Jitter Model

3.2 Factors Non-ideal in Current Comparator

The design of the comparators is very critical part in the data converter and directly affects the performance of the circuits, Figure 12. Present the comparator model with the main

limitation, the main non-ideality sources in the comparator are the comparator offset and the thermal noise.

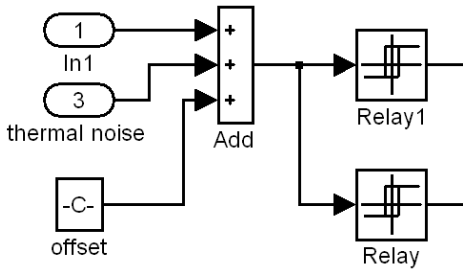

Figure 12. Comparator Model

3.3 Matching Errors in Current Sources

The converter accuracy is limited by the matching accuracy of the analogue converter elements (cmos switch, current source). Basically, CMOS current source circuits suffer from three main mechanisms responsible for mismatch errors, transconductance mismatch β, threshold voltage mismatch Vth and channel length modulation mismatch λ. The transconductance parameters include the variation of μ and COX. As it is shown in this equation $\beta = \mu . C_0$, the mismatch errors coming from the variation of threshold voltage and channel length modulation is caused by physical parameters.

The current S/H and current steering DAC use generally principle of current mirror as basic building block; Figure (13) illustrate the first generation of CM S/H and the basic current DAC.

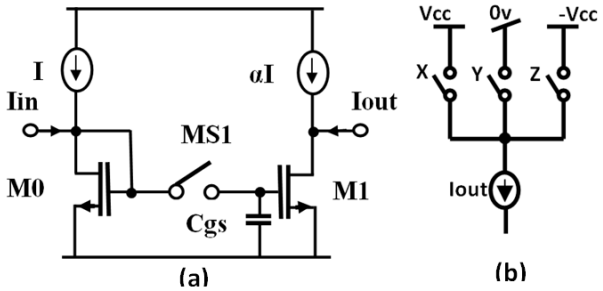

Figure 13 (a). Basic Current S/H, (b) Basic Current DAC

In the current S/H, the drain current of M0 can be written as the following;

$$I_{ds0} = I + I_{in} = \frac{B_0}{2} \times (V_{gs} - V_{th0})^2 \times (1 + \lambda_0 \times V_{ds0}) \quad (14)$$

Due to mismatch errors, the drain current in device M1 can be written as

$$I_{ds1} = I + I_{OUT} = \frac{B_0 + \Delta B}{2} \times (V_{gs1} - (V_{th0} + \Delta V_{th}))^2 \times (1 + (\lambda_0 + \Delta\lambda) \times V_{ds1}) \quad (15)$$

By using equations (13) and (14), the following equation is obtained;

$$\frac{I_{ds1}}{I_{ds0}} = \left(1 + \frac{\Delta B}{B_0}\right) \times \left(1 + \left(\frac{\Delta V_{th}}{V_{gs} - V_{th0}}\right)^2 - 2 \times \frac{\Delta V_{th}}{V_{gs} - V_{th0}}\right) \times \left(1 + \frac{\Delta\lambda \times V_{ds0}}{1 + \lambda_0 \times V_{ds0}}\right) \quad (16)$$

using the last equation, the following reltion between drain current of M0 and M1 is obtained

$$I_{ds1} = I_{ds0} . (1 + \varepsilon) \quad (17)$$

Ideally in the current S/H, the drain currents of both the input and the output transistors have the same value. However, due the mismatch error, an offset current is obtained.

In the ideal current DAC, the total output current is given by

$$I_{OUT} = [b_{N-1}(n) * 2^{N-1} + \cdots + b_1(n) * 2 + b_0(n)] * I_{unit} \quad (18)$$

In the non-ideal model, the current source in current DAC is modeled as a nominal current source Ik in parallel with error source Ek as shown in figure (14)

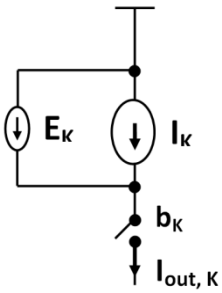

Figure 14. Non-ideal Model of Current Source

The output current of non-ideal DAC is give by

$$I_{OUT}(n) = \sum_{K=0}^{N-1} b_k\,(n) * I_{OUT,K} \qquad (19)$$

Where

$$I_{OUT,K} = I_{unit} * 2^K + E_K \qquad (20)$$

3.4 The Non Idealities in Current Amplifier

The different current amplifier topologies have been already and widely discussed in the literature treating the topic of analogue integrated circuit design [25-27]. There are two main basic current amplifiers. The first proposal current amplifier is implemented by current mirrors. For the second type, it is known source-coupled pair or differential current amplifier stage. As shown in Figure 15, such as all transistors operating in the saturation region.

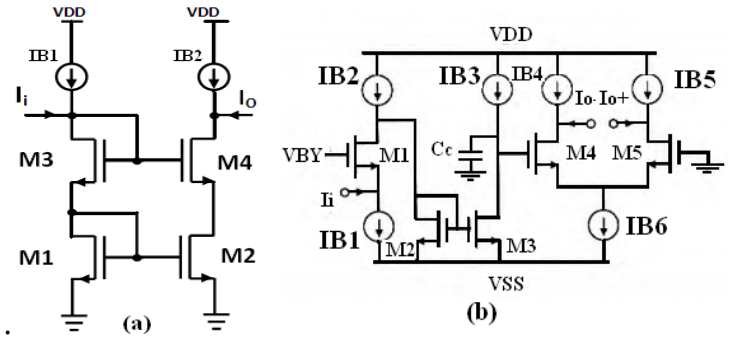

Figure 15 (a). Cascode Current Amplifier, (b) Differential Current Amplifier

The current amplifier suffers from a number of a various non idealities factors. Those factors are; input current offset, amplifier slew-rate, amplifier thermal noise and mismatch errors. In this section, the main non-idealities and their effects on current amplifier are discussed.

3.4.1 Matching Errors

In the current amplifier, the current gain is proportional to the aspect ratio of transistor M1 and M2 as shown in Figure 15 (a), as it is given by this equation

$$A_i = \frac{I_{out}}{I_{in}} = \frac{B_2}{B_1} \times \left(\frac{v_{gs2} - v_{t2}}{v_{gs1} - v_{t1}}\right)^2 \times \left(\frac{1+\lambda_2\, v_{ds2}}{1+\lambda_1\, v_{ds1}}\right) \qquad (21)$$

The current amplifier suffers from various non idealities factors (devices mismatches) such as nonlinear gain segments which caused by the nonlinear transconductance, non idealities due to the channel length modulation λ, and non idealities due to the VT mismatch. The current gain of the current amplifier with mismatches taken into account is given by

$$I_{out} = A_i \square(I_{in} + I_{bais} \square\square) + \delta A_i \ (I_{in} + I_{bais}) \quad (22)$$

Where δ is the mismatch coefficient express by

$$\delta = \delta B + \delta v_{gs} + \delta v_t + \delta\lambda \quad (23)$$

As a consequence of the device mismatches, there will be a constant offset error at the output gain current.

4. Simulation Results

To confirm and check the specifications of the new architecture version of the pipeline ADC model, a simulink model of the ADC has been implemented in order to simulate some parameters. Simulation results with dynamic and static performance are presented in this section. MATLAB and simulink environment are used for this study. In the ideal case, and with the introduction of various non-idealities factors reported in previous sections for non-ideal model, it has been demonstrated how the parameters of the converter are affected by the non-idealities factors.

In order to extract signal to noise ratio (SNR) and superious free dynamic range (SFDR), the power spectrum is plotted with the application to the input of the ADC an analogue signal equivalent to sine wave with input frequancy 3 Mhz, the sampling rate of the ADC is 100 Mhz, the input signal and th output reconstruction analogue signal in non-ideal model are shown in Figure 16, the fast fourier transform (FFT) ploted in Figures 17 and 18, with the input frequncy 100khz and 1Mhz respectively. Such as we can extract the values of SNDR and SFDR around of 46.29 dB, 51.2 dB.

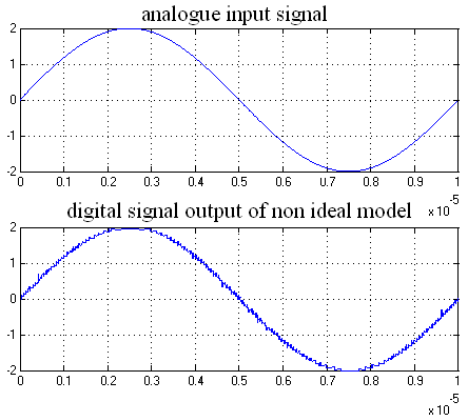

Figure 16. The Input Signal and Reconstruction Output for Fin=100 kHz, Fs=100 MHz

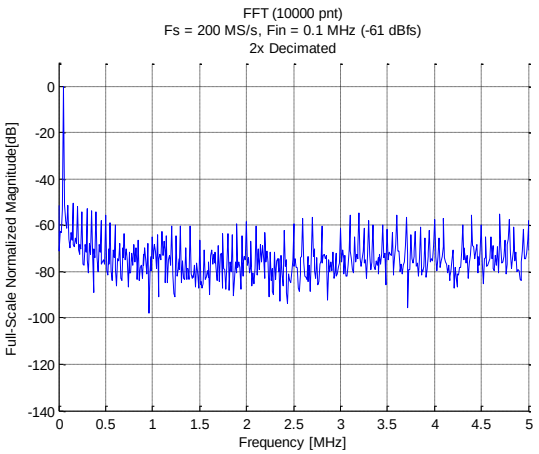

Figure 17. FFT of the ADC Output Signal with Fin = 0.1MHz; Fs = 100MHz

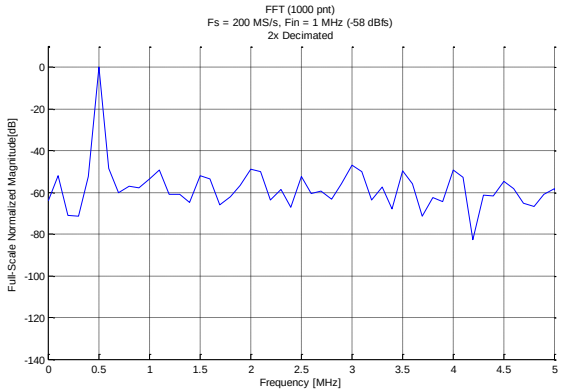

Figure 18. FFT of the ADC Output Signal with Fin = 1MHz; Fs = 100MHz

The linearity is the most important parameter in the data converter, the static performance includes Integral Non-Linearity (INL) and Differential Non-Linearity (DNL), Figures 19 and 20 shows simulation results of DNL and INL of CM pipeline model, the DNL and INL within the range of -0.06 to 0.16 LSB, -1.4 to 0.9 LSB This was obtained including various errors factors.

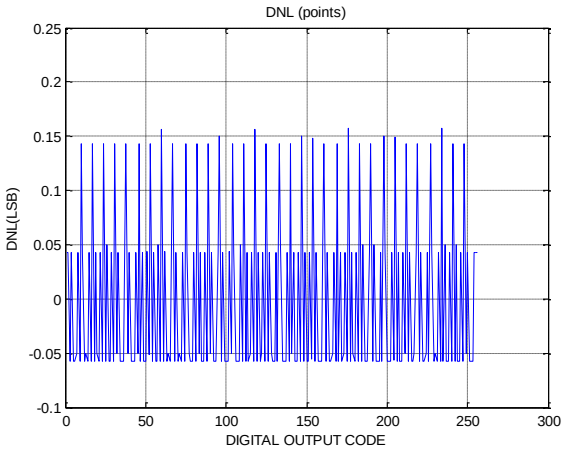

Figure 19. DNL 08-bit CM Pipelined ADC, Fin = 1MHz, Fs = 100MHz

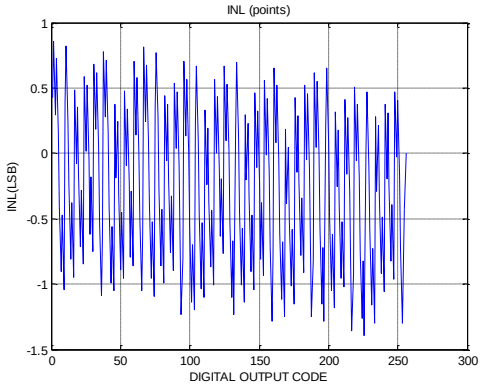

Figure 20. INL 08-bit CM Pipelined ADC, Fin = 1MHz, Fs = 100MHz

The results of the behavioral level simulations were a set of specifications for the mentioned non-idealities, which are shown in Table 1.

Table 1. CM Pipeline ADC Specifications from Behavioral Modeling

Specification	Value
Technology TSMC	0.18 μm
Resolution	08 bits
Offset of the amplifier	400nA
Hold capacitance *Cgs*	0.08fF
Overlap capacitance Covl	0.08 fF
Oxide capacitance *Cox*	$8.78*10^{-3}$ F/m2
Sampling frequency *fs*	100MHz
Offset of the comparator	200nA
Delay time of the comparator	60ns
Current flicker noise	$6*10^{-10}$ A
DAC component matching (ε)	<10 %

From the results presented in the previous sections, a comparison can be made between the CM pipeline model with the real ADCs [6-28]. It can be seen from Table 2 that proposed models shows a good match to the real ADCs; this proves the accuracy of our behavior model.

Table 2. Comparison the Performance of the Current Mode Pipeline ADC MODEL

Parameters	This work	[6]	[28]
Technology	**0.18µm**	**0.35µm**	**0.8µm**
Resolution (bit)	**8 bits**	**9 bits**	**10 bits**
Sampling rate	**100MHz**	**50MHz**	**20MHz**
INL (LSB)	**-1.4/0.9**	**0,9**	**0.9**
DNL (LSB)	**-0.06/0.16**	**0,7**	**0.9**
SNR (dB)	**46.25**	**52**	**40.8**
SFDR (dB)	**51.2**	**/**	**/**
SNDR (dB)	**46.29**	**/**	**/**

5. Conclusion

The behavioral modeling of mixed-signal CM circuits at a higher level was successfully performed. The development of CM pipeline ADC model using Matlab and Simulink with main advantageous of current mode circuits was presented. The model is used to analyze various non idealities and demonstrate how those errors factors affect the performance of the ADC. The analysis of static and dynamic performances confirms the good performance of the model. The behavioral model and the simulation results will help the design 8-bit current mode pipeline ADC circuit with low power and high efficiency in the chip area by using Sub current ADC and DAC blocks.

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