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Embedded and Digital Controller Based Multi Level Inverter

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Abstract

In this paper, a new symmetrical cascaded multilevel inverter is proposed. Multilevel inverter is a device which is capable of producing different voltage levels. The proposed multilevel inverter is analyzed in symmetric mode of operation. This paper proposes a cascaded multilevel inverter by using digital and embedded controller. In digital controller, by using four bit counter; the Boolean equation is formed from the switching table. These equations are given as the input to each switch of the inverter by using logic gates. But in embedded controller coding is used to trigger the pulse. This coding is written by using switching table. The proposed topologies can produce the five level output which are nearer to the sinusoidal wave. This proposed system is used to reduce the total harmonic distortion (THD). To validate the developed technique, simulations are carried out through MATLAB/SIMULINK.

Keywords: *symmetrical cascaded multilevel inverter, digital controller, embedded controller.*

1. Introduction

Multilevel inverters have become more popular over the years in high power electric applications without use of transformer and filters. Multilevel inverters are used in high power applications for reducing the voltage rating of semiconductor switching devices. The multi-level inverter is to synthesis a near sinusoidal voltage from several levels of DC voltages. The synthesized output waveform has more steps, which provides a staircase wave that approaches a desired waveform as number of levels increases. Also, as step are added to waveform, the harmonic distortion of the output wave decreases there by approaching zero as the number of voltage levels increases. The attractive feature of this technology is mainly used in medium to high voltage application and offers a number of advantages when compared to conventional two level inverter. Power electronic inverters are becoming popular for various industrial drives applications. Contemporary inverters have become a necessity for many implementations such as motor controlling, renewable energy system, and transportation and power systems. The disadvantages of multilevel configurations over the two -level inverter configuration are the increase in the number of power devices required and the circuit complexity, which necessitates complex control schemes that add to the cost and reduces the reliability of the converter. This may lead the overall system to be more complex. Therefore in practical implementation reducing the number of switches and gate driver circuits is very important. The multilevel inverter is used to produce a desired sinusoidal voltage from several separate DC sources. By using a multilevel inverter the stress on each switching device can be reduced proportional to the number of levels. Thus the inverter can handle higher voltage without using an expensive and bulky step up transformer in various applications. The number of inverter output voltage levels is increased the harmonic content will be low enough to avoid the need of bulky filters. Multilevel inverters generate the output voltages with very low distortion,

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produce smaller common mode voltage, draw input current with low distortion and can operate at both fundamental switching frequency and high switching frequency. Kang and Hyun [1] proposed a simplified method to calculate the relation between the reference phase voltage and the output phase voltage to the load neutral point. Boora et al [2] proposes a new single inductor multi output DC/DC converter that can control the dc link voltages of single-phase diode-clamped inverter asymmetrically to achieve voltage quality enhancements. Namei et al [3] developed a hybrid cascaded converter topology with series connected symmetrical and asymmetrical diode clamped H-bridge cells. Pereda and Dixon [4] suggested a solution for using only one dc source in asymmetric cascaded multilevel inverter. Najafi and Yatim [5] developed a new multilevel inverter which is used to reduce complexity and gate circuit. Kangarlu et al [6] proposes a new topology with reduced number of switches which is used to operate in high power, high voltage, improved output waveform quality and flexibility. Judi and Nowicki [7] propose bypass technique for multi level inverter to ensure even power distribution in all voltages sources. Kangarlu and Babaei [8] developed an optimal structure in different criteria such as number of switches, standing voltage on the switches, number of dc voltage sources etc. Babaei et al [9] proposed anew algorithm to determine magnitude of dc voltage source. Palanivel and Dash [10] developed using carrier pulse width modulation technique which is used for lower magnetic interference and high output voltages. The proposed topology is appropriate for battery powered applications (such as electric vehicle and submarine propulsion). Main advantages of this topology are better control and protection of each H-bridge.

2. Proposed Topology

The general structure of the multilevel inverter is to synthesize a near sinusoidal voltage from several levels of dc voltages. The synthesized output waveform has more steps which produce a staircase wave that approaches a preferred waveform as the number of levels increases. By increasing number of level will enhance these advantages. But it can impose a substantial expense due to increase the circuit complexity and reduce the reliability. The attractive feature of proposed technology is mainly in the range of medium to high voltage application and offers a number of advantages when compared to the conventional two-level inverter. Cascaded H-bridge multilevel inverters have been received a great attention because of their merits such as minimum number of components, reliability and modularity A new topology of multilevel inverter is proposed. Each block can be considered as a multilevel inverter. The fundamental block and generalized topology are presented. Therefore, a detailed study of power loss and calculation of PIV are given. Finally, computer aided simulations are verified by using MATLAB/ SIMULINK. Symmetric multilevel inverter is considered to make by series connection of n symmetric blocks. The overall output voltage is equal to summation of output voltage blocks.

2.1. Explicit Block Diagram of Proposed Topology

The basic block of proposed multilevel inverter consists of $2V_{dc}$ voltage sources. Generally, the voltage sources can be unequal. If dc voltage sources have same voltages, then the block will be analyzed in symmetric mode. Fig 1 shows that the basic block of multilevel inverter includes 6 semiconductor switches S_1, S_2, S_3, S_4, S_5 and S_6. Each switch is connected with an anti-parallel diode. In addition to mentioned ingredients and to have proper operation of circuit,8 diodes D_1, D_2, D_3, D_4, D_5, D_6, D_7 and D_8 can be employed. As a matter of fact, anti-parallel diode and 8 diodes are undertaken for conduction of backward current. Backward current is caused by inductive characteristic of

load. In the viewpoint of obtaining a sinusoidal output voltage wave, multilevel inverters may increase the number of output voltage levels. However, it will need more module end result in complexity and cost increase. The number of switches, IGBT drivers and independent DC sources, power losses, complexity of control algorithm, number of levels and total harmonic distortion for output voltage waveform, voltage stress on semiconductor devices and also the rate of standing voltage for switches are the optimization subjects in new topologies. The stress on each switching device can be reduced by using the multilevel inverter which is proportional to the number of levels of multilevel inverter method. Two methods are implemented in this paper. In digital controller, Flip flop is a data storage element that has two stable states. It is used to store the state information. Flip flops can be spitted into types. It can be simple or clocked. The simple one is latches, while clocked devices are called as flip flops. While, in embedded controller, by using switching table, codlings are used to trigger the pulse. V_{rms} and THD value are compared with digital controller and embedded controller. In both methods the simulation parameters chosen are V_{dc1} = 100V and V_{dc2} = 100V.

$$V_{dc1} = V_{dc2} \qquad (1)$$

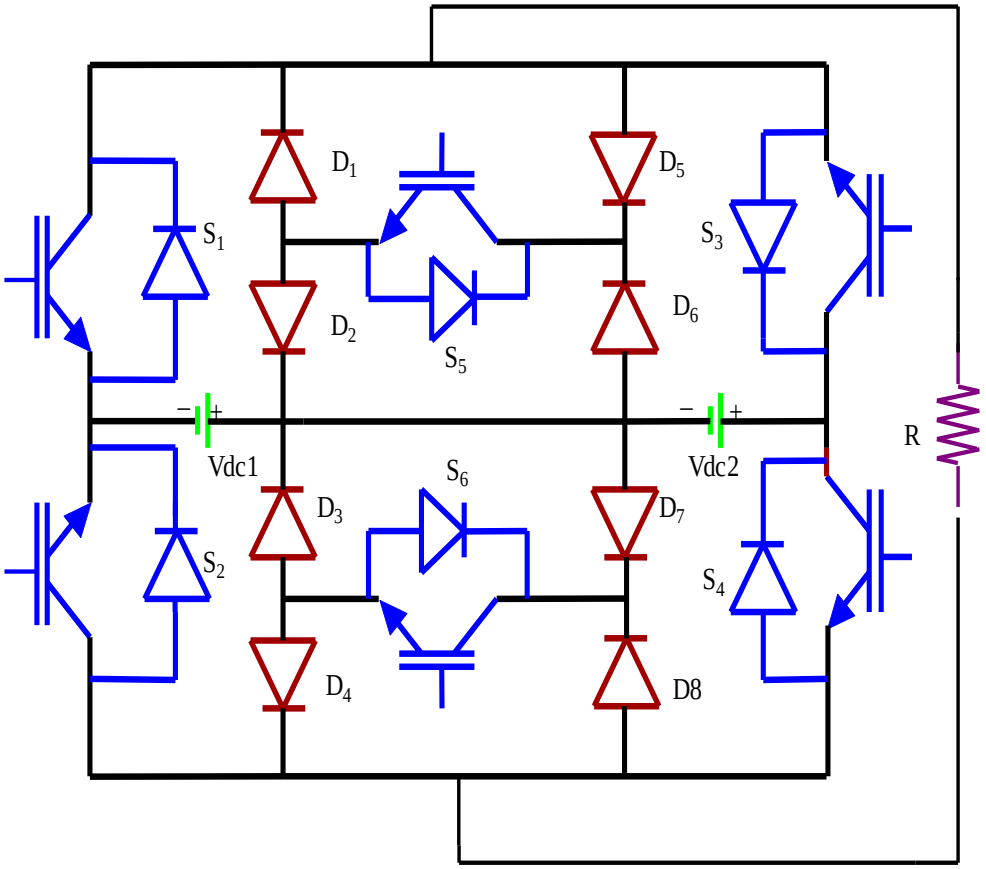

Figure1. Block Diagram of Proposed Multilevel Inverter

Table 1. Switching Table for Proposed Topology

S_1	S_2	S_3	S_4	S_5	S_6	Output Voltage
1	0	1	0	0	0	$+2V_{dc}$
1	0	0	0	1	0	$+V_{dc}$
0	0	1	1	0	0	0
0	1	0	0	0	1	$-V_{dc}$
0	1	0	1	0	0	$-2V_{dc}$

Table 1. Represents the switching states of the five level cascaded multilevel inverter. Here S_1, S_2, S_3, S_4, S_5, S_6 represents the switches of the multilevel inverter and V_{dc} represents the input voltage source. To obtain $2V_{dc}$ switches S_1, S_3 will be turned ON, and other switches will be turned OFF. For V_{dc} switches S_1, S_5 will be turned ON . For $0V_{dc}$ switches S_3, S_4 will be ON state. To get $-V_{dc}$ switches S_2, S_6 will be turned ON, and remaining switches will be turned OFF and switches S_2, S_4 will be in ON state for -2Vdc.

3. Modulation Strategy

The proposed topology is
1. Digital Controller
2. Embedded Controller

3.1. Digital Controller

In this method, logic gates and flip flop are used to generate pulses. The following Boolean equations are formed by using switching state and four bit counter.

P_1=D'CA'+ D'B'A+D'C'B (1)
P_2=DCA'+DB'A+DC'B. (2)
P_3=D'CB'+D'C'B+C'B'A'+CBA (3)
P_4=DCB'+DC'B+C'B'A'+CBA (4)
P_5=D'CBA+D'C'B'A (5)
P_6=DCBA'+DC'B'A' (6)

The above equation is given as input for logic gates and flips flops. These equations are obtained by using logic gates. The logic diagram for each switch is given as the input. The schematic diagram for JK flip flop is shown in Fig 2.

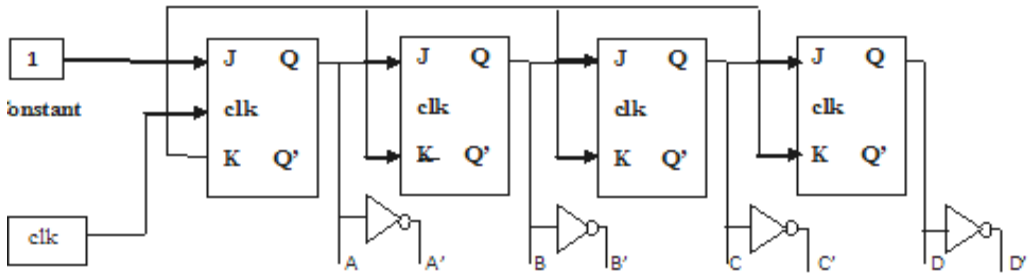

Figure 2. Schematic Diagram of JK Flip Flop

The output of the JK flip flop represent as A A', B B', C C', and D D'. For each switches these output are given as the input to the logic diagram which is formed by using logic gates. Each switch has the separate logic diagram.

A logic gate is a physical device which is used to implement a Boolean function. It performs a logical operation with one or more logical inputs and produces a logical output. This topology produces the five level output with reduced Total Harmonic Distortion (THD). Figure 3. Represents the simulation output of the five level flip flops based cascaded multilevel inverter. The cascaded five level inverter can be modeled in SIMULINK model by using power system block set. Switching signals for MLI are developed using flip flop topology. Figure 4. Represents THD plot for five level inverter based on flip flop topology.

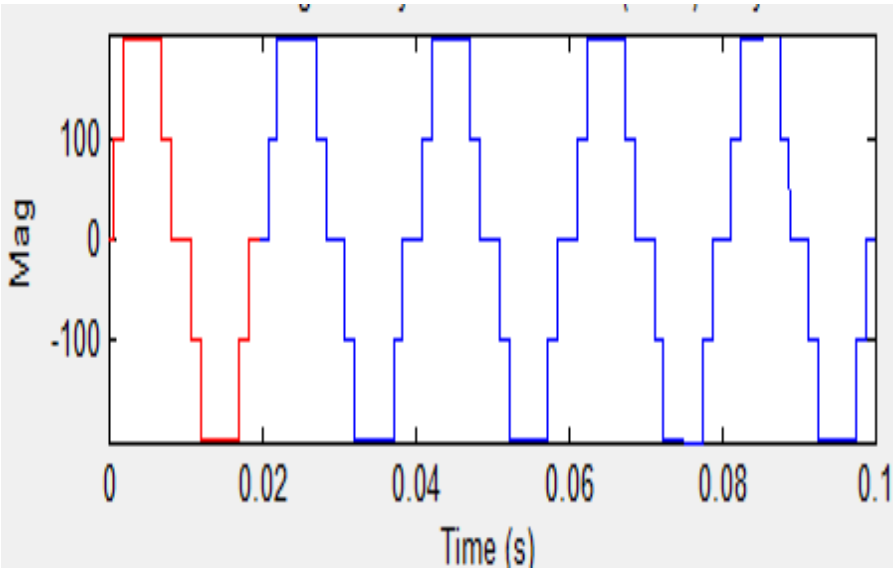

Figure 3. Output Voltage of Five Level Inverter based on Digital Controller

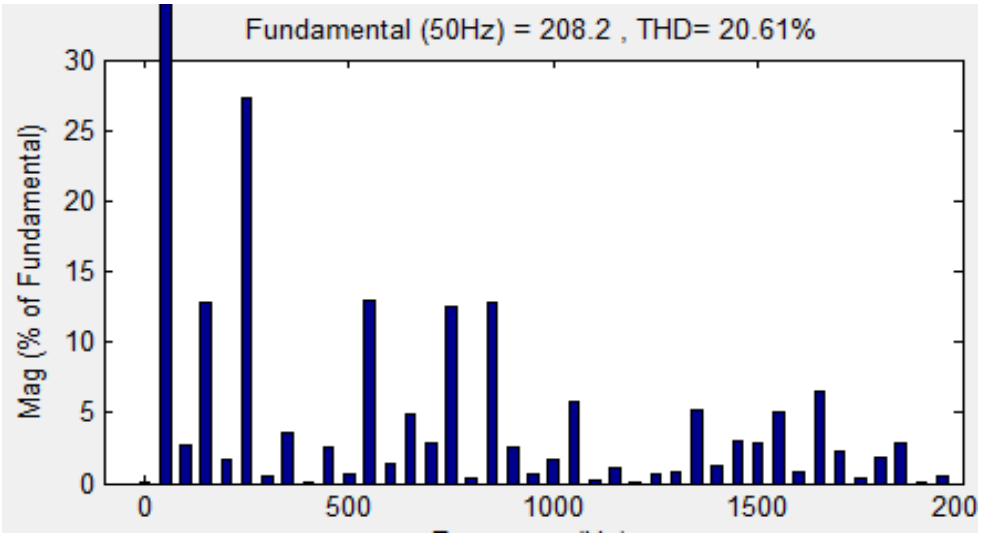

Figure 4.THD Plot for Five Level Output Voltage based on Digital Controller

3.2. Embedded controller

Embedded Controllers (ECs) are often found in low power embedded reference designs. It performs a range of input/output and system management functions. Embedded controllers are often the heart of an industrial control system or a process control application. They may also be at the center of a portable data acquisition system or remote controller that allows an application to keep running even if its umbilical link to the outside world is cut. Embedded controller coding are used to trigger the pulse. Coding is written by using switching table.

The switching pattern scheme is used to improve the performance of multilevel inverter. The proposed inverter topologies can synthesize high quality output voltage near to sinusoidal waves. Unlike other schemes, the proposed method significantly reduces the Total Harmonic Distortion (THD) and switching losses.

The circuit configuration is simple and easy to control. Figure 5. Represents the simulation output of the five level multilevel inverter based on embedded controller. The cascaded five level inverter can be modeled in SIMULINK by using power system block set. Switching signals for MLI are developed with the help of the embedded controller. Figure 6. Represents the THD plot for five level output voltage based on embedded controller.

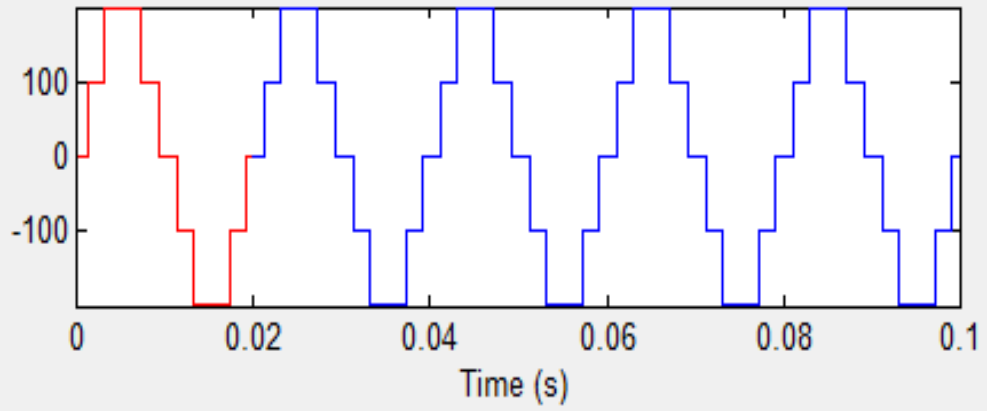

Figure 5. Output Voltage of Five Level Inverter based Embedded Controller

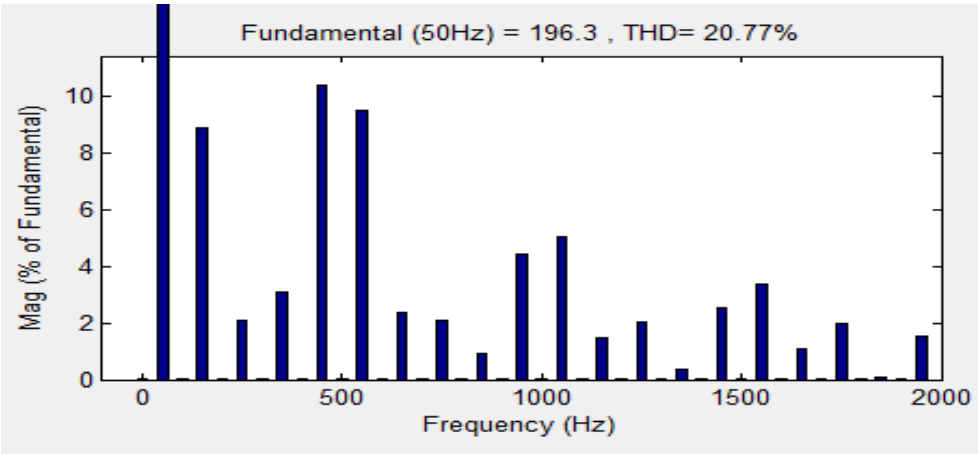

Figure 6. THD Plot for Five Level Output Voltage based on Embedded Controller

4. Conclusion

The proposed digital and embedded controller based method produces five level output voltage. Both methods are operated in symmetric mode. Triggering pulses are generated with the help of codings using embedded controller for all the switches. For digital controller, flip flop and logic gates are used to generate pulse. The proposed inverter can synthesize high quality output voltage near to sinusoidal waves. It is used to provide better performance than the conventional multilevel inverter and also this proposed methods is used to reduce the switching losses and total harmonic distortion (THD). Switching scheme has been improved the performance of the multi-level inverter. Comparing the two methods, the flip flop based controller gives better performance.

Table 2. Comparison between Digital and Embedded Controller

Topology	Digital controller	Embedded Controller
THD	20.61%	20.77%
V_{peak}	208.2	196.3
V_{RMS}	147.2	138.8

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