International Journal of Hybrid Information Technology
Vol.8, No.11 (2015), pp.181-188
http://dx.doi.org/10.14257/ijhit.2015.8.11.15

Design of Low Power Signed Multiplier Based on EMBR Techniques

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Abstract

Multiplier is the major component for processing of large amount of data in DSP applications. Using different recoding schemes in Fused Add-Multiply (FAM) design for the reduction of power and look up tables. The performances of 8-bit, 12-bit & 16-bit signed multipliers were designed and obtained results are tabulated using Efficient Modified Booth Recoding (EMBR) techniques, which can be used for low power applications.

Keywords*-FAM, Signed, Modified Booth Multiplier, EMBR, Low Power VLSI*

1. Introduction

In good olden days, multiplication was generally achieved by a chain of addition, subtraction, and shift operations. Presently, electronic applications make ample use of Digital Signal Processing, based on huge number of arithmetic operations. Multiplication [2] is one of them, reflected as repetitive additions. The number to be added is the multiplicand, the number of times added is the multiplier, and the end result is the product. Basic operation of multiplication involves partial products creation and accumulation. Process can be in two ways: reducing number of partial products and/or accelerating accumulation. System's presentation primarily depends on multiplier performance. The final Carry Look Ahead (CLA) [8] adder and The Carry Save Adder (CSA) tree used for speediness operation.

2. Motivation

Implementations of shift and add multipliers can elevate performance over software synthesis, but are still slow. The reason is that as each supplementary partial-product is summed a carry must be propagated from the least significant bit (LSB) to the most significant bit (MSB). This carry propagation is overwhelming, and must be repeated for each partial product to be summed. Such a technique was first proposed by Booth [6]. The original Booth's algorithm [1, 6] of closest strings l's by using the property that: $2 + 2(l-1) + 2(l-2) + \ldots + 2n) = 2(l+l) - 2(l-n)$. Although Booth's algorithm yields at most N/2 encoded partial products from an N bit operand, the number of partial products produced differs. As a result different versions of Booth's algorithm for multipliers are used. Modified Booth Encoding, halves the number of partial products to be summed.

3. Modified Booth Multiplier

In this paper multiplication involves Modified Booth (MB) [6, 7, 11] form. In this generation of at most n/2+1 partial product; it is a redundant signed-digit radix-4 encoding technique. The partial products are decreased to half in multiplication relating to any other radix-2 version.

ISSN: 1738-9968 IJHIT

3.1. Algorithm

1. The LSB padded with one zero.
2. The MSB padded with 2 zeros in case of even and 1 zero in case of odd.
3. Overlapping groups of 3-bits are created by dividing the multiplier.
4. Partial product scale factor is determined from modified booth to form table of encoding.
5. The Multiplicand Multiples are computed.
6. Partial Products are summed.

The process of encoding is done by grouping of three bits at a time and must be able to add multiplicand times –2, -1, 0, 1 and 2. As Booth recoding [6] got rid of 3's, generating partial products is not that rigid (shifting and negating). After the grouping of partial products, they are added, weighted appropriately, through a Carry-Save Adder (CSA) tree. Carry - Save.

Further, carry look ahead adder, a carry signal will be generated in two cases: (1) when both bits s and t are 1, or (2) when one of the two bits is 1 and the carry-in is 1. The Carry Look Ahead adder (CLA) [8] resolves the carry delay problem by computing the carry signals in advance, centered on the input signals. This addition reduces all partial-products down to a carry-save number by summing them up in an adder tree.

Table 1. Grouping Table

y_{2j+1}	y_{2j}	y_{2j-1}	y_j^{MB}	s_j	one_j	two_j	c_{inj}
0	0	0	0	0	0	0	0
0	0	1	1	0	1	0	0
0	1	0	1	0	1	0	0
0	1	1	2	0	0	1	0
1	0	0	-2	1	0	1	1
1	0	1	-1	1	1	0	1
1	1	0	-1	1	1	0	1
1	1	1	0	1	0	0	0

$one_j = y_{2j-1} \oplus y_{2j}$ $\quad two_j = (y_{2j+1} \oplus y_{2j}).\overline{one_j}$ $\quad s_j = y_{2j+1}$

4. Recoding Techniques of Sum to Efficient Modified Booth (S-MB)

4.1. Arithmetic of Structured Signed

Increasing multiplier piece is by means of recoding of partial products to be summed. Conventional and signed HAs and FAs [1, 10] are to be used, each of the three schemes are applied in either signed (2's complement representation) which consist of even number of bits.

In the following techniques, both inputs are in 2's complement form for signed, consist of bits 2k in case of even or 2k+1 bits in case of odd bit-width [9] considered. In this method of recoding, recoding the sum of two consecutive bits of the input S (s2j, s2j+1) with two consecutive bits of the input T (t2j, t2j+1) into one MB digit Y_J^{MB}. Two types of HAs in signed form used which are referred as HA* and HA**.

$$Y = S + T = y_k . 2^{2k} + \sum_{j=0}^{k-1} y_j{}^{MB} . 2^{2j} \quad (1)$$

Where $y_j{}^{MB} = -2\, s_{2j+1} + s_{2j} + c_{2j}$.

4.2. Techniques of S-MB Recoding

4.2.1. Signed Input Numbers: If the input numbers S and T are signed, their MSB is negatively signed. Below represents are S-MB schemes for even bit-width of S and T. The basic recoding block in all schemes remains unchanged.

Using these in FAM model [4] which depends on the MB algorithm is designed. The term S = $(S_{n-1}S_{n-2} \ldots S_0)$ 2's is encoded based on the MB algorithm [1, 10] and multiplied with T = $(T_{n-1}T_{n-2} \ldots T_0)$ 2's. Both S and T consist of n=2k bits are in 2's complement type.

After the partial products generated, added, suitably weighted, by using Wallace Carry-Save Adder (CSA) tree along with the Correction Term (CT) which is specified by the following equation (4):

$$R = S.\ T = CT + \sum_{j=0}^{k-1} PP_j \ .\ 2^{2j} \qquad (2)$$

4.2.1.1 Technique of S-MB-1

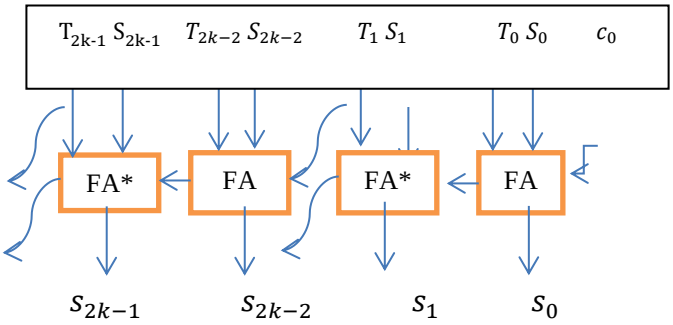

Figure 1. Technique of Signed S-MB1 Even Bits

4.2.1.2 Technique of S-MB-2

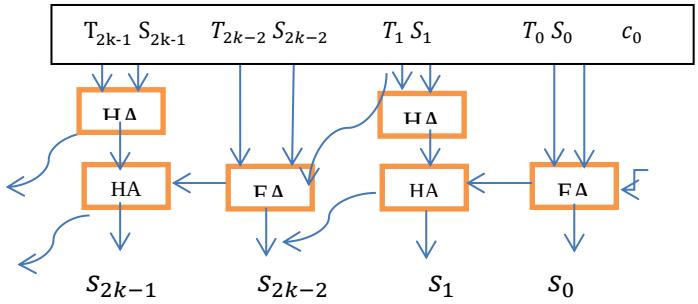

Figure 2. Technique of Signed S-MB2 Even Bits

4.2.1.3 Technique of S-MB-3

4.2.1.4

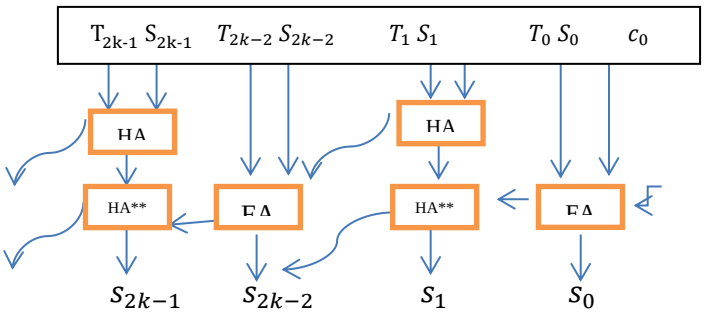

Figure 3. Technique of Signed S-MB3 Even Bits

6. Results

An Efficient Modified Booth Recoding techniques based 8, 12 and 16-bit multipliers were designed in FAM model and simulated using Xilinx tool of device power 33.61 mw. The performance comparison of signed multipliers parameters are shown in table form.

6.1. Results of 8-bit Signed Multiplier

Table 2. 8-bit Signed Multiplier using EMBR Technique

Parameters	SMB-1	SMB-2	SMB-3
Power (mw)	3.16	2.88	2.97
No of LUT's	181	165	170
Delay (ns)	19.641	20.343	19.497
Memory (kb)	140392	140392	141416

According to Table 2, it is clearly observed that SMB-2 is proficient in case of power and number of elements (LUT's) than the other two schemes. The RTL schematic and Simulation results of 8-bit Signed multiplier is shown in Figure 4 and Figure 5.

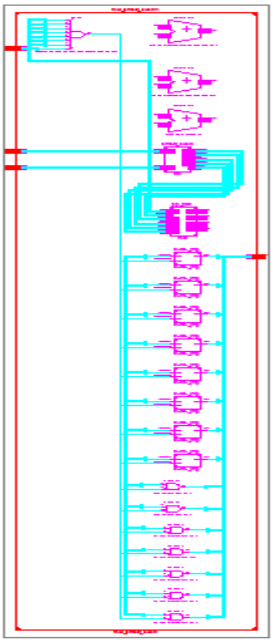

Figure 4. RTL Schematic for 8-bit Multiplier using SMB-2

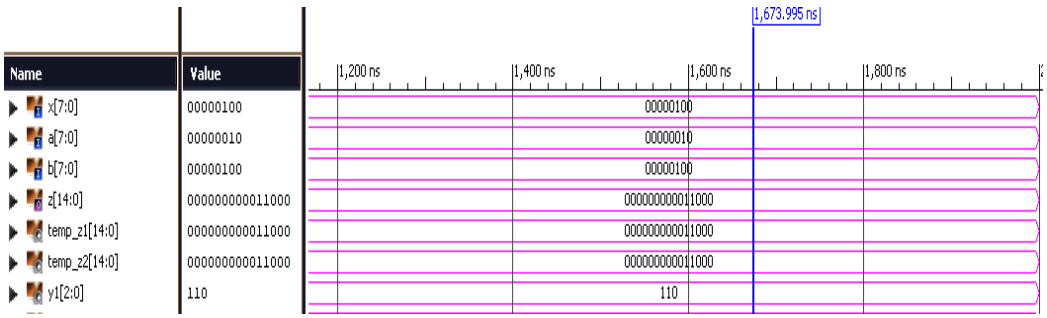

Figure 5. Simulation Results for 8-bit Multiplier using SMB-2

6.2. Results of 12-bit Signed Multiplier

Table 3. 12-bit Signed Multiplier using EMBR Technique

Parameters	SMB-1	SMB-2	SMB-3
Power(mw)	5.81	5.65	6.28
No of LUT's	332	323	358
Delay(ns)	23.154	23.154	23.556
Memory(kb)	142440	143464	143464

According to Table 3, it is clearly observed that SMB-2 is proficient in case of power and number of elements (LUT's) than the other two schemes. The RTL schematic and Simulation results of 12-bit Signed multiplier is shown in Figure 6 and Figure 7.

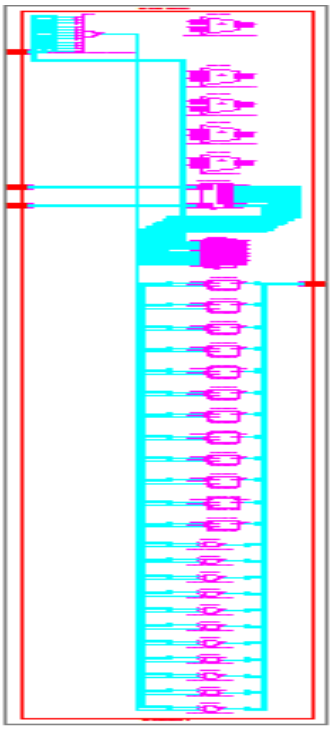

Figure 6. RTL Schematic for 12-bit Multiplier using SMB-2

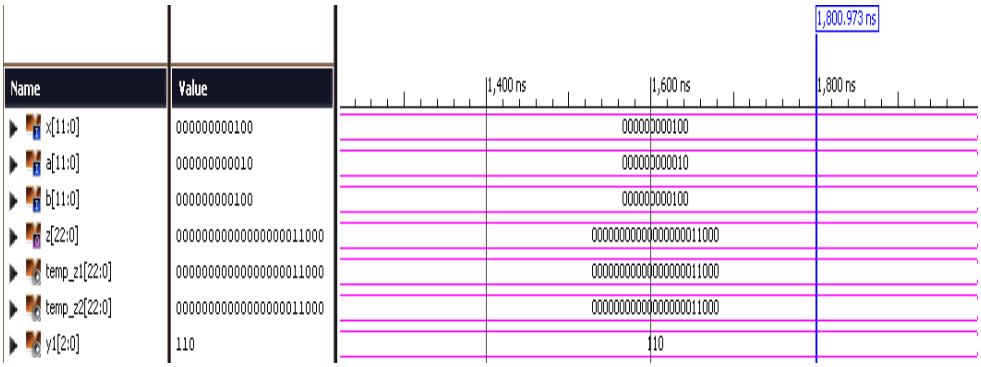

Figure 7. Simulation Results for 12-bit Multiplier using SMB-2

6.2. Results of 16-bit Signed Multiplier

Table 4. 16-bit Signed Multiplier using EMBR Technique

Parameters	SMB-1	SMB-2	SMB-3
Power(mw)	11.93	12.30	11.51
No of LUT's	682	703	658
Delay(ns)	29.535	29.549	28.056
Memory(kb)	146536	147560	148584

According to Table 4, it is clearly observed that SMB-3 is proficient in case of power and number of elements (LUT's) than the other two schemes. The RTL schematic and Simulation results of 16-bit Signed multiplier is shown in Figure 8 and Figure 9.

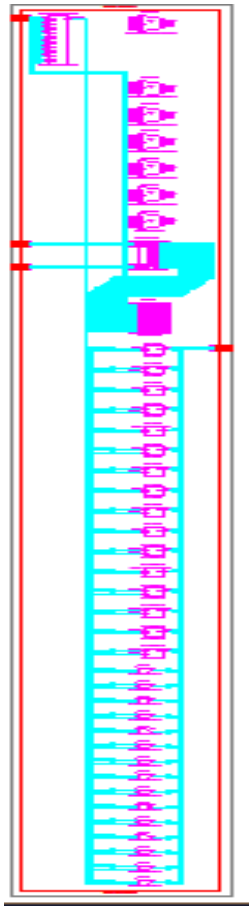

Figure 8. RTL Schematic for 16-bit multiplier using SMB-3

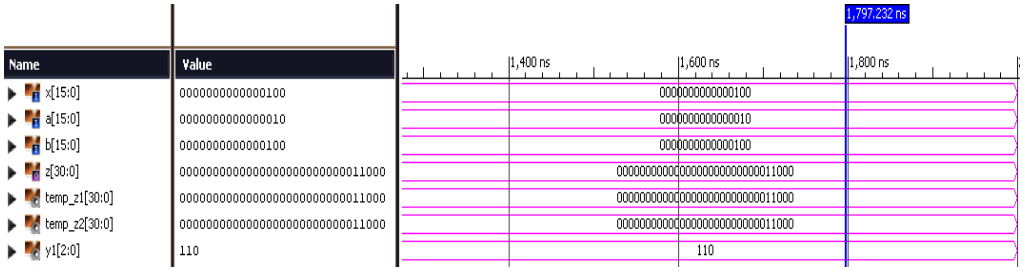

Figure 9. Simulation Results for 16-bit Multiplier using SMB-3

7. Conclusion

In this paper, design of 8 bit, 12 bit & 16-bit signed multipliers based on EMBR techniques in fused add-multiply is presented. The proposed designs are shows major improvement in terms of power consumption, number of elements and delay. From the simulation results, we are clearly concludes that signed SMB-2 will gives the better performance for both 8 bit &12 bit signed multipliers and signed SMB-3 will gives better performance in design of 16 bit signed multiplier in terms of power consumption, number of elements and delay. In future, the proposed EMBR based signed multipliers can be used in low power digital VLSI design applications like MAC, Integrated ALU and DSP's.

References

[1] K. Taoumanis, S. Xydis, C. Efstathiou, N. Moschopoulos and K. Pekmestzi, "An Optimized Modified Booth Recoder for Efficient Design of the Add-Multiply Operator", IEEE Trans. Computers and Systems-I Regular Papers, vol. 61, no. 4, **(2014)** April.
[2] Y. Liao and D. B. Roberts, "A High-Performance and Low-Power 32-bit Multiply–Accumulate Unit with Single-Instruction-Multiple-Data (SIMD) Feature", IEEE Journal of Solid-State Circuits, vol. 37, no. 7, **(2002)** July.
[3] T. T. Hoang and P. Larsson-Edefors, "A High-Speed, Energy-Efficient Two-Cycle Multiply-Accumulate (MAC) Architecture and Its Application to a Double-Throughput MAC Unit", IEEE Transactions on Circuits And Systems—I: Regular Papers, vol. 57, no. 12, **(2010)** December.
[4] A. Amaricai, M. Vladutiu, and O. Boncalo, "Design Issues and Implementations for Floating-Point Divide–Add Fused", IEEE Transactions On Circuits And Systems—Ii: Express Briefs, vol. 57, no. 4, **(2010)** April.
[5] J. Mori, *et al.*, "A 10 ns 54 54b parallel structured full array multiplier with 0.5 m units cmos technology", IEEE Journal of Solid-State Circuits, vol. 26, no. 4, **(1991)**, pp. 600-605.
[6] D. Chandel, G. Kumawat, P. Lahoty, V. V. Chandrodaya, S. Sharma, "Booth Multiplier: Ease of multiplication", International Journal of Emerging Technology and Advanced Engineering (ISSN 2250-2459, ISO 9001:2008 Certified Journal, vol. 3, Issue 3, **(2013)** March.
[7] S. K. Suman and M. S. Manna, "Implementation of Modified Booth Algorithm (Radix 4) and its Comparison with Booth Algorithm (Radix-2)", Advance in Electronic and Electric Engineering, vol. 3, **(2013)** November 6, pp. 683-690.
[8] R. Uma, V. Vijayan, M. Mohanapriya and S. Paul, "Area, Delay and Power Comparison of Adder Topologies", International Journal of VLSI design & Communication Systems (VLSICS), vol. 3, no. 1, DOI: 10.5121/VLSIC (2012) 3113 153.
[9] K. N. N. Swamy, V. J. Suman, "Design of Efficient and Fast Multiplier using MB recoding Techniques", International Journal of Emerging Research in Management and Technology, vol. 4, Issue 6, **(2015)** June.
[10] R. Zimmermann and Q. David, "Tran Design Ware, Solutions Group, Synopsys, Inc. 2025 NW Cornelius Pass Rd., Hillsboro, OR 97124, 'Optimized Synthesis of Sum-of-Products", Proceedings 37th Asilomar Conference on Signals, Systems, and Computers IEEE, **(2013)** November.
[11] M. Chaudhary and M. S. Narula, "High Speed Modified Booth's Multiplier for Signed and Unsigned Number", ITM University, Gurgaon, Haryana, (Dept. of EECE), ITM University, GurIn thisgaon, Haryana.

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