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Design and Simulation of Novel 10-T Subtraction logic for ALU design using GDI Technique

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Abstract

Design based upon CMOS logic are becoming increasingly attractive for many applications under electronic gadgets, but with increasing demand of small and portable devices, new techniques for low power are emerging. This paper focus on the design of subtarction logic for ALU sub-module in microprocessor design. Set of four different 10-T subtraction logic using Gate Diffusion Index(a new technique for low power design) has been designed using 180nm technology using Cadence Virtuoso and simulation are performed . Complete verification for performance of proposed subtraction logic is carried and circuit with least power and delay has been selected for the ALU design of the microprocessor. Layout design for the best optimum ciruit is designed using Layout XL and area of 17.28 X 11.135 μm^2 is calculated.

Index Terms*: ALU, CMOS, Delay, Full Subtractor, GDI, Low power design*

I. INTRODUCTION

Since the invention of first microprocessor in 1971, there are lots of advancement taking place in design and functionality, leading to more powerful and complex designs. VLSI engineers are working to improve the performance of existing microprocessor modules such as ALU, memory, registers, Control Unit etc. in some aspects, especially in power depletion and size. [1-4] Low power devices can be achieved by selecting new technology or logic. Technology means scaling down the size of transistor, which further help in reducing the area and power. Second term is logic, which implies reducing power and area by changing the logic while keeping the transistor size constant. GDI is one such new technique, which allows implementation of a wide range of complex logic functions using very less number of transistors. This method is suitable for design of fast, low-power circuits, using a reduced number of transistors (as compared to CMOS and existing PTL techniques), while improving logic level swing and static power characteristics and allowing simple top-down design by using small cell library [5-9].

This paper is organized as follows: basics of microprocessor design are presented in Section II. Section III contains the basic of GDI cell as essential fundamentals. Section IV contains four logic equations relevant to 1-bit full subtractor and four design of full subtractor based on the proposed XOR and XNOR gate is presented. Section V includes design of sub-modules, which helps in designing of the subtractor circuit. Section VI includes result analysis of all the four designs and calculation of delay and power analysis.

II. MICROPROCESSOR SYSTEM

Microprocessor is the heart of any intelligent device, maybe as small as a smart phone or as big as workstations. Basically microprocessor has four essential modules inside, an ALU unit, a Register unit, a Control Unit and a Program Counter and Instruction Register. Among all four units, ALU unit is the most important among all units because all the processing and decision are performed inside it. Figure 1 show the basic block diagram of

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a microprocessor.

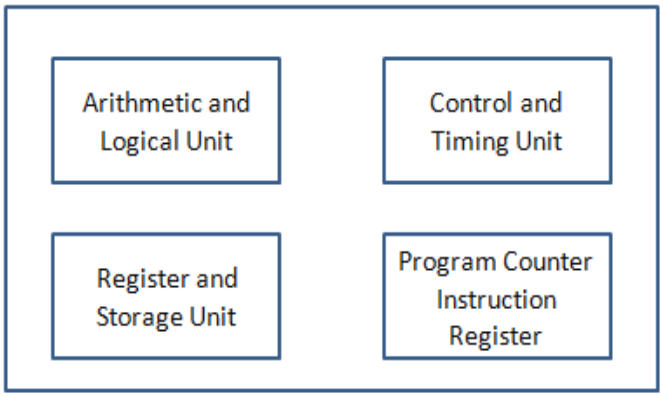

Figure 1. Basic Block Diagram of Microprocessor

The history of microprocessor can be traced back from the discovery of INTEL 4004(4-Bit Processor), and till then there are lots of enhancement with respect to speed, functionality and power consumption. Current microprocessor has multi tasking, pipelining, multi-core type features embedded inside a single processor. In order to inbuilt these entire features, VLSI engineers have to design small and energy efficient architecture so as to meet the area and power constraint of the microprocessor IC. The paper discusses the GDI technique for designing of small size and energy efficient subtractor logic for ALU unit, which can be further extended for designing of complete ALU unit, thus meeting the area and power consumption constraints.

III. BASIC GDI CELL

Basic GDI cell look similar as inverter in CMOS logic, but functionality is quite different. Figure 2 displays the basic GDI cell which clearly illustrate the Source of P-type connected to P pin(External Pin) and NMOS source connected to the N pin(external Pin). Table 1 tabulates the different function performed by basic GDI cell by just altering the various input of both external pin.

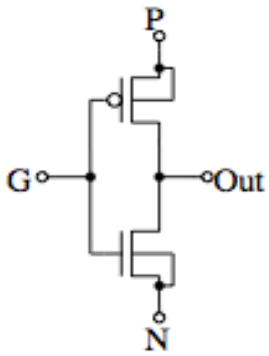

Figure 2. Basic GDI function [10]

Following are the difference compared to CMOS logic:

1. GDI techniques involve input from P (input of source/drain of pMOS), N (input of source/drain of nMOS) and G (common input).
2. Bulks of both nMOS and pMOS are connected to N or P (respectively). [11-13]

TABLE 1. GDI FUNCTION [12]

N	P	G	Out	Function
'0'	B	A	$\bar{A}.B$	F1
B	'1'	A	$\bar{A}$ +B	F2
'1'	B	A	A+B	OR
B	'0'	A	A.B	AND
Sel	B	A	$\bar{A}$. B+A(Sel)	Mux
'0'	'1'	A	$\bar{A}$	Not

IV. SUBTRACTOR LOGIC

A. Conventional CMOS full subtraction

The conventional design for full subtractor is illustrated in Figure 3, which clearly depicts the usage of seven gates and thus making it a bulky and power inefficient circuit. Equations 1 and 2 are responsible for the design of conventional subtractor circuit.

$$Diff = A - B - Cin \quad (1)$$

$$Bout = 1 \; if \; A < (B + Cin) \quad (2)$$

$$Diff = A \oplus B \oplus Bin \quad (3)$$

$$Bout = Bin.\overline{(A \oplus B)} + \bar{A}.B \quad (4)$$

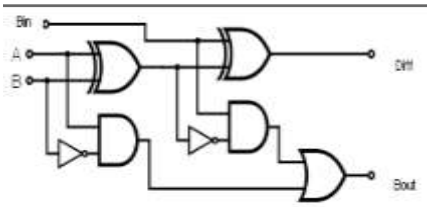

Figure 3. Conventional Full Subtarctor [4]

B. XOR/XNOR based full subtractor

Based on conventional design, new design for full subtractor was designed using XOR and XNOR gate. Figure 4(a,b) display the XOR based design, which is derived from equation 3 and 4 and it include XOR gate and multiplexer.

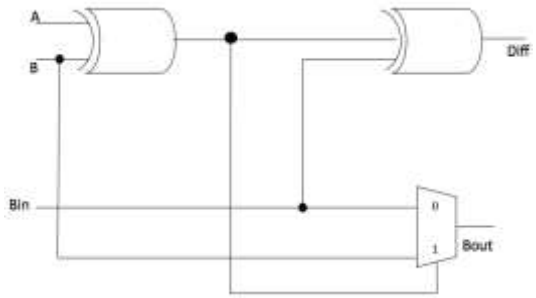

Figure 4(a). XOR based Full Subtractor-1

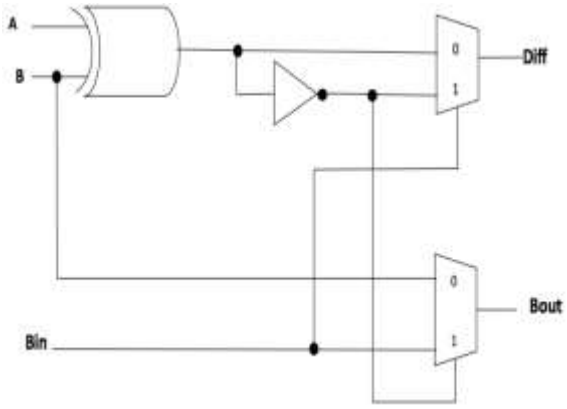

Figure 4 (b). XOR based Full Substractor-2

Based on XNOR gate, two different circuits are designed, Figure 5(a,b) display the XNOR based design, which is derived from equation 3 and 4 and it include XNOR gate and multiplexer.

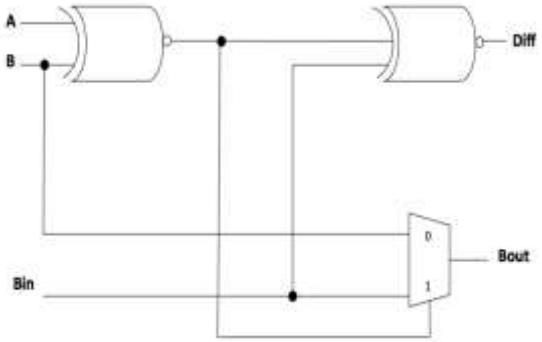

Figure 5(a). XNOR based Full Substractor-1

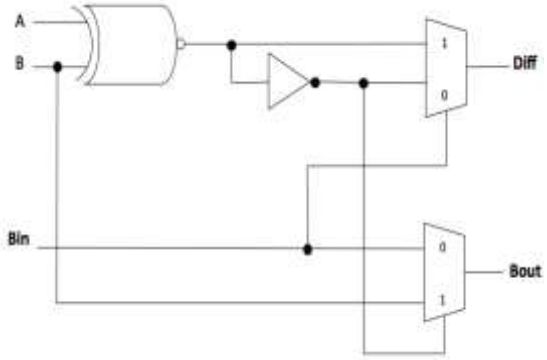

Figure 5(b). XNOR based Full Subtractor-2

V. IMPLEMENTATION OF MODULES

Designing the subtraction logic involves the designing of small modules. XOR gate and multiplexer module is designed before actual designing of subtractor logic.

A. XOR Gate

Firstly XOR gate was designed, which include four transistors instead of sixteen transistors as observed in CMOS technology. Figure 6 display the design of XOR gate using GDI technique. [15]

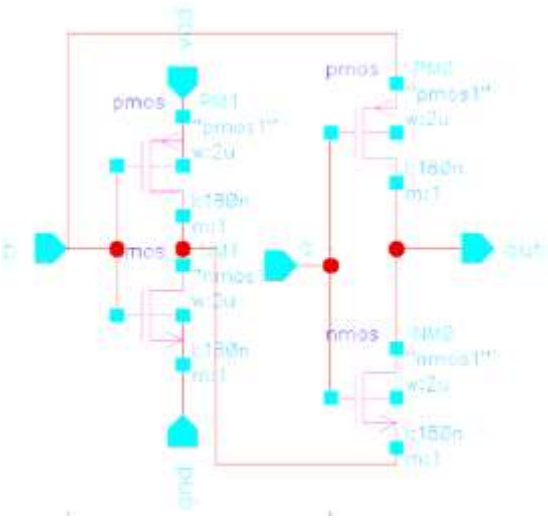

Figure 6. XOR Gate Design

B. Multiplexer

Multiplexer was designed, which require only two transistors instead of twelve transistors as observed in CMOS technology. Figure 7 display the multiplexer design using GDI technique.

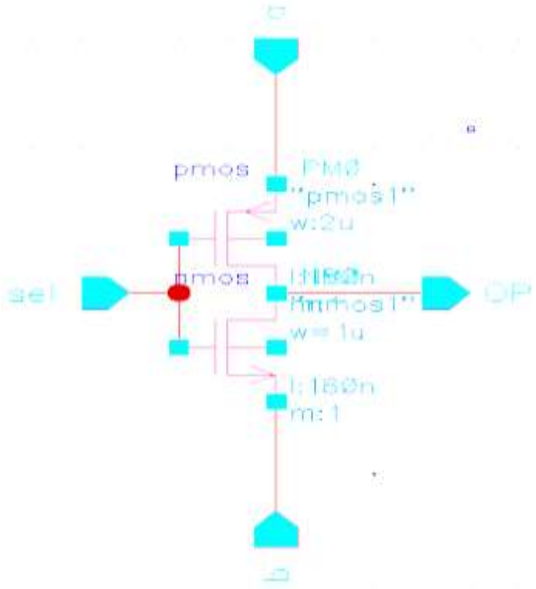

Figure 7. Multiplexer Design

VI. RESULT AND DISCUSSIONS

In order to test the performance of subtactor logic using GDI technique detailed comparison has been carried. Firstly all four types of logic had been designed using 180nm CMOS technology on Cadence Virtuoso. Simulation result of all logics is thoroughly verified and then they were compared for identifying the most power efficient design. Delay and power analysis were carried out for each and every case.

A. Simulation Results for XOR based Full Substractor

Two different XOR based subtractor design using 180nm technology is shown is Figure 8(a) and 8(c). The signal 'A', 'B' and 'Bin' acts as input for the circuit and 'Diff' and 'Bout' signal acts as output for the circuit. The simulation is carried out to verify the functionality of the circuit. Figure 8(b) and 8(d) display the output waveform for XOR based design, which clearly verify the functionality of the same.

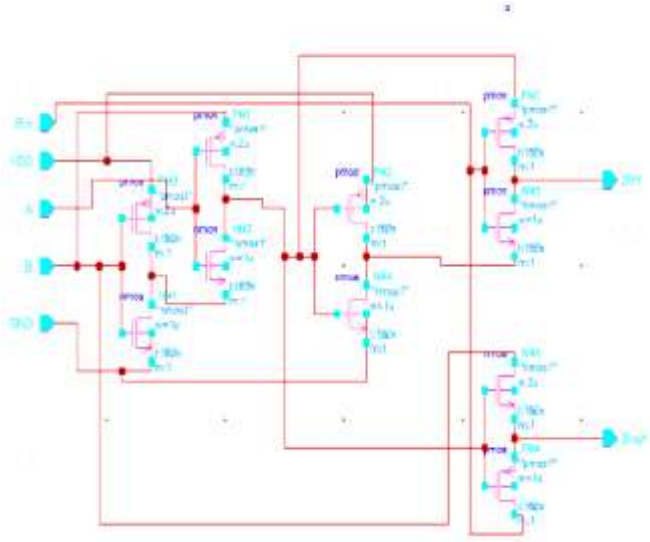

Figure 8(a). Schematic of XOR based Full Subtractor-1

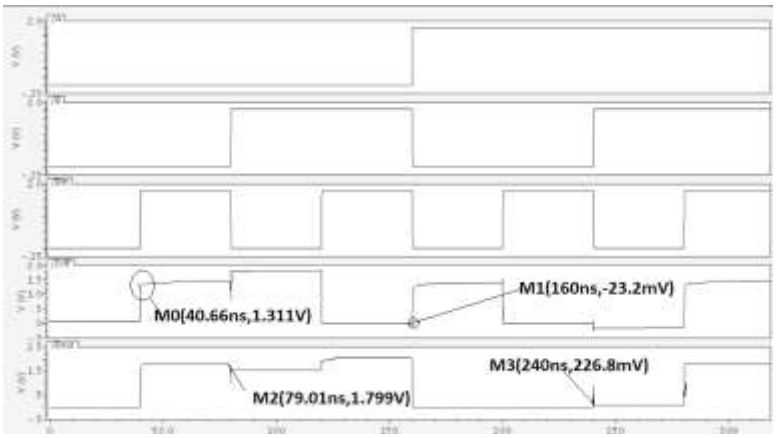

Figure 8(b), Output of XOR based Full Subtractor-1

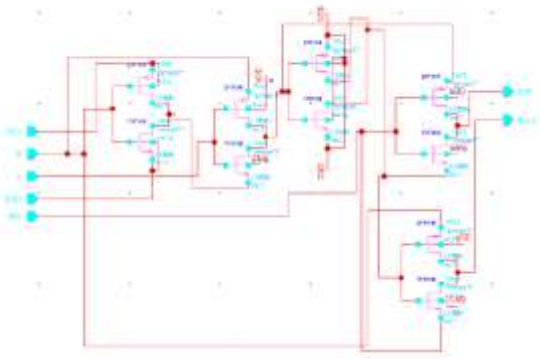

Figure 8(c). Schematic of XOR based Full Subtractor-2

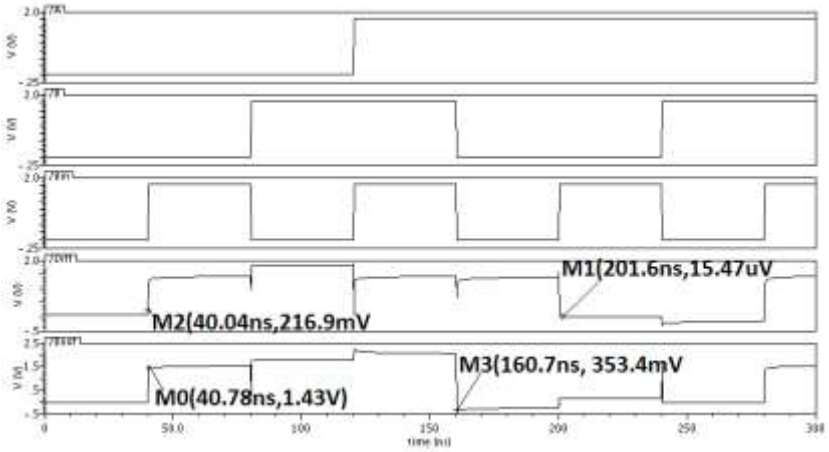

Figure 8(d). Output of XOR based Full Subtractor-2

B. Simulation Results for XNOR based Full Substractor

Two different XNOR based subtractor using 180nm technology is designed as shown is figure 9(a) and 9(c). The signal 'A', 'B' and 'Bin' acts as input for the circuit and 'Diff' and 'Bout' signal acts as output for the circuit.

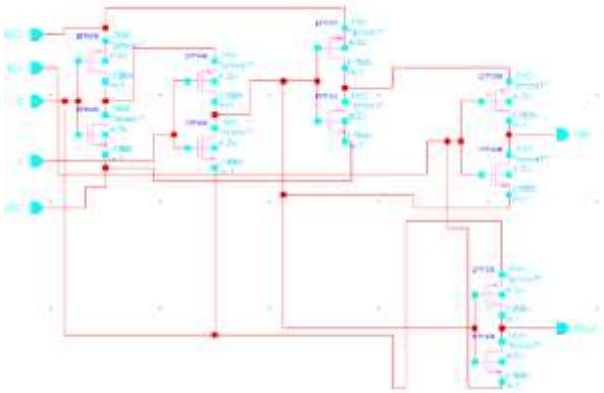

Figure 9(a). Schematic of XNOR based Full Subtractor-1

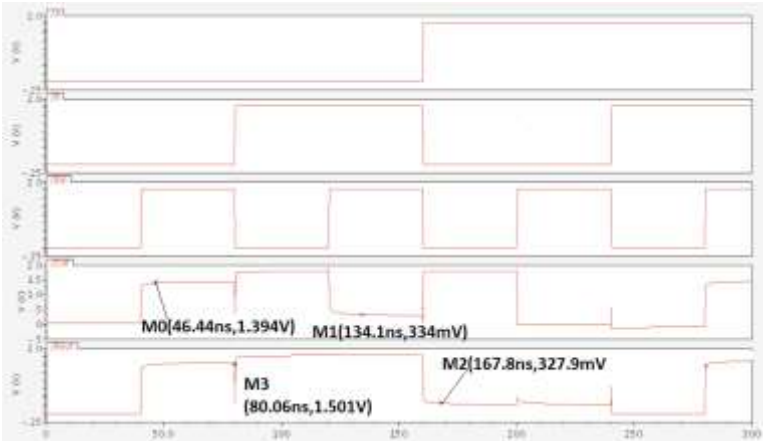

Figure 9(b). Output of XNOR based Full Subtractor-1

The simulation is carried out to verify the functionality of the circuit. Figure 9(b) and 9(d) display the output waveform for XOR based design, which clearly verify the functionality of the same.

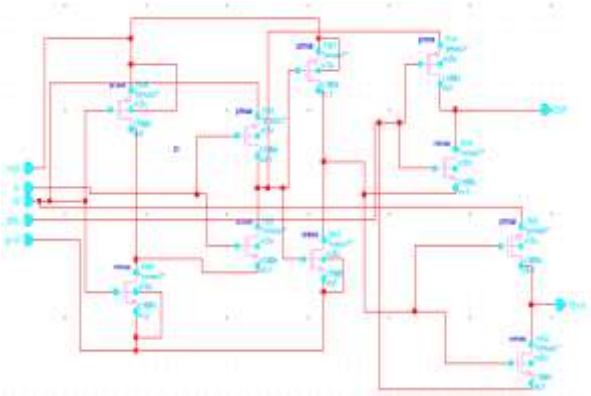

Figure 9(c). Schematic of XNOR based Full Subtractor-2

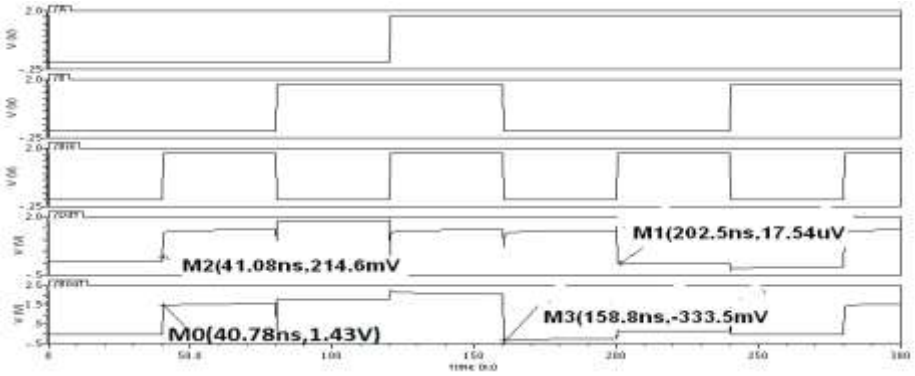

Figure 9(d). Output of XNOR based Full Subtractor-2

Power and delay analysis is carried out for comparison of all the four design. After comparison, the best design for minimum delay and minimum power is reported. The aim of this step is to meet the design according to the requirement.

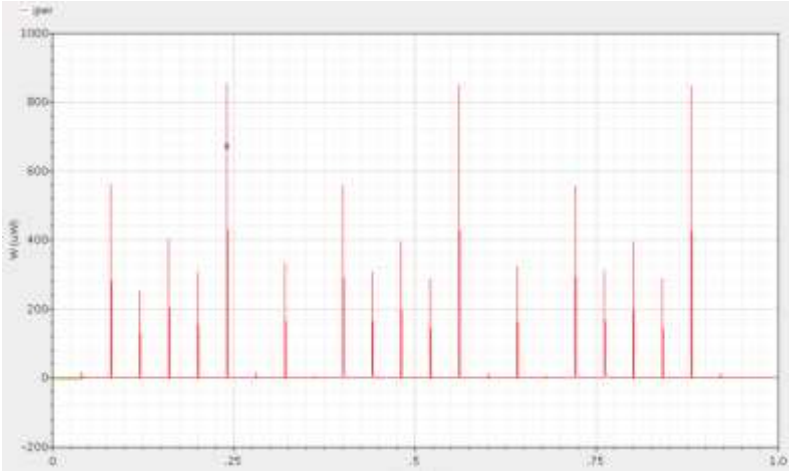

Figure 10. Power Calculation of XOR Gate based Full Subtractor-1

Figure 10 displays the power calculation for XOR gate based full subtractor-1. Power is calculated using Calculator tool in cadence virtuoso and average was calculated for the complete output.

TABLE II. DELAY ANALYSIS OF XOR BASED DESIGN

Diff	Sub XOR1	Sub XOR2
A→ Diff	40.0148 ns	40.02 ns
A→ Bout	24.9943 ps	6.214 ps
B→ Diff	21.5543 ps	29.22 ps
B→Bout	80.025 ns	10 ps
Bin→ Diff	40.0216 ns	40.03 ns
Bin→ Bout	120.025 ns	40.01 ns

TABLE III. DELAY ANALYSIS OF XNOR BASED DESIGN

Diff	Sub XNOR1	Sub XNOR2
A→ Diff	40.0142 ns	40.0118 ns
A→ Bout	11.91 ps	5.217 ps
B→ Diff	6.534 ps	11.56 ps
B→Bout	10.09 ps	19.67 ps
Bin→ Diff	40.01 ns	40.01 ns
Bin→ Bout	40.01 ns	40.01 ns

Delay option from calculator tool is used for calculating the delay between the input and output signal. Table II and III tabulates the delay analysis for XOR and XNOR gates design respectively. Table IV and V tabulates the power analysis for XOR and XNOR based design respectively.

TABLE IV. POWER ANALYSIS OF XOR BASED DESIGN

Power	XOR Based1	XOR Based2
	1.227 μW	686 nW

TABLE V. POWER ANALYSIS OF XNOR BASED DESGN

Power	XNOR Based1	XNOR Based2
	2.723 μW	965.4 nW

In concern with power analysis, XOR based substractor-2 is reported as the least power design with 686nW power. In concern with delay, XNOR based subtrator-2 is reported as the least delay design

E. Implementation

During the analysis for least power, XOR based full subtractor- 2 have been calculated as the least power circuit. In order to get the real performance, layout design for it has been designed and chip is realized. Layout XL from cadence has been used for layout design using 180nm technology. Complete layout design for XOR based subtractor-2 is displayed in Figure 11. Area calculated is 17.28 X 11.135 μm^2.

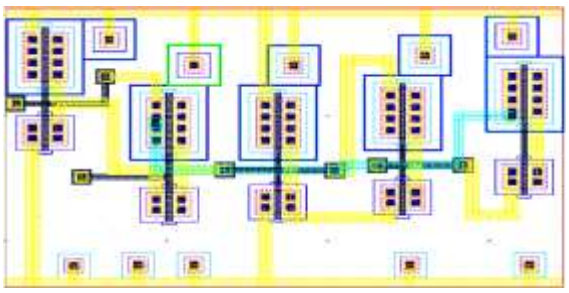

Figure 11. Layout of XOR based Subtractor-2

VII. CONCLUSION

The paper discussed the necessity of area and power constraints in electronic devices especially in microprocessor design. Subtractor logic for ALU design has been selected and four different designs have been implemented. The proposed design using XOR gate or XNOR Gate, takes the advantage of low power, lesser transistor using GDI technique. All four designs are compared for power and delay analysis. In concern with power analysis, XOR based subtractor-2 is reported as the least power design with 686nW power. In concern with delay, XNOR based subtrator-2 is reported as the least delay design. Layout design for XOR based subtarctor-2 was designed and the total area calculated is 17.28 X 11.135 μm^2.

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