

Cordic Iterations based Architecture for Low Power and High Quality DCT

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Abstract

Discrete Cosine Transform (DCT) is widely used in image and video compression standards. This paper presents low-power co-ordinate rotation digital computer (CORDIC) based reconfigurable discrete cosine transform (DCT) architecture. All the computations in DCT are not equally important in generating the frequency domain output. Considering the important difference in the DCT co-efficient the number of CORDIC iterations can be dynamically changed to reduce the power of consumption with improved image quality. The proposed CORDIC based 2D DCT architecture is simulated using Modelsim and the experimental results show that our reconfigurable DCT achieves power savings with improved image quality.

Keywords: *Coordinate rotation digital computer (CORDIC); Discrete Cosine Transform (DCT); Low power reconfigurable architecture*

1. Introduction

With the rapid growth of multimedia service running on portable applications, demands low power and high quality implementation of complex signal processing algorithm. The applications of multimedia systems involve image and video processing and it should be implemented with low cost because of limited battery lifetime. Many papers have been published on reducing power dissipation of image and video applications. Especially low power design of discrete cosine transform. DCT is a computation intensive operation in image and video compression. It is used in image and video compression standards such as JPEG [2], MPEG, H.263 [3] and H.264. For direct implementation of DCT require large number of multiple and adder in order to reduce hardware complexity. Many previous works forced about DA based DCT & multiple constant multiplications [4]. To reduce the power consumption Distributed Arithmetic (DA) is used without multiplier [5]. DCT implementation using Distributed arithmetic [DA] include several advantage such as area saving and high speed performance operations. High speed can be achieved by using conventional DA implementation by pre-computing possible values and stored it in ROM. But ROM based DA has the disadvantage of redundancy which is introduced to accommodate all possible combinations of bit pattern of input signals. A regular and simple DCT architecture can be obtained by using bit serial DA based approach. MCM based DCT can be implemented with a smaller number of shifts and add operations. Since first proposed in 1959 [7], coordinate rotation digital computer algorithm is well known and widely used iterative technique. It is used for evaluating any basic arithmetic operations, trigonometric, hyperbolic, singular value decomposition [8] and so on. Conventional CORDIC can be operations of addition and shifts; it has been used for multiplier less power DCT architecture. In order to skip the internal

CORDIC iterations, data correlations between neighboring pixels are efficiently used in low power CORDIC based DCT architecture [6]. In DCT all the computations involved in generating the frequency domain outputs are not equally important. In this some of the computations are more important for determining the output image quality while others play relatively less important roles. Thus the number of cordic iterations can be controlled by considering the importance of DCT coefficients by which considerable power savings can be achieved. In this work, present a low power and high quality DCT architecture based on CORDIC iterations, where the important difference among the DCT coefficients are efficiently exploited to achieve the power saving.

2. Related Works

Many of the multimedia applications such as video conferencing, internet, video streaming and video over wireless are most bandwidth consuming modes of communications. In order to reduce power and area low power architecture was presented in [9]. In this CSD representation for fixed point DCT coefficient and multiplier less multiplication was implemented. Although to concentrate on image quality a CORDIC based DCT [10] was presented. An algorithmic approach for low power design [11] was presented and based on trade off between image quality and power consumption, In order to concentrate on low power and high speed [12] was presented. To reduce power consumption based on sealable multiplier [13] was presented, this method used sealable multiplier and dynamically reconfiguring the width of the multiplier leads to significant power savings.

3. Cordic based DCT Architecture

A. Cordic Architecture:

The CORDIC algorithm is well known and widely studied iterative technique [15] for evaluating many arithmetic operations and trigonometric functions CORDIC algorithm can be used to evaluate not only the trigonometric functions but also transcendental functions and elementary functions like square root, division, *etc.* The basic principal of CORDIC is to iteratively rotate a vector using a rotation matrix [14] which is represented as

$$\begin{bmatrix} x_i \\ y_i \\ z_i \end{bmatrix} = \begin{bmatrix} x_{i-1} - \sigma_i 2^{1-i} y_{i-1} \\ y_{i-1} + \sigma_i 2^{1-i} x_{i-1} \\ z_{i-1} - \sigma_i \alpha_i \end{bmatrix} \quad (1)$$

where x and y are the vector co-ordinate components of x and y axes, i is the i th iteration step, σ is the sign bit that can be $+1$ or -1 represents the direction of vector rotation, z is the accumulated rotation angle and α is the predefined angle value of each micro rotation step $\alpha_i = \arctan(2^{1-i})$

The CORDIC algorithm can operates on two modes of operation. The vectoring mode of operation is used to find the amplitude and argument of a given vector, while the rotation mode is used to obtain the sine and cosine values of the given angle [16]. The hardware architecture of the CORDIC iteration is shown in Figure 1.

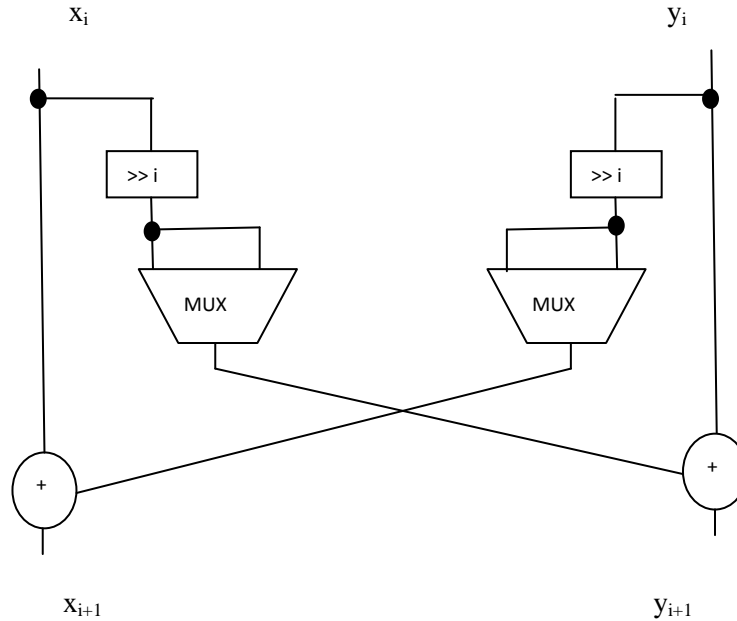


Figure 1. Hardware Architecture of CORDIC Iteration

In the CORDIC operation the magnitude of the rotated vector is scaled and accumulated after every iteration according to the following equation

$$k_i = \frac{1}{\sqrt{1 + 2^{-2(1-i)}}} \quad (2)$$

The accumulated k_i value in [2] is converged to a constant as follows.

$$k(n) = \prod_{i=1}^n k_i = \prod_{i=1}^n \frac{1}{\sqrt{1 + 2^{-2(1-i)}}} \quad (3)$$

$$\lim_{n \rightarrow \infty} k(n) \approx 0.60725 \dots$$

Where n is the number of iterations.

B. Cordic Based DCT Architecture:

DCT express a signal in terms of a sum of cosine function with different frequencies. Based on separable property 2D-DCT process is decomposed into and 1D DCT which is expressed as the following equation.

$$Z = Ty^t \quad (4)$$

Where $y = TXt$, as a result the separable 2D DCT computation can be obtained by using 1D DCT computation can be obtained by using 1-D DCT computations. The 8 x 8 1-D DCT transform is expressed as

$$X(t) = \frac{c(k)}{2} \sum_{i=0}^7 x(i) \cos \left(\frac{(2i+1)}{16} u \Pi \right)$$

Where $k = 0, 1, \dots, 7$

$$c(k) = \begin{cases} \frac{1}{\sqrt{2}} & k = 0 \\ 1 & \end{cases} \quad (5)$$

Otherwise

Where $x(i)$ is the input data and $x(t)$ is 1-D DCT transformed output data.

The 1-D DCT transform is represented as follows.

$$\begin{bmatrix} X(0) \\ X(4) \end{bmatrix} = \frac{1}{2} \begin{bmatrix} C4 & C4 \\ C4 & -C4 \end{bmatrix} \begin{bmatrix} x(0) + x(7) + x(3) + x(4) \\ x(1) + x(6) + x(2) + x(5) \end{bmatrix}$$

$$\begin{bmatrix} X(2) \\ X(6) \end{bmatrix} = \frac{1}{2} \begin{bmatrix} C2 & C6 \\ C6 & -C2 \end{bmatrix} \begin{bmatrix} x(0) + x(7) - x(3) - x(4) \\ x(1) + x(6) - x(2) - x(5) \end{bmatrix}$$

$$\begin{bmatrix} X(1) \\ X(3) \\ X(5) \\ X(7) \end{bmatrix} = \frac{1}{2} \begin{bmatrix} C1 & C3 & C5 & C7 \\ C3 & -C7 & -C1 & -C5 \\ C5 & -C1 & C7 & C3 \\ C7 & -C5 & C3 & -C1 \end{bmatrix} \begin{bmatrix} x(0) - x(7) \\ x(1) - x(6) \\ x(2) - x(5) \\ x(3) - x(4) \end{bmatrix} \quad (6)$$

Where $ck = \cos(k\pi/16)$. The cosine elements in (6) can be changed into sine elements through trigonometric symmetric property, and (6) can be rearranged as the following equations:

$$\begin{bmatrix} X(4) \\ X(0) \end{bmatrix} = \frac{1}{2} \begin{bmatrix} C4 & -S4 \\ S4 & C4 \end{bmatrix} \begin{bmatrix} x(0) + x(7) + x(3) + x(4) \\ x(1) + x(6) + x(2) + x(5) \end{bmatrix}$$

$$\begin{bmatrix} X(3) \\ X(5) \end{bmatrix} = \frac{1}{2} \begin{bmatrix} C3 & -S3 \\ -S3 & C3 \end{bmatrix} \begin{bmatrix} x(0) - x(7) \\ x(3) - x(4) \end{bmatrix}$$

$$\begin{bmatrix} X(1) \\ X(7) \end{bmatrix} = \frac{1}{2} \begin{bmatrix} C7 & S7 \\ -S7 & C7 \end{bmatrix} \begin{bmatrix} x(3) - x(4) \\ x(0) - x(7) \end{bmatrix} + \frac{1}{2} \begin{bmatrix} C1 & S1 \\ -S1 & C1 \end{bmatrix} \begin{bmatrix} x(2) - x(5) \\ x(1) - x(6) \end{bmatrix}$$

$$\begin{bmatrix} X(6) \\ X(2) \end{bmatrix} = \frac{1}{2} \begin{bmatrix} C6 & -S6 \\ S6 & -C6 \end{bmatrix} \begin{bmatrix} x(0) + x(7) - x(3) - x(4) \\ x(1) + x(6) - x(2) - x(5) \end{bmatrix} + \frac{1}{2} \begin{bmatrix} C3 & S3 \\ -S3 & C3 \end{bmatrix} \begin{bmatrix} x(1) - x(6) \\ x(2) - x(5) \end{bmatrix} \quad (7)$$

Where $s_m = \sin(m\pi/16) = ck$, and $m=8-k$. The rearranged 1-D DCT equation is now represented as vector rotation matrix together with the consecutive CORDIC iterations as shown in Figure 2.

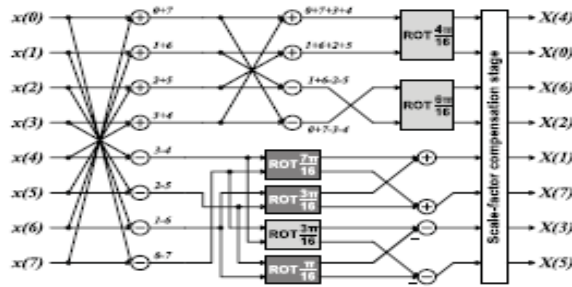


Figure 2. Hardware Architecture of CORDIC based 1-D DCT

After 2-D DCT operation, the input data in space domain is transformed to the frequency domain which is the 8 x 8 block of 64 DCT co-efficient shown in Figure 3.

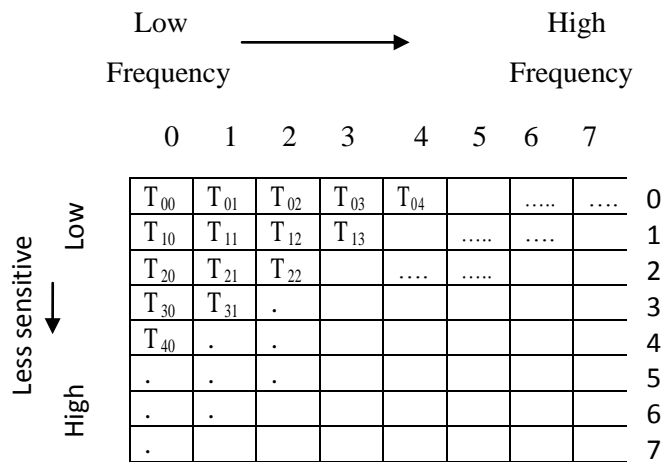


Figure 3. Sensitivity Difference of 8 x 8 2-D DCT co-efficient

Based on signal compaction property of DCT, the lower frequency components has more signal energy of the output data compared to that of high frequency components. After the quantization [17], the high frequency DCT co-efficient becomes even smaller, this means that the lower frequency components are more sensitive to human eyes than high frequency components. Based on that fact the low frequency DCT co-efficient are more important compared to that of high frequency components. CORDIC based DCT architecture is designed considering the important difference between DCT coefficients. A large number of CORDIC iterations are assigned to generate the low frequency DCT coefficients of iterations are used for the high frequency components

4. Proposed Low Power Cordic based DCT

In the proposed low power CORDIC based DCT architecture, to generate DCT co-efficient a different number of iterations are assigned and the number of iterations should be carefully selected in order to get the minimum error between the desired input angle and corresponding accumulated angle Table 1 shows the required iterations and vector rotation direction σ (sign bits).

Table 1. Required Iterations and Directions for Vector Rotation

Angle	Required Iterations	Directions (Sign-Bits)
$\pi/16^+$	i=0,1,3,10	$\sigma = -1,+1,+1,+1$
$3\pi/16^+$	i=1,3,10	$\sigma = -1,-1,-1$
$3\pi/16^*$	i=1,3,10	$\sigma = -1,+1,+1$
$4\pi/16^*$	i=0	$\sigma = +1$
$6\pi/16^*$	i=(90 ^o),2,3,5,7	$\sigma = -1,+1,+1,+1, -1$
$7\pi/16^+$	i=0,1,3,10	$\sigma = -1,-1,-1,-1$

For example, to rotate the vector by $7\pi/16$, only the i^{th} iterations (i=0, 1, 3, 10) are executed and for power savings the rest of the iterations can be skipped. The look ahead algorithm for $7\pi/16$ cordic rotator can be written as follows.

$$\begin{bmatrix} x \\ y \end{bmatrix} = \begin{bmatrix} 1 & \sigma_{10} 2^{-10} \\ \sigma_{10} 2^{-10} & 1 \end{bmatrix} \begin{bmatrix} 1 & \sigma_3 2^{-3} \\ \sigma_3 2^{-3} & 1 \end{bmatrix} \begin{bmatrix} x_0 \\ y_0 \end{bmatrix} \quad (8)$$

where $\sigma_0 = -1, \sigma_1 = -1, \sigma_3 = -1, \sigma_{10} = -1$. In Table 1 i = 900 represent the optional first iteration of the CORDIC [14]. The numbers of iterations for our DCT architecture are carefully selected such that the error between the desired angle and the corresponding accumulated angle does not exceed 0.004 for all the given angles

Table 2. CORDIC Scale Factor and their Approximation Values

Angle	Desired Scale-Factor	Approximation Value
$\pi/16$	0.3137856.....	$2^{-2} + 2^{-4} + 2^{-10}$
$3\pi/16$	0.4437599.....	$2^{-1} - 2^{-4} + 2^{-7} - 2^{-9}$
$4\pi/16$	0.3535533.....	$2^{-2} + 2^{-4} + 2^{-5} + 2^{-7} + 2^{-9}$
$6\pi/16$	0.4810759.....	$2^{-1} - 2^{-6} - 2^{-8}$
$7\pi/16$	0.3137856.....	$2^{-2} + 2^{-4} + 2^{-10}$

The scale factor is decided according to the number of the executed CORDIC iterations. As the number of iterations is known ahead, the scale factors are pre determined. Which are shown in Table 2. One interesting observation is that the look ahead CORDIC using less number of iterations has the similar effect when the high shift terms is removing from the look ahead CORDIC. For example, if the CORDIC rotation with $7\pi/16$ is executed using three iterations (i=0, 1, 3) the look ahead CORDIC algorithm and its corresponding scale factor are as follows.

$$x = (1-2^{-1}-2^{-3}-2^{-4}) x_0 + (1+2^{-1}+2^{-3}-2^{-4}) y_0 \quad (9)$$

$$y = (-1-2^{-1}-2^{-3}+2^{-4}) x_0 + (1-2^{-1}-2^{-3}-2^{-4}) y_0 \quad (10)$$

$$k_{7\pi/16} = 0.3137856$$

In (8) when the higher shift terms (smaller than 2^{-10} terms) are eliminated, the equation is changed to (9) & (10).

5. Reconfigurable Cordic based DCT Architecture

As mentioned in the last part, the high shift term of the look ahead CORDIC can be carefully removed which has the same effect with the less number of CORDIC iterations. The less number of CORDIC iterations means the CORDIC with low computational complexity. To further reduce the power consumption, we propose a reconfigurable CORDIC based DCT architecture. In this section several nodes are presented and the proposal reconfigurable architecture can dynamically change the CORDIC iterations. Generally in the look ahead CORDIC, the shift terms for calculating low frequency DCT coefficients *i.e.*, terms for calculating $X(0)$, $X(1)$ in [7] are more important than the shift terms for calculating high frequency co-efficient. In look ahead CORDIC equation low shift terms are more important whereas the high shift terms are less important. To save the computation power, the least important shift term $X(7)$ is removed. To calculate $X(3)$ component both the CORDIC rotators of $3\pi/16$ and $\pi/16$ are needed and those are expressed as the following look ahead CORDIC equation in the normal mode.

$$X_{7\pi/16^*} = (1-2^{-1}-2^{-3}+2^{-4}-2^{-10}) x_0 + (1+2^{-1}+2^{-3}-2^{-4}-2^{-10}) y_0 \quad (11)$$

$$X_{\pi/16^+} = (1+2^{-1}+2^{-3}-2^{-4}+2^{-10}) x_0 + (1-2^{-1}-2^{-3}-2^{-4}-2^{-10}) y_0 \quad (12)$$

The scale factor in normal mode

$$k_{3\pi/16^*} = 2^{-1} - 2^{-4} \quad (13)$$

$$k_{\pi/16^+} = 2^{-1} + 2^{-4} \quad (14)$$

For mode 1, $3\pi/16$ CORDIC rotator is reduced as follows.

$$X'_{3\pi/16} = (1-2^{-1}-2^{-3}-2^{-4}) x_0 + (1+2^{-1}+2^{-3}-2^{-4}) y_0 \quad (15)$$

As it goes to the higher level the number of shift terms are further reduced.

6. Experimental Results of the Proposed Low Power Cordic based DCT Architecture

In this section, the experimental results of the proposed CORDIC based DCT architecture are presented. In this, the number of CORDIC iterations is selected according to the target angle. The power consumption for DCT architecture is measured with 50 MHz clock cycles, 2.5 V supply voltage. The power value for three different modes is calculated. Because some of the higher order shift terms in CORDIC iterations can be removed considering the important difference of DCT co efficient, our proposed DCT architecture shows the lowest gate count and power consumption with improved image quality.

The component requirement for our DCT architecture for various modes is given in Table 3. In this the amount of adder, subtractor, and multiplier required for three different modes of DCT architecture is given.

Table 3. Component Requirement for Various Mode

Gate count	Normal Mode	Mode 1	Mode 2
Adder	232	176	112
Sub tractor	296	264	128
Multiplier	96	96	96

The power consumption for our DT architecture at different modes is shown in Table 4. The power consumption is measured with 50 MHz clock cycles, 2.5V supply voltage.

Table 4. Power Consumption at Different Modes

Power consumption	Normal mode	Mode 1	Mode 2
Power(mw)	0.186	0.185	0.184

7. Conclusion

CORDIC is a powerful algorithm and a popular algorithm of choice when it comes to various digital signal processing applications. In DCT architecture, all the computation are not equally important in generating the frequency domain outputs. This paper presented a low power CORDIC based DCT architecture, where the important difference in DCT co-efficient are efficiently exploited to allocate the number of CORDIC iterations. The reconfigurable CORDIC based DCT architecture can dynamically change the modes with power savings and improve image quality. The device utilization summary showed that minimum resources were consumed. This idea can assist the low power design of image and video compression applications.

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