International Journal of Hybrid Information Technology
Vol.7, No.3 (2014), pp.325-336
http://dx.doi.org/10.14257/ijhit.2014.7.3.30

Analysis of Low Frequency Drain Current Model for Silicon Nanowire Gate-All-Around Field Effect Transistor

Awanit Sharma

Department of Electronics, Jiwaji University, Gwalior, India
awanitsharma@gmail.com

Abstract

This paper is investigated the low frequency noise behavior in subthreshold regime of gate-all-around silicon nanowire field effect transistors. Downscaling of multi gate structure beyond 50 nm gate length describes the quantum confinement related model. A drain current model has been described for output characteristics of silicon nanowire FET that is incorporated with velocity saturation effects and compact modeling of RF noise behavior is analyzed for gate-all-around structure. Noise performance of gate-all-around transistor is investigated at high frequency band for radio frequency RF specified application and consequently low frequency noise behavior can be analyzed using drain current model. This paper shows that noise is decreasing with frequency. Higher subthreshold, lower drain induced barrier lowering DIBL, higher on-off ratio and higher noise figure at lower frequency is achieved by gate all around configuration and comparison has been done with double gate structure.

Keywords: *Gate-all-around (GAA); Double gate; Silicon nanowire; Drain current model; Flicker noise; Noise figure; Equivalent noise resistance; Subthreshold; DIBL*

1. Introduction

The continuous scaling of Gate-All-Around silicon nanowire field effect transistor FET as compared with single gate and double gate FET shows better short channel control over other structures [1]. GAA silicon nanowire FET is most promising candidate for future CMOS based electronic systems due to their gate controllability, low leakage, high on-off ration and enhanced carrier transport property. Analytical models of GAA fet for parameter extraction of devices is described in [2] , most of these models and SCE models describe the effectiveness of ideal GAA structure with quadruple cross section were reported in this paper . [3] Gate-all-around (GAA) Nanowire FET have been fabricated by top-down and bottom-up design [3], [4].Gate-All-Around (GAA) nanowire Field effect transistor has researched excellent electrostatic control over the channel surrounded by conducting gate and provides higher transconductance [5].Gate all-around (GAA) MOSFETs have captivated considerable observation as compared with double-gate and tri-gate [6], [7].Simulation and analysis shows that gate-all-around GAA configuration provides excellent performance owing to considerable effect of short channel as compared with other structures [8]..DIBL suppression, and excellent subthreshold slope is advantage of GAA devices. Downscaling of channel length to 45 nm of MOSFET is restricting factor of static power consumption due to increase leakage in off state [9].In this paper performance analysis of GAA nanowire CMOS configuration is estimated and described [10]- [12]. High noise values in the subthreshold are the concerned factor that

ISSN: 1738-9968 IJHIT

affects the normal behavior of switching and circuit performance of silicon nanowire FET. Silicon nanowire have also been used as biochemical sensors [13]–[15].

This paper is divided into 4 sections. Section 2 describes the GAA silicon nanowire description and corresponding current model. Section 3 shows the result and analysis about noise of GAA configuration. Section 4 provides the concluded part of whole paper.

2. GAA Nanowire FET Design Concept And Simulation

Figure 1(a) describes the general schematic of GAA silicon nanowire fet and figure 1(b) shows its cross sectional view and gate surrounded from all sides provide better electrostatic control over double gate fet.

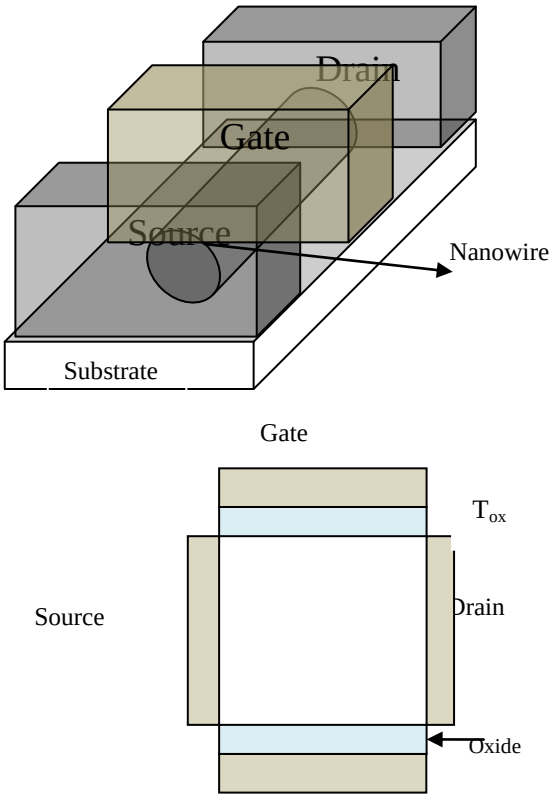

Figure 1 (a). Basic Schematic of GAA Silicon Nanowire fet and 1(b). Cross Sectional view of GAA

2.1. Drain Current Model

2.1.1. Poisson Equation

Schrödinger equation can be described in channel region is defined as follows.

$$\frac{d^2\varphi}{dx^2} + k_1^2\varphi = 0 \qquad \text{for } x < 0 \tag{1}$$

$$\frac{d^2\varphi}{dx^2} + k_2^2\varphi = 0 \qquad \text{for } 0 \le x \le d \tag{2}$$

$$\frac{d^2\varphi}{dx^2} + k_3^2\varphi = 0 \qquad \text{for } x \ge d \tag{3}$$

Where

$$k_1{}^2 = k_3{}^2 = \frac{2m}{\hbar^2} \tag{4}$$

$K_2{}^2 = n_b^2 k_1^2$ and

$$n_b^2 = \frac{(E - E_b)}{d} \tag{5}$$

solution of the Schrödinger equation tunneling probability is given by expression

$$D(E) = e^{\frac{-2[2m(E_b - E)]^{1/2}d}{\hbar}} \tag{6}$$

2.1.2. Drain current

GAA silicon nanowire having short channel therefore quasi-ballistic behavior is still applicable to the nanowire fet so velocity overshoot is expected which has been described by [16]. Average charge carrier's energy is estimated by mobility function that is a function of the temperature therefore electron mobility describes with simple and normal energy-balance process. Drain current transport model at room temperature which has been previously described and it has been applied to double gate MOSFETs is still applicable to GAA silicon nanowire fet [17], Drain current can be described in linear channel saturation region which is shown by given equation.

$$I_{DS} = \frac{W\int_0^{V_{Dsat}} \mu_n Q(v)dV}{\int_0^L \left(1 + \left(\frac{2k\mu_n}{q\lambda_w V_{sat}}\right)(T_e(x) - T_0)\right)dx} \tag{7}$$

where Le is the channel length of the GAA fet, μ_n is the electron mobility and it depend on voltage applied across gate, k is the Boltzmann constant and it value is fixed, Te is the temperature of electron charge and the energy-relaxation length is defined as $\lambda_w$which one is depended on relaxation time , τw and Vsat is the velocity that being saturated. Here W is the width of GAA FET and it depend on fingers numbers in the structure.

To evaluate charge density of GAA structure it must be integrate from charge at source end that is QS and charge at drain end that is Qd and this is shown below in given equation [18]

$$f(V_{GS,}, V_{DSS}) = \int_0^{V_{Dsat}} \mu_{n0} Q(v)dV \tag{8}$$

$$I_{DS} = \frac{2\pi R}{L}\mu\left[2\frac{KT}{q}(Q_s - Q_d) + \frac{(Q_s^2 - Q_d^2)}{2C_{OX}} + \frac{KT}{q}Q_0 \log\left[\frac{Q_d + Q_0}{Q_d - Q_0}\right]\right] \tag{9}$$

$$Q_0 = 4\left(\frac{KTC_{OX}}{q}\right) \tag{10}$$

The ultra-thin film mobility is not sensitive to the silicon thickness tsi and it is higher than heavily doped bulk MOSFET devices at inversion densities that is large value in case of floating body structure. Lower effective electric field is occurred ,but at lower inversion densities the mobility is reduced with reduction of tsi [19]. Quantum well is developed between oxide layers which is formed by thin silicon layer .Quantum well is reduced and this reduction in the mobility is observed due to the scattering occur by surface roughness. Previously described method for double gate MOSFET .We suggest using the method given by [20]-[21], originally proposed for DG MOSFET devices. The effective mobility reduces with the effective vertical field Eeff is given by [20]

$$E_{0eff} = \frac{Q}{4\varepsilon_{si}}V \tag{11}$$

$$\mu_n(t_{si}, E_{eff}) = \frac{\mu_0}{1+\frac{\mu_0}{\mu_{ph(bulk)}}\left(\frac{\mu_{ph(bulk)}}{\mu_{ph(t_{si},E_{eff})}}-1\right)+\theta\frac{\mu_0}{\mu_{sr}}} \tag{12}$$

Where μ_0 and θ are the parameters that depend on structure formation.

Schrödinger-Poisson equation is generally described the 2d charge density model therefore this drain current model which is operated at the lower sub-band can be described by the same poisson equation. This drain current model still applicable for GAA structure as silmilar for double gate configuration because of shape eigenfunction is almost similar to double gate. Drain current model can be described effectively by electron temperature profiling process.

$$\frac{dT_e}{dx} + \frac{T_e - T_0}{\lambda_w} = -\frac{q}{2k}E_X(x) \tag{13}$$

Equation 7 can be defined under boundary value condition for Te=T0 at room temperature and electric field is described as function of channel potential vary with the x. Field is found to be linear at the source to drain end therefore drain to source current can be described as given by

$$I_{DS} = \frac{Wf(V_{GS,}V_{DSS})}{L_e+\frac{q\alpha}{2k}\int_0^L V(\xi)e^{\frac{\xi-L_e}{\lambda_w}}d\xi} = \frac{W}{L_e}\frac{f(V_{GS,}V_{DSS})}{1+\gamma_n V_{DSS}} \tag{14}$$

Where

$$\gamma_n = \frac{\mu_{eff}}{v_{sat}L_e}\frac{1}{(1+2\lambda_w/L_e)} \tag{15}$$

V_{DSS} become equal to non saturated channels V_{DS} and become similarly equal to saturated channel V_{DSS} =V_{DSSAT}

$$V_{DSS} = V_{DS} - \frac{kT\ln\left[1+\exp\left[A(V_{DS}-V_{Dsat})/kT/q\right]\right]}{qA} \tag{16}$$

Where A is the control parameter for transition between saturated and non saturated channel. The current which has been described before at saturated channel region therefore V_{Dsat} can be described by current that is shown below [22]-[23].

$$I_{DS} = WQ(V_{Dsat})v_{sat,ns} \tag{17}$$

And Overshoot velocity can be evaluated and described by given equation below

$$V_{sat,ns} = \frac{\mu_{eff}}{1+\alpha(T(L)-T_0)} E_x \quad (18)$$

Where α is described as

$$\alpha = \frac{2k\mu_n}{q\lambda_w V_{sat}} \quad (19)$$

Channel length saturation must be found for device operated in saturation region of the device due to the channel length modulation which become an important factor and this effect is shown below

$$\Delta L = L - L_e = L_c \operatorname{arc\,sin\,h}\left(\frac{V_{DS}-V_{Dsat}}{E_{sat}L_c}\right) \quad (20)$$

Where L_C is proportionally depended on λ_c and this is given by equation as shown below [24].

$$\lambda_c = \sqrt{\left(\frac{\varepsilon_{si} t_{ox} R}{\varepsilon_{ox}} + \frac{R^2}{2}\right)} \quad (21)$$

3. Results and Analysis

3.1. Subthreshold Regime

GAA nanowire thus operated in accumulation mode FET generally p-transistors. V_T threshold voltage observed before FET enter into accumulation mode. Voltage supply VDD of 1 V is applied that improve threshold voltage and a better response of drain current ($I_{D)}$ versus gate to source voltage (V_{GS}) I_D–V_{GS} is obtained as given in figure 2 .Large p-FET on drive current is observed that is higher than n-FET is achieved due to high mobility of carriers in respect of two lateral gates orientation. Figure 2 shows transfer graph of ID-VGS for n-FET . Asymmetry is reported in p-FET and n-FET configuration and pull-down logic is observed due to similar channel length of wire 45 nm [9].For V_{DS} = 1.2 V,V_T threshold voltage for p-MOS and n-MOS are -0.2 and 0.3 V. Similarly for V_{DS} = 0.6 V, V_T are 0.3 and 0.49 V.

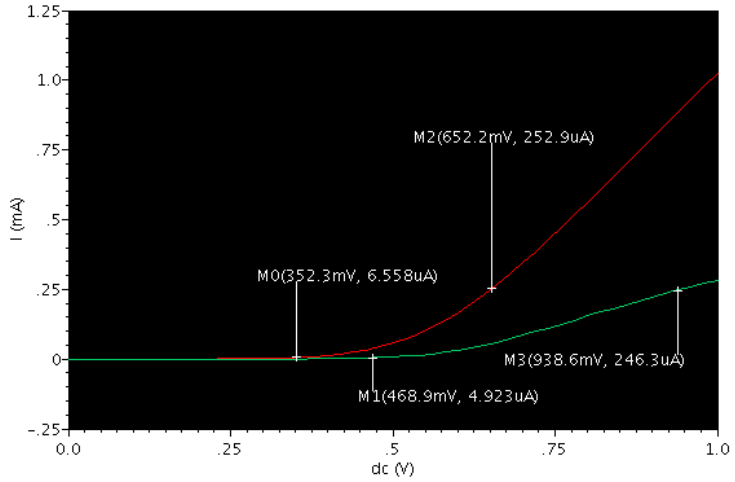

Figure 2. n-FET characteristics curve I_{DS} versus V_{GS} with V_{DS} = 1 V and 0.1 V

Figure 3 shows different output characteristics curve.I_D versus V_{DS} curve shows high drive current 23.26mA (PMOS) and 0.18 mA (NMOS) for gate-source voltage(V_{GS} = 1 V).

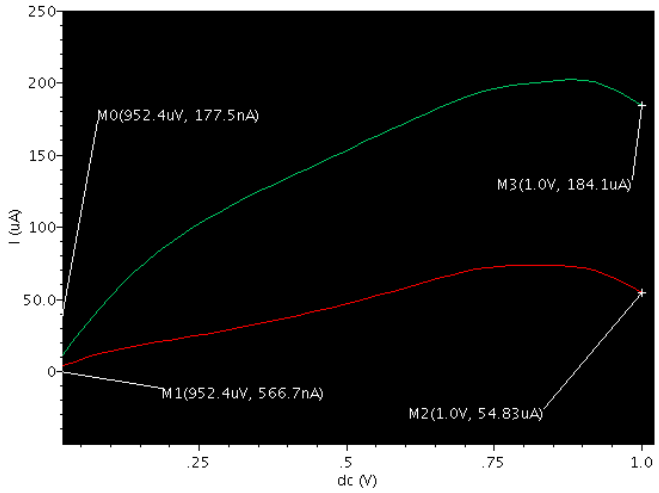

Figure 3 . n-FET I_D-V_{DS} curve for V_{GS} = 1 V and V_{GS} = 0.6 V

Channel current is generally described by Fermi and silicon body potential.

$$I_{DS} = W\mu Q(x)\frac{(d\varphi_F(x))}{dx} \quad (22)$$

Channel length of 45 nm for both p-FET and n-FET is fixed. Leakage current minimization occurs due to volume inversion of surrounding gate [13].As substrate is used as back gate for gate-all-around structure that made to be grounded then there some asymmetry observed in the output characteristics. Current intensity is low in the direction of forward bias of drain.I_D saturation current is observed 5.7mA for V_{GS} = 1 V. Figure 4 show the output characteristics of the 45 nm gate-all-around FET.A good and better agreement can be seen between different and simulated model. Simulated model

provides the high on-drive current capability and low off leakage without the effect of velocity overshoot and quantum effects. Good subthrehold and lower DIBL is achieved with simulated model. We have bipolar behavior in weak inversion shows that it is good model.

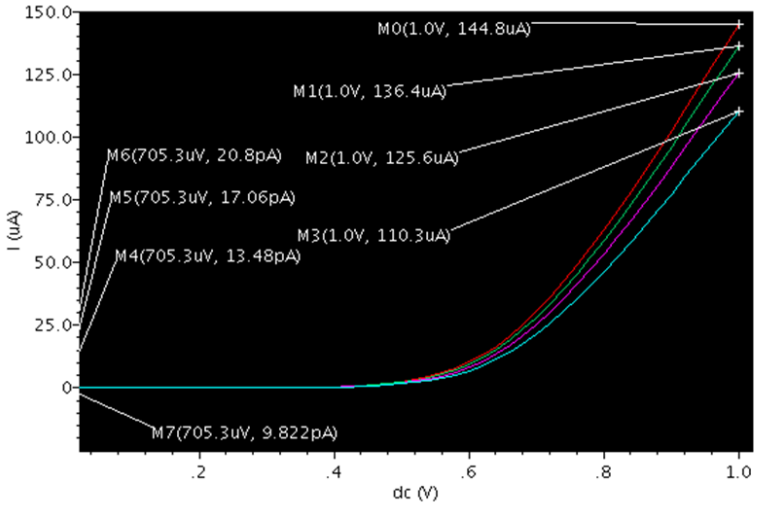

Figure 4. Different Current Models as Compared with Simulated Model

3.2. Low Frequency Noise Simulation

Noise is the considerable factor when GAA silicon nanowire fet has scope in application like RF, low noise amplifier, mixer therefore analysis of noise at high frequency is just required for high performance and high reliability of device associated with GAA structure. The gate , Source and drain resistance provide thermal noise which can be calculated by given equation. Channel resistance contribute channel induced noise and gate resistance , oxide gate capacitance contribute to gate induced noise. Thermal noise is the most dominant factor of noise analysis that is generated by the resistor connected at output load. The RF input voltage source can be the noise source which is shown below.Figure 5 shows the equivalent noise resistance for GAA silicon nanowire fet in band of 1GHz-10GHz .The equivalent noise resistance R_N become higher at low frequencies and then continuously decreases with increase in frequency. Equivalent resistance value of 2.168×1036 ohm is measured at low frequency due to flicker noise associated with channel.

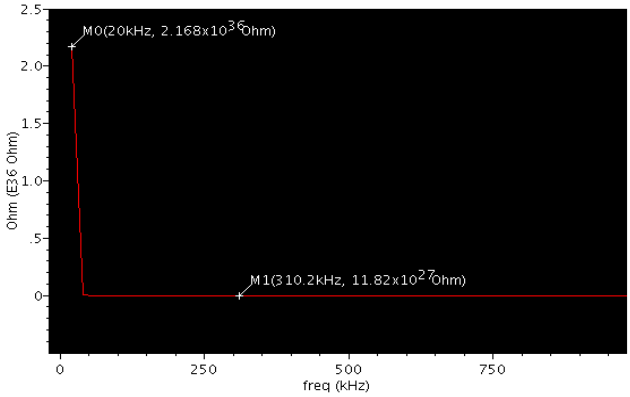

Figure 5. Equivalent noise resistance of GAA nanowire structure

Figure 6 shows noise figure is higher at lower frequency and decreases with increasing frequency. This occurs due to flicker noise contribution at low frequency and gate induced noise at higher frequency.

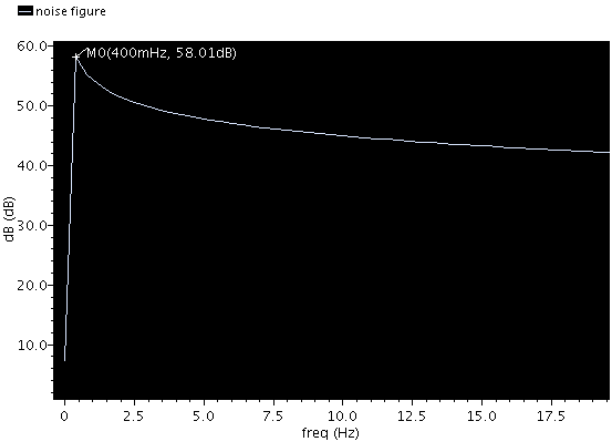

Figure 6. Noise figure of GAA fet

Table 1. Noise Parameters Comparison of Gate all Around and Double Gate in Subthreshold Regime

Parameters	**Gate-all-around silicon nanowire configuration**	**Double gate configuration**
Subthreshold	93.5 mV/decade	78.67 mV/decade
DIBL	66 mV/V	82.6 mV/V
I_{ON}/I_{OFF}	1.4×10^{7}	3.5×10^{4}
Noise figure	58.01 dB	62.7 dB
Equivalent noise resistance	2.168×10^{36} ohm	5.43×10^{27}

Table 1 describes the noise comparison between gate-all-around and double gate structure. It has been observed that noise figure is approximately equal to double gate by minimum margin. More flicker noise is contributed by double gate configuration as compared with GAA.

Table 2. Noise Figure and Equivalent Resistance at Different Voltage Supply

Voltage applied (V)	Noise figure dB	Equivalent noise resistance
0.8	61.5	3.76×10^{31}
1.0	58.01	2.168×10^{36}
1.2	53.98	6.937×10^{45}
1.4	43.34	3.43×10^{57}

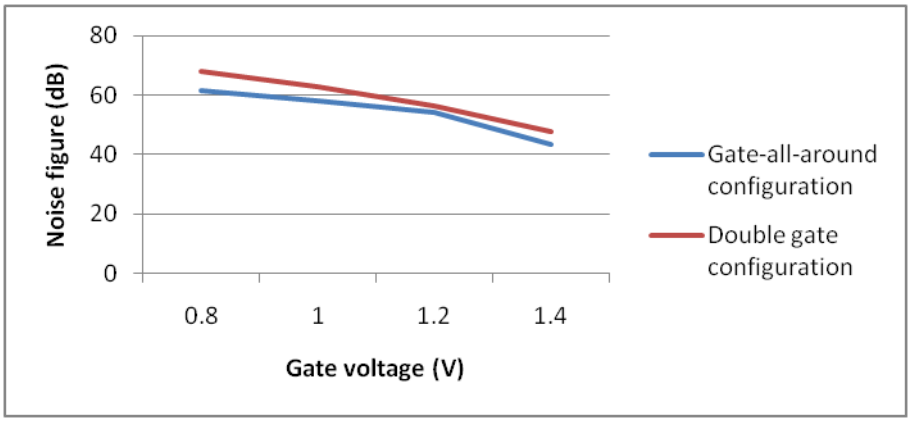

Figure 7. Noise Figure Comparison at Different Supply Voltages

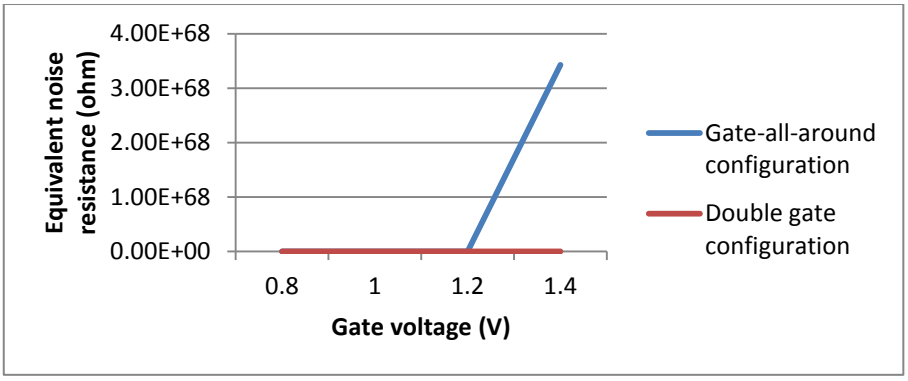

Figure 8. Equivalent Noise Resistance at Different Supply Voltages

4. Conclusion

In this paper result describe that drain current model is useful to evaluate output characteristics for short gate length in silicon nanowire gate-all-around configuration. It has been observed velocity overshoot increasing the transconductance and the noise with increasing temperature. Noise figure of higher value at low frequency show that

flicker noise contributes noise to the device at very low frequency and gate-all-around structure cancel out the flicker noise by induced gate noise. This paper compares the gate all around structure with double gate and it has been reported that GAA exhibit lower flicker noise, channel noise but higher gate induced noise as compared with double gate. GAA also provide the fhigher subthreshold regime, lower drain induced barrier lowering and higher on-off ratio as compared with double gate related devices.

Acknowledgements

The authors would have been grateful to ITM gwalior provide cadence software lab and valuable support by its staff.

References

[1] S. Bangsaruntip, G. M. Cohen, A. Majumdar and J. W. Sleight, "Universality of Short-Channel Effects in Undoped-Body Silicon Nanowire MOSFETs," IEEE Electron Device Lett., vol. 31, no. 9, **(2010)** September, pp. 903-905.
[2] B. Yu, Y. Yuan, J. Song and Y. Taur, "A two-dimensional analytical solution for short-channel effects in nano wire MOSFETs," IEEE Trans. Electron Devices, vol. 56, no. 10, **(2009)** October, pp. 2357–2362.
[3] N. Singh, K. D. Buddharaju, S. K. Manhas, A. Agarwal, S. C. Ru, G. Q. Lo, N. Balasubramanian and D. L. Kwong, " Si, SiGe nanowire devices by top-down technology and their applications", IEEE Trans. Electron Devices, vol. 55, no. 11, **(2008)** November, pp. 3107–3118.
[4] N. Singh, A. Agarwal, L. K. Bera, T. Y. Liow, R. Yang, S. C. Rustagi, C. H. Tung, R. Kumar, G. Q. Lo, N. Balasubramanian and D. L. Kwong, "High-Performance Fully Depleted Silicon Nanowire (Diameter ≤ 5 nm) Gate-All-Around CMOS Devices," IEEE Electron Device Lett., vol. 27, no. 5, **(2006)** May, pp. 383-386.
[5] J. Guo, J. Wang, E. Polizzi, S. Datta and M. Lundstrom, "Electrostatics of nanowire transistors," IEEE Trans. Nanotechnol., vol. 2, no. 4, **(2003)** December, pp. 329–334, ,
[6] S. H. Oh, D. Monroe and J. M. Hergenrother, "Analytical description of short-channel effects in fully depleted double-gate and cylindrical surrounding-gate MOSFETs," IEEE Electron Device Lett., vol. 21, no.9, **(2000)** September, pp. 445–447.
[7] B. Doyle, S. Datta, M. Doczy, S. Hareland, B. Jin, J. Kavalieros, T. Linton, A. Murthy, R. Rios and R. Chau, "High performance fully-depleted tri-gate CMOS transistor," IEEE Electron Device Lett., vol. 24, no. 4, **(2003)** April, pp. 263–265.
[8] C. P. Auth and J. D. Plummer, "Scaling theory for cylindrical, fully depleted, surrounding-gate MOSFETs," IEEE Electron Device Lett., vol. 18, no. 2, **(1997)** February, pp. 74–76.
[9] S. H. Oh, D. Monroe and J. M.Hergenrother, "Analytic description of short-channel effects in fully-depleted double-gate and cylindrical,surrounding-gate MOSFETs," IEEE Electron Device Lett., vol. 21, no. 9, **(2000)** September, pp. 445–447.
[10] B. Yang, K. D. Buddharaju, S. H. G. Teo, N. Singh, G. Q. Lo and D. L. Kwong," Vertical silicon nanowire formation and gate-all-around MOSFET,"IEEE Electron Device Lett., vol. 29, no. 7, **(2008)** July, pp. 791–794.
[11] S. Maheshwaram, S. K. Manhas, G. Kaushal, B. Anand and N. Singh, "Vertical silicon nano-wire gate-all-around field effect transistor based nanoscale CMOS," IEEE Electron Device Lett., vol. 32, no. 8, **(2011)** August, pp. 1011-1013.
[12] S. C. Rustagi, N. Singh, W. W. Fang, K. D. Buddaraju, S. R. Omampuliyar, S. H. G. Teo, C. H. Tung G. Q. Lo, N. Balasubramanian and D. L. Kwong, "CMOS inverter based on gate-all-around silicon- nanowire MOSFETs fabricated using top-down approach," IEEE Electron Device Lett.,vol. 28, no.11, **(2007)** November, pp. 1021–1024.
[13] G. J. Zhang, A. Agarwal, D. Buddharaju, N. Singh and Z. Gao, "Highly sensitive sensors for alkali metal ions based on complementary– metal–oxide–semiconductor-compatible silicon nanowire," Appl. Phys. Lett., vol. 90, no. 23, **(2007)** June, pp. 233 903.
[14] G. J. Zhang, G. Zhang, J. H. Chua, R. E. Chee, E. H. Wong, A. Agarwal and K. D. Buddharaju, "DNA sensing by silicon nanowire: Charge layer distance dependence," Nano Lett., vol. 8, no. 4, **(2008)** April, pp. 1066–1070.
[15] E. Stern, J. F. Klemic, D. A. Routenberg, P. N. Wyrembak and D. B. Turner-Evans, "Label-free immunodetection with CMOScompatible semiconducting nanowires," Nature, vol. 445, no. 7127, **(2007)** February, pp. 519–522.

[16] G. Baccarani and S. Reggiani, "A compact Double-Gate MOSFET model comprising quantum-mechanical and nonstatic effects", IEEE Transactions on Electron Devices, vol. 46, no. 8, **(1999),** pp**.** 1656-1666.
[17] A. Lazaro, B. Nae, O. Moldovan and B. Iniguez, "A compact quantum model of nanoscale double-gate metal-oxide-semiconductor field-effect transistor for high frequency and noise simulations", Journal of Applied Physics, vol. 100, no. 8, **(2006),** pp. 084320.
[18] O. Moldovan, B. Iniguez, D. Jimenez and J. Roig, "Analytical charge and capacitance models of undoped cylindrical surrounding-gate MOSFETs", IEEE Transactions on Electron Devices, vol. 54, no. 1, **(2007),** pp. 162-165.
[19] D. Esseni, M. Mastrapasqua, G. K. Celler, C. Fiegna, L. Selmi and E. Sangiorgi, "An experimental study of mobility enhancement in ultrathin SOI transistors operated in double-gate mode", IEEE Transactions on Electron Devices, vol. 50, no. 3, **(2003),** pp. 802-808.
[20] V. P. Trivedi, J. G. Fossum and F. Gamiz, "A compact QM-based mobility model for nanoscale ultra-thin-body CMOS devices", IEEE International Electron Devices Meeting, **(2004),** pp. 763-766.
[21] S. Reggiani, E. Gnani, A. Gnudi, M. Rudan and G. Baccarani, "Low-Field Electron Mobility Model for Ultrathin-Body SOI and Double-Gate MOSFETs With Extremely Small Silicon Thicknesses", IEEE Transactions on Electron Devices, vol. 54, no. 9, **(2007),** pp. 2204-2212.
[22] S. Akashe and S. Sharma, "Leakage Current Reduction Techniques for 7T SRAM Cell on 45nm Technology", Wireless Personal Communications, vol. 71, no.1, **(2013)** July, pp. 123-136.
[23] S. Akashe and S. Sharma, "High Density and Low Leakage Current based SRAM cell using 45nm Technology", International Journal of Electronic, vol. 100, no. 4, **(2013)** April.
[24] J.-P. Colinge, "Multiple-gate SOI MOSFETs", Solid-State Electronics, vol. 48, no. 6, **(2004),** pp. 897-905.

Author

Awanit Sharma was born in 8th Jan 1984.I received the Bachelor degree in Electronics and Communication Engineering from RGPV University, India and I am Master in Technology (VLSI) from ITM Gwalior, India. His current research interest include are VLSI design, Low power design, noise modeling of nanoscale semiconductor devices.

