International Journal of Hybrid Information Technology
Vol.7, No.2 (2014), pp.95-102
http://dx.doi.org/10.14257/ijhit.2014.7.2.10

A Failure Testing System with March C- Algorithm for Single Event Upset

Peng Wang[1], Zhen Li[2], Chengxiang Jiang[2], Wei Shao[2] and Qiannan Xue[1*]

[1]*Tianjin Key Laboratory for Civil Aircraft Airworthiness and Maintenance, Civil Aviation University of China, Tianjin 300300, China;*
[2]*College of Safety Science & Engineering, Civil Aviation University of China, Tianjin 300300, China*

**Corresponding author (E-mail:qiannanxue@163.com)*

Abstract

A testing system has been designed to detect the single event upset failure of SRAM chips in this paper: a visual test bench for failure monitoring is developed based on LabVIEW, it could perform the task of data acquisition, storage and results analysis. At the testing board, the test vectors based on March C- algorithm are written to the reference SRAM and the under-test SRAM through FPGA. NI HSDIO-6548 card is used to collect all the data from the SRAMs, judging whether SEU failure occurred according to comparison results. The system could accomplish the work of real-time monitoring the failure status and test process with a good extensibility.

Key words: *emulation test; Single Event Upset; LabVIEW; March C- algorithm; SRAM*

1. Introduction

SEE (Single Event Effect) is a kind of ionization effect. It refers to the phenomenon of a large number of charged particles pour into the electronic devices' sensitive area. SEE is one of the leading space radiation effects which caused failure or abnormal of airborne equipment. SEU (Single Event Upset) and SEL (Single Event Latchup) are two kinds of SEE phenomena which endanger the chips most. Therefore, they got wide range of attention. When high-energy particles, either in the air or on the ground, strike to the sensitive node of storage location or time sequence unit, the data in the logic device or memory would change due to the amount of electronic-hole pairs caused by ionization effect, at this moment, SEU has taken place [1-2].

SRAM (Static Random Access Memory) chips possess a super-speed and high stability in data storage, which made them widely used in aerospace system. In recent years, with the development of deep sub-micron technology, in order to meet the growing demand of integration and low power consumption, the size of the integrated device and the working voltage gradually reduced. When applied to airborne electronic equipment, these chips show the extreme sensitivity of SEU. With the continuous progress of integrated circuit technology, SEU is not only a serious problem in space environment, but also gradually becomes a worthy question in the low altitude and ground environment [3-4].

This paper focus on the problem of read/write errors in SRAM memory caused by SEU failure, set up a visual SEU failure test platform using NI HSDIO (High Speed Digital Input Output) card and LabVIEW software. The host computer executes the task of data acquisition and failure state real-time monitoring; on the testing board, the same specific test vectors

ISSN: 1738-9968 IJHIT
Copyright ⓒ 2014 SERSC

based on March C- algorithm are written to the reference SRAM and under-test SRAM. Experiments show that the platform could display the SEU failure index number of under-test SRAM, complete the testing work correctly. This testing system has high real-time performance, could make quick response to failure state. At the same time, data processing task are performed on the host computer, not only saves the hardware cost, but also improves the working efficiency.

In this paper, the testing system is introduced from the following aspects, the first part is the basic theory of March C- algorithm, the second part includes the main components and principle of the testing system, the third part introduces the working process and results analysis, the fourth part brings up the conclusion.

2. March C- algorithm Description

March algorithm is the most commonly used algorithm in memory test. Finite state machine is used to perform read and write operation one by one until all addresses are covered, ensure that each test vector between any two bytes occur at least once “00”, “01”, “10” and “11”. For the sake of checking the influence of read/write order, address increasing and decreasing operations are respectively used [5]. March algorithm is a byte oriented algorithm, a series of operations are carried out at a storage unit then move to the next one. The works include the inside test of each unit and also faults among them. Through continuous read and write operations, the system could detect almost all the memory faults.

March algorithm is put forward by Marinescu in the year of 1982, it could detect the fixed faults, the conversion faults and most of the coupling faults in a memory. In 1991, Van DE Goor proposed March C- algorithm based on the basic principle of March C, lower its complexity but could obtain the same fault coverage. The basic operation steps of March C-algorithm is as follows: [6-7]

M0: in accordance with any address order, write 0 to all the storage units;

M1: in accordance with the rising address order, read 0 from all the storage units, and write 1 to them;

M2: in accordance with the rising address order, read 1 from all the storage units, and write 0 to them;

M3: in accordance with the decreasing address order, read 0 from all the storage units, and write 1 to them;

M4: in accordance with the decreasing address order, read 1 from all the storage units, and write 0 to them;

M5: in accordance with any address order, read 0 from all the storage units;

In this paper, the lower eight data bits of SRAM are checked to find the failure of SEU. Based on March C- algorithm, four kinds of test vectors “0x00”, “0xFF”, “0x55” and “0xAA” are written to the reference SRAM and under-test SRAM, guarantee that each storage unit’s each bit could complete 0/1 data traversal.

3. The Main Components and Principle of Testing System

The mainly function of the system is to test the data correctness in SRAM chips. Data collected from the receiving end, whether in reference SRAM or under-test SRAM, are all real-time compared to judge whether SEU failure happened. The testing system mainly consists of the following modules, as shown in Figure 1:

 Copyright ⓒ 2014 SERSC

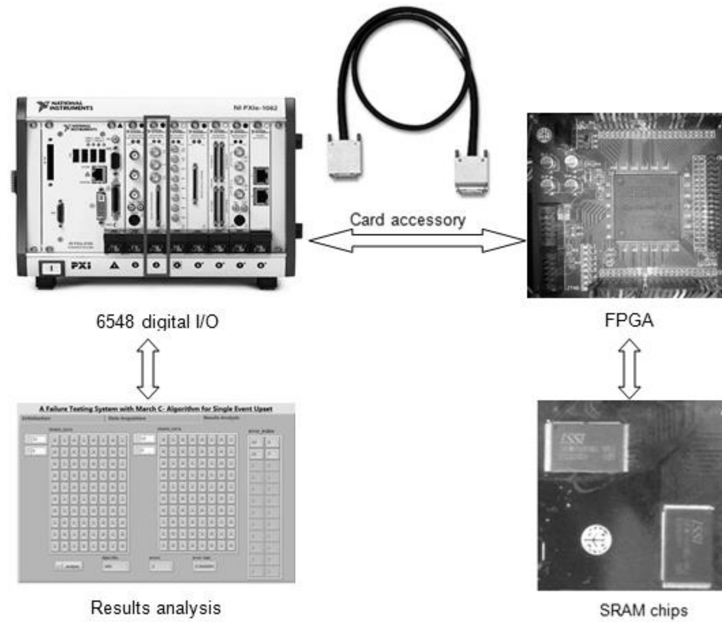

Figure 1. Main components of the testing system

The 6548 digital card is embedded in the PXIe-1082 chassis. It undertakes the task of data and commands transmission in the whole system. LabVIEW software could help users controlling the test work conveniently on a visual interface. The FPGA minimum system development board connected with two pieces of SRAM chips: in testing process, the same vectors are written to the two SRAM chips at the same time through the Verilog HDL language which programmed based on March C- algorithm [8-11].

3.1. The brief introduction of LabVIEW visual test platform

LabVIEW visual test platform includes initialization module, data acquisition module and results analysis module. Initialization module is to complete the configuration of 6548 card, such as acquisition channels selection and sampling clock frequency definition, it also set the file storage path of the received data and their comparison results. The working state of data acquisition module is shown in Figure 2, 6548 card collect the data from the two SRAM chips and send them to LabVIEW software for further analysis. The comparison results displayed on LabVIEW front panel in real time, SRAMs' current state could be judged by the color of the lights, whether they are in read/write state or the failure happened. Comparison results are displayed in the form of digital waveform graph, "0" indicates that the SEU failure is not happened at the current address, "1" indicates that SEU failure is detected. Progress indicates the March C- algorithm steps (M0 ~ M5) executed currently, implementation schedule indicates the completion of the whole state machine cycle. This module could monitor the working state of the system at any time, so, the platform improves the testing efficiency greatly.

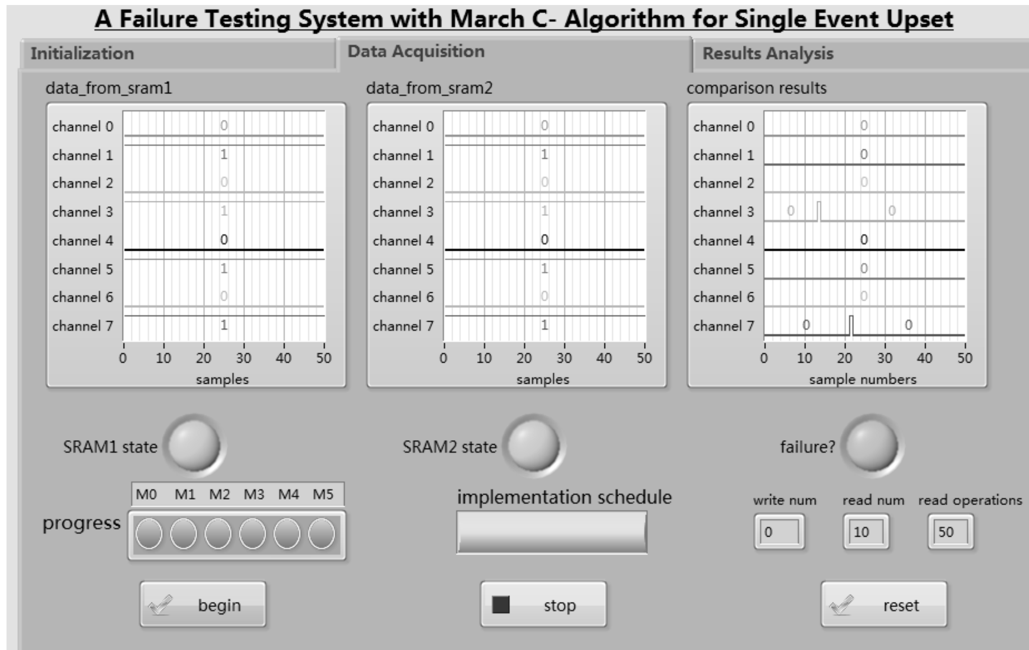

Figure 2. Working state of the data acquisition module

The results analysis module displays all the data acquired from the two SRAMs, counts SEU faults and calculates the error rate. Error addresses and data bits could be tracked conveniently and accurately through the failure index number, thus debugging time is saved and the reliability of test work enhanced. In addition, the collected data, the comparison results and failure index numbers will be stored in the file, easy to verify the results and make deep analysis.

3.2. Test vectors ejected procedure

FPGA board's mainly function is to control the read or write operation of the two SRAM chips. Verilog HDL language is used in this paper to write the programs of finite state machine based on March C- algorithm. Suppose that the test vector of each data bit is "0", figure 3 describes the transitions of the relationship between the states:

Among them, the "idle" state indicates that SRAM chips are neither in the state of read nor write; the SRAM operation addresses and read/write enable signals are configured in the states of "setting1" and "setting2"; the states of "address add" and "address minus" complete the operation addresses' transition after the "read before write" in the same storage unit; The whole state machine judges the transition condition according to the addresses information and some additional control signals [12].

 Copyright ⓒ 2014 SERSC

Figure 3. Finite state machine transitions based on March C- algorithm

4. Test Process and Results Analysis

4.1. Functional simulation of the testing system

Modelsim is used to simulate this test. March C- algorithm's M1 step is simulated as shown in figure 4. Among them, "sram1_addr" and "sram2_addr" respectively refers to the current operation address of the two SRAM chips; "data_from_sram" and "sram_data" shows the data read from the current address of SRAMs and the data on the SRAMs data cable separately; "rd_cnt" and "wr_cnt" indicate the numbers of read or write operations; "state" and "next" mean the current state and the next state the program would jump to. It could be seen from the diagram, when the operation addresses change, "rd_cnt" changes prior to "wr_cnt" and the read operation begins: as shown of the signals "sram1_data" and "sram2_data", data "55" are read from SRAM chips which were written into them at the last step of M0, and then the data are transferred to "data_from_sram1" and "data_from_sram2", after this, the new data "AA" are written to the same operation addresses, at last, addresses would change and the new cycle come.

The type of SRAM chips used in this paper shares one cable to judge whether it is in the state of read or write: at the low voltage SRAM could be written, else, it is in the state of read. As shown in the picture, if SRAM chips are not in the state of read, "data_from_sram1" and "data_from_sram2" are all in the state of high impedance, there are not any outputs from the acquire channels. The simulation analysis result has shown that the state machine could well complete the basic function of March C- algorithm, thus the testing work could be carried out successfully.

Copyright ⓒ 2014 SERSC

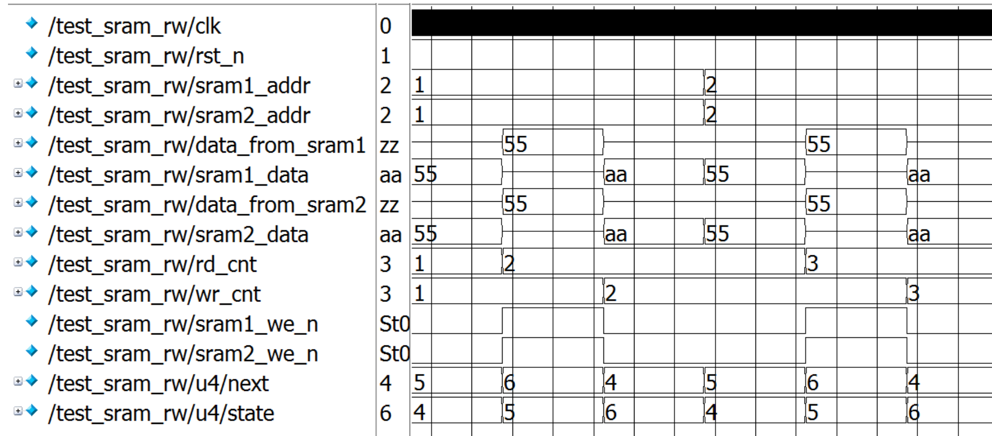

Figure 4. March C- algorithm's simulation results in Modelsim

4.2. Test for SRAM chips

Click the "begin" button on LabVIEW front panel, 6548 card start the sample clock to monitor the data on the acquisition channels. The "read number" and "write number" display read and write operations at the step of M0~M5. Parallel to the data acquisition progress, 6548 card checks the completion status of the program, when a complete state machine cycle is performed successfully, "test done" dialog box popped up to instruct the user to complete the test work.

Different from the traditional behavior which distribute data comparison and results analysis to FPGA, in this paper, LabVIEW daemon is used to assume these responsibilities, on one side, such conduct reduces signal transmission channels, saves the hardware cost, and on the other side, it decreases the workload of FPGA and shortens the test cycle. In this mode, the host controller and the slave one share the tasks and work at the method of streamline, give LabVIEW full play to the function of data processing. Experiments have proven this mode could improve the test efficiency to a great extent. In the result analysis module, all acquired data will be written into arrays. Table 1 shows the results when the failure occurred, the error data bits could be found conveniently and quickly [13-14].

Table 1. SEU test results analysis of SRAM chips

	Data from SRAM1								Data from SRAM2								Error_ Channel
Channel	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	
…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…
Line 13	0	1	0	1	0	1	0	1	0	1	0	0	0	1	0	1	3
Line 14	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	
Line 15	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	
Line 16	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	
Line 17	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	
Line 18	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	
Line 19	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	
Line 20	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	
Line 21	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	1	7
Line 22	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	
…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…

 Copyright ⓒ 2014 SERSC

According to literature [15], 90nm SRAM's relative SEU rate in FITs/kbit is 1.0. Depend on Table 1, there are 2 failures occurred at ten addresses, the frequency of system clock is 1ms, it could be reckoned this SRAM's relative SEU rate in FITs/kbit is 0.075, this mean time between failures is far less than 1.0, and there are reasons to certify this testing system's reliability.

5. Conclusions

Based on March C- algorithm, in this paper, an SEU failure testing platform of SRAM chips is built. The system realizes the function of virtual instrument's control to the traditional ones in a visual interface. This system could monitor the failure status and testing progress, display the SEU failure data bits and track the failure addresses quickly, make the test work simple. In addition, the system has good environmental adaptability and extensible ability. Other different chips could develop corresponding test functions based on it.

Acknowledgements

This paper was funded by "Joint Fund of the National Natural Science Foundation of China and the Civil Aviation Administration of China (No. U1333120), the Fundamental Research Funds for the Central Universities of China (No. 3122013P004), and the Research Startup Foundation of Civil Aviation University of China (No. 2012QD26X)".

References

[1] H. Jian-wei and Z. Zhen-long, "Single Event Latchup Test of Extreme Sensitive Device and Warning for China's Space Security", Spacecraft Environment Engineering, vol. 25, no. 3, (**2008**), pp. 263-268.
[2] S. G. Shi-peng and F. Guo-qiang, "Experimental Study on Single Event Effects of Deep Sub-micron SRAM Simulated by Pulsed Laser", Atomic Energy Science and Technology, vol. 46, no. 8, (**2012**), pp. 1019-1024.
[3] W. Liang and Y. Su-ge, "A Kind of Mechanism of Single Event Upset and its Mitigation", Information and Electronic Engineering. vol. 10, no. 3, (**2012**), pp. 355-358.
[4] W. Mansour and R. Velazco, "SEU Fault-Injection in VHDL-Based Processors: A Case Study", Electron Test, vol. 29, (**2013**), pp. 87-94.
[5] Z. Zheng-jun and C. Xin-ming, "Design of a Memory Test Controller Based on March Algorithm", Microcomputer Information, vol. 23, no. 0-2, (**2007**), pp. 107-109.
[6] B. Shi, "Research on Design for Testability and Test Algorithm of Embedded Memory", Harbin: Harbin Institute of Technology, (**2009**).
[7] Z. Hui, "Application of the Improved March Algorithm in Memory Exceptional Test Abstract", Xiamen: Xiamen University, (**2008**).
[8] C. Xi-hui and Z. Yin-hong, "LabVIEW 8.20 programming from entry to the master", Beijing: Tsinghua University Press, (**2007**).
[9] Data Acquisition Programming Guide, gsdzone.net/community.
[10] NI_PXIe-6544/6545/6547/6548_Specifications, http://digital.ni.com/manuals.nsf/websearch/E28F145FF2CE8076862577500074C296.
[11] M. Rebaudengo, M. Sonza and M. Violante, "Analysis of SEU effects in a pipelined processor", www.cad.polito.it.
[12] W. Xiao-liang, "The Design of Memory Testing System based on LabVIEW", Changsha: Hunan University, (**2012**).
[13] S. Ning-fang, Q. Jiao-mei, P. Xiong and J. Yun-tian, "Evaluating SEU Effects in SRAM-Based FPGA with bit-by-bit Upset Fault Injection", Journal of Beijing University of Aeronautics and Astronautics, vol. 38, no. 10, (**2012**), pp. 1285-1289.
[14] Z. Qiu-yan, W. Zu-lin and G. Xu-jing, "A Kind of SRAM-based FPGA SEE Fault Injection Method", Electronic Measurement Technology. vol. 7, (**2011**), pp. 23-25.
[15] A. Dixit, R. Heald and A. Wood, "Trends from ten years of soft error experimentation", System Effects of Logic Soft Errors (SELSE), (**2009**).

Copyright ⓒ 2014 SERSC

Authors

Peng Wang

He was born in 1982, he incepted his master degree in ENSICA (École Nationale Supérieur d'Ingénieurs deConstructions Aéronautique) in 2005.

Now he is working in Airworthiness Certification Technology Research and Management Center, Civil Aviation University of China, as an associate professor. He mainly engaged in the commercial system security design and evaluation, airborne electronic hardware airworthiness technology research.

Zhen Li

He was born in 1989, now is a master's student. He mainly engaged in civil aircraft research of airborne electronic hardware fault injection method.

Chengxiang Jiang

He was born in 1988, now is a master's student. He mainly engaged in the mitigation technology of single event upset in avionics application.

Wei Shao

He was born in 1990, now is a master's student. He mainly engaged in civil airborne electronic hardware design and validation.

Qiannan Xue

She was born in 1984. She incepted his Ph.D. degree in Institute of Electronics, Chinese Academy of Sciences in 2012. She is a research associate now. Her major is civil airborne electronic hardware design and the study of airworthiness approval.

 Copyright ⓒ 2014 SERSC