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A Low Power 5.8GHz Fully Integrated CMOS LNA for Wireless Applications

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Abstract

A low power 5.8 GHz fully integrated CMOS low noise amplifier (LNA) with on chip spiral inductors for wireless applications is designed based on TSMC 0.18 μm technology in this paper. The cascode structure and power-constrained simultaneous noise and input matching technique are adopted to achieve low noise, low power and high gain characteristics. The proposed LNA exhibit a state of the art performance consuming only 6.4mW from a 1.8V power supply. The simulation results show that it has a noise figure (NF) only 0.972 dB, which is perfectly close to NF_{min} while maintaining the other performances. The proposed LNA also has an input 1-dB compression point (IP_{1dB}) of -21.22 dBm, a power gain of 17.04 dB, and good input and output reflection coefficients, which indicate that the proposed LNA topology is very suitable for the implementation of narrowband LNAs in 802.11a wireless applications.

Keywords: *CMOS, low power, low noise amplifier, noise figure*

1. Introduction

During the recent years radio frequency (RF) and microwave electronics have faced with the following major advances: the boom of telecommunications market; a rise in application frequency; the emergence of silicon-based processes in the microwave area [1]. Moreover, the widely application of the high-speed (up to 54Mb/s) wireless local area network (WLAN), which makes all kinds of portable wireless communication products have considerably developed and the demands for higher frequency band, faster transfer rates and wider bandwidth RFIC has also rose sharply in consumer electronics market. Some WLAN standards such as IEEE 802.11a (5-5.825GHz), IEEE 802.11n (2.4-2.485GHz and 5.725-5.825GHz) and U-NII (5.15-5.35GHz and 5.725-5.825GHz) require a transceiver with approximately 5.5GHz center frequency [2]. In order to satisfy this increasingly requirement, more and more companies and research institutions have increased input to the integrated circuit industry.

Just as know, in millimetre-wave receiver design, the low-noise amplifier (LNA) is a critical building block that amplifies the received signal and contributes most of the noise figure of the whole receiver [3]. In order to replace the external off-chip LNAs with CMOS LNAs, the noise figure (NF) less than 1 dB is required with lower consumption. Adding in progressively lower power dissipation constraints inherent to battery-powered portable applications, a primary challenge in LNA design is achieving simultaneous noise and input matching at any given amount of power dissipation. Moreover, the amplifier's compression point requirement also imposes a limitation on the LNA transistor size, making the simultaneous noise and input match even more difficult to achieve in practice [4]. Therefore, many kinds of amplifier topologies have been proposed as a way to satisfy the requirement

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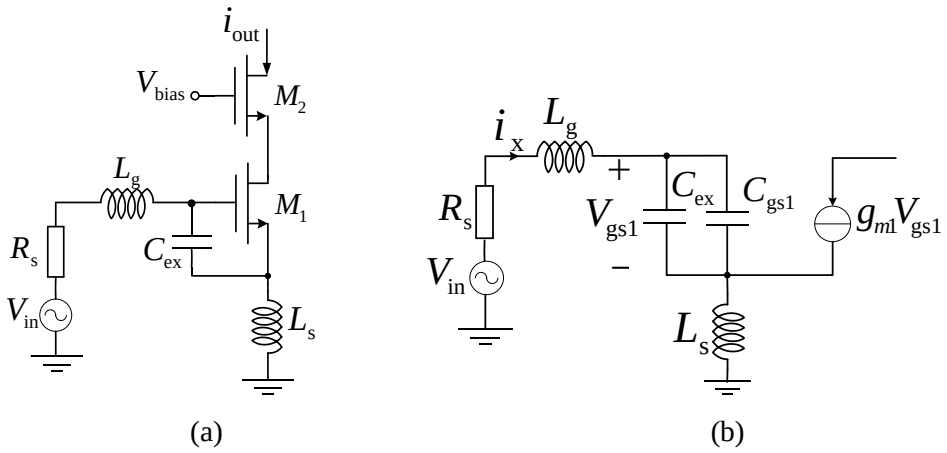
for low power dissipation as well as other good performances. In this paper, a 0.18μm CMOS LNA simultaneously achieving input impedance and minimum noise matching, and excellent noise figure has been designed, which is suitable for IEEE 802.11a wireless applications. This paper is structured as follows. In Section 2 is the description about the circuit design and analysis, including the LNA topology, the noise analysis, and the LNA circuit design. Section 3 presents the simulation results and discussion, which following by the conclusion about the achievement and results.

2. Circuit Design and Analysis

2.1. Topology

Figure 1(a) shows the traditional cascode structure with the inductive source degeneration. Its small signal equivalent circuit for impedance calculation is shown in Figure 1(b).



(a) (b)

Figure 1. (a) The Cascode LNA With Inductive Degeneration; (b) Small Signal Equivalent Circuit of Figure 1(a)

A capacitor C_{ex} is connected between gate and source of the input transistors M1 to achieve noise and input impedance match simultaneously [3]. This well-know structure is widely used due to its high gain and the increase in the output impedance, as well as better isolation between the input and output ports. The input impedance of this LNA can be equal to (1), in which the gate resistance and the total parasitic capacitances except gate-source capacitances are neglected to simplify the analysis.

$$Z_{in} = j\omega(L_g + L_s) + \frac{1}{j\omega(C_{gs1} + C_{ex})} + \frac{g_{m1}}{C_{gs1} + C_{ex}} L_s \quad (1)$$

Where C_{gs1} and g_{m1} are the intrinsic gate-to-source capacitor and the transconductance of M1, respectively. When the input impedance matching network composed by L_g, L_s and C_{ex} resonating at the operating frequency, the imaginary part of Z_{in} is eliminated. The impedance becomes a pure real part and only relevant to L_s and C_{ex}, Therefore, by adjusting L_s and C_{ex} can easily realize to real $50\,\Omega$ resistance at the input of the LNA.

2.2 Noise analysis

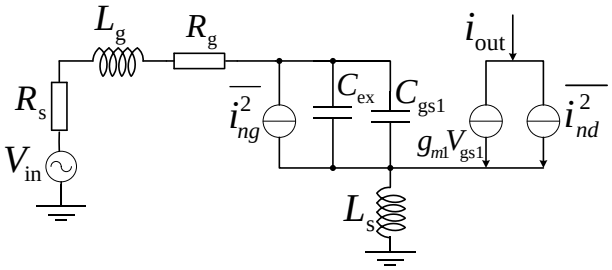


Figure 2. The Small Signal Noise Equivalent Circuit of the Input Stage

Figure 2 is the simplified small signal noise equivalent circuit. Because the derivation of the complete noise figure equation (taking into the effect of all existing parasitic effects in the circuit) would be quite cumbersome, and the obtained results would not give an insight into how to choose design parameters such as the width and the biasing of the transistors. Therefore, if the noise contribution from the cascode stage is ignored, the noise factor of the cascode LNA becomes [5-6].

$$F = 1 + \frac{R_g}{R_s} + \frac{\gamma}{\alpha}\chi g_m R_s (\frac{\omega_0}{\omega_T})^2 \tag{2}$$

$$\chi = 1 + 2|c|Q_{in}\sqrt{\frac{\alpha^2\delta_{eff}}{5\gamma}} + \frac{\alpha^2\delta_{eff}}{5\gamma}(1+Q_{in}^2) \tag{3}$$

$$Q_{in} = \frac{1}{\omega_0(c_{gs1}+c_{ex})R_s} \tag{4}$$

Where R_s is the input voltage source resistance, R_g is the gate resistance of M1, ω_0 is the operating frequency, α , δ_{eff} and γ are bias-dependant parameters. The inductive source degeneration is employed to make Z_{in}^* (where Z_{in}^* is the complex conjugate of the amplifier input impedance Z_{in}) close to Z_{opt}, as derived in Equation (5).

$$Z_{opt} = \frac{\alpha\sqrt{\frac{\delta_{eff}}{5\gamma(1-|c|^2)}} + j(\frac{c_t}{c_{gs}} + \alpha|c|\sqrt{\frac{\delta_{eff}}{5\gamma}})}{\omega c_{gs}\left\{\frac{\alpha^2\delta_{eff}}{5\gamma(1-|c|^2)} + (\frac{c_t}{c_{gs}} + \alpha|c|\sqrt{\frac{\delta_{eff}}{5\gamma}})^2\right\}} - sL_s \tag{5}$$

Where Z_{opt} is the optimum noise impedance. Note that in equation 2 the second term shows the noise due to the gate resistance, which can be minimized by careful layout

techniques. By increasing the number of fingers in the layout design we can effectively reduce this resistance. Therefore, the only term which is of our concern should be optimized is the third one. Based on the methodology in [3], simultaneous input impedance and noise matching at 5.8GHz frequency are achieved by appropriately selecting the values of L_g, C_{ex}, L_s, the size and bias of the input transistor M1. Nevertheless, to reach simultaneously noise and power exactly matching at power constrained condition is a very difficult job in practice. Because that the LNA design involves trade-offs between noise-figure, gain, power dissipation, input matching, and harmonic content in the output signal. In this circuit, the capacitor C_{ex} is a key component, which has a great effect on NF and the available power gain of the LNA. Too much C_{ex} will lead to the deterioration of noise and gain due to the degradation of the cutoff frequency of the composite transistor ($f_T \approx g_{m1}/(c_{gs}+c_{ex})$). The relationship between the different capacitance C_{ex} and NF and gain are shown in Figure 3 and Figure 4, respectively. It can be seen that the value of C_{ex} has a great influence on the NF and power gain.

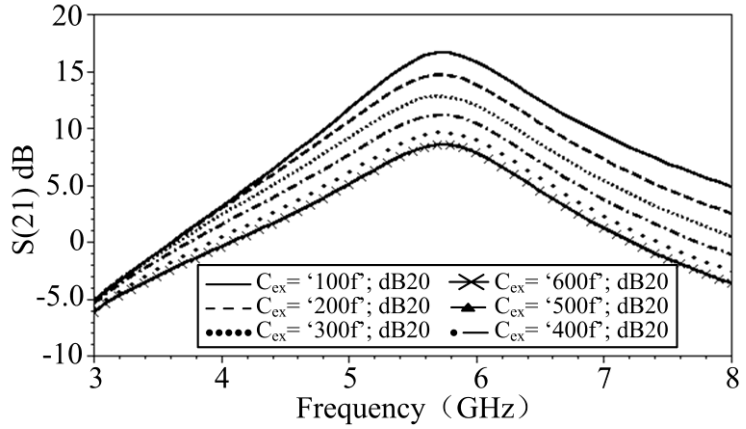


Figure 3. The Relationship Between the Capacitance C_{ex} and the Gain S_{21}

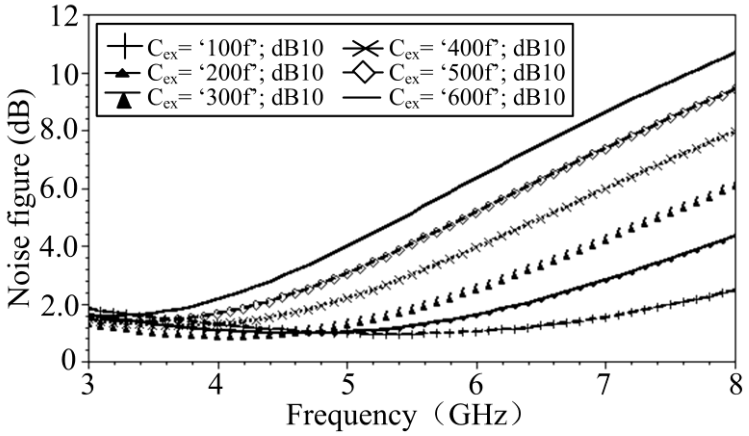


Figure 4. The Relationship Between the Capacitance C_{ex} and the Noise *NF*

2.3 The LNA circuit design

Based on the traditional cascode structure as analysis above, we propose the LNA schematic as shown in Figure 5.

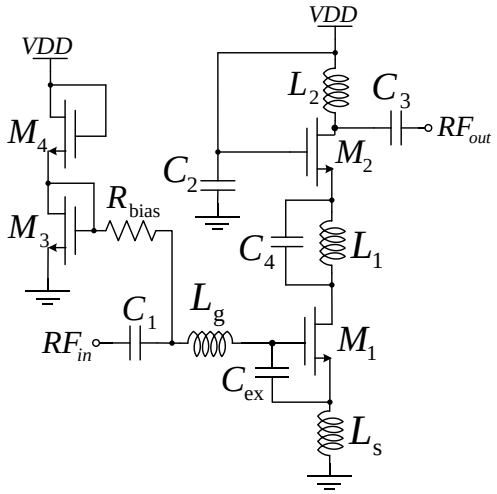


Figure 5. Complete Schematic of the LNA

In this circuit, transistors M1 and M3 form a cascade topology to provide better reverse isolation and reduce the Miller effect. The inductance L_1 and capacitance C_4 are inserted between the cascade transistor M1 and M2 for inter-stage matching to improve the LNA gain and noise performance. The inductances L_s, L_g and the additional capacitance C_{ex} consist of the input matching network of this LNA to match the signal source impedance (50 Ω) at the operating frequency. Their sizes depend on the input transistor size. When selecting the input transistor's size, a major design tradeoff is that the current density required for minimum noise figure [13]. In order to obtain the best noise performance, the optimum width of the input transistors (M1, M3) was chosen here according to [13], where the noise figure was optimized under power constrain.

$$W_{opt} \cong \frac{1}{3\omega L C_{ox} R_s} \tag{6}$$

Where ω, L, C_{ox} and R_s are the operating frequency, the length of the input transistors, the gate capacitance per area and the source resistance, respectively. According to [12], once those devices size are determined, the optimum impedance needed to be matched to the optimal noise matching is also determined. Transistors M3, M4 are used to bias the LNA by mirroring the reference current to the transistor M1. The value of the bias resistant R_{bias} is about 2~4 kΩ, which can avoid the signal path disturbed by the biasing circuit and mitigate the effect of gate-source capacitance of the transistor M3.

3. Simulation Results and Discussions

The LNA has been implemented in a TSMC 0.18-μm RF process. The lengths of all the transistors adopt the minimum channel length 0.18μm to obtain a higher cutoff frequency. The main component parameters of the LNA are listed as follows: the overdrive voltage of

M1 is 81mV, the gate-width of M1 and M2 are 134.9 μm. The designed LNA including the bias circuit draw only 3.56 mA current from power supply of 1.8 V. Therefore, the overall DC power consumption is 6.4 mW. This is relatively low for a 5.8 GHz CMOS LNA with a power gain greater than 17.04 dB.

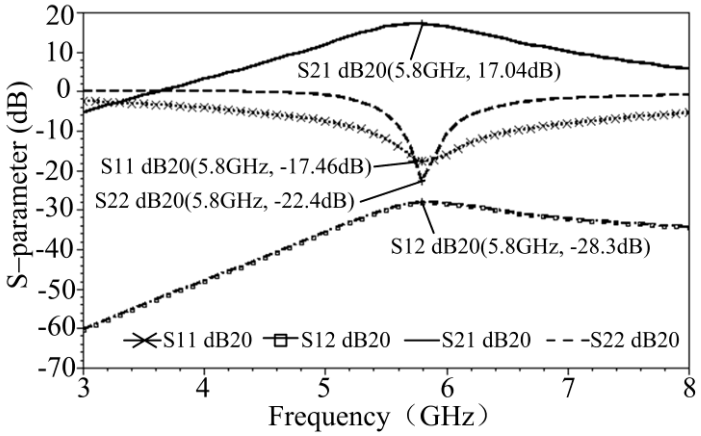


Figure 6. Simulated S-parameters of the LNA

Figure 6 presents the simulation results of the scattering parameters of the LNA. In the operating frequency of 5.8 GHz, a power gain S_{21} of 17.04 dB is achieved and remains above 16 dB over the band 5.5-6 GHz. The input return and output return losses (S_{11}, S_{22}) of the LNA are -17.46 dB and -22.4 dB at 5.8 GHz, respectively. This illustrates that the LNA circuit has exhibited a good input and output matching at the operating band. Due to the utilizing cascade structure, the propose LNA circuit also achieves a good reverse isolation lower than -28.3 dB over the band from 3-8 GHz.

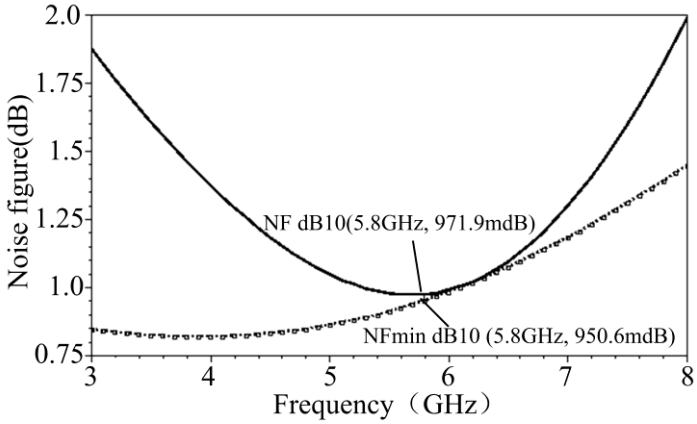


Figure 7. The Simulation of Noise Figure

Figure 7 presents the noise simulation result of the proposed LNA. It can be seen that the noise figure is 0.9719 dB at the central frequency 5.8 GHz, and with a NF ripple of $\pm$ 0.01 dB in the frequency range of 5.25-5.825 GHz, which is excellent compared to recently reported designs. Note that, the NF of the LNA coincides with NF_{min} =0.9506 dB very well at the

frequency of 5.8 GHz. The result illustrates that the noise performance is better than most previous CMOS LNAs.

Figure 8 shows the simulation result of the input 1-dB compression point (IP_{1dB}). An input sinusoidal signal with a frequency of 5.8 GHz is used. It can be seen that the value of IP_{1dB} is about -21.22 dBm.

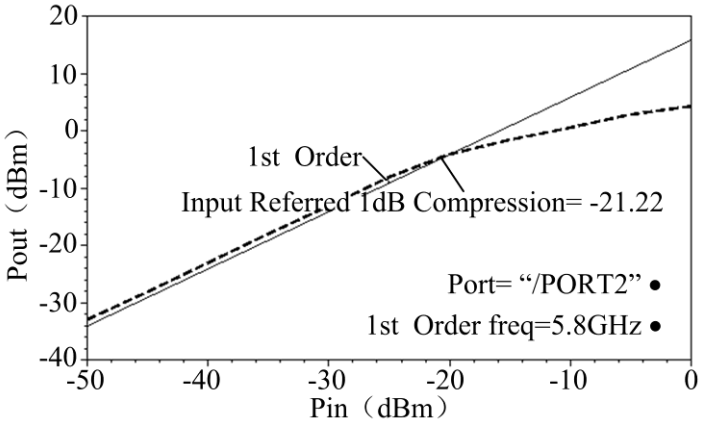


Figure 8. The Simulation Result of the Input 1-dB Compression Point

In order to remain stable for all source impedance at all frequencies and avoid oscillate at any frequency, the LNA circuit must be satisfy the unconditionally stable. It has been shown that stability factor Kf>1 (or Bf>0) alone is necessary and sufficient for a circuit to be unconditionally stable [7]. Figure 9 shows the simulated stability factors Kf and Bf versus frequency characteristics of the LNA. According to the Rollett stability criteria for unconditional stability, defined as [11]

$$K = \frac{1-|S_{11}|^2-|S_{22}|^2+|S_{11}S_{22}-S_{12}S_{21}|^2}{2|S_{12}||S_{21}|} > 1 \qquad (7)$$

the LNA satisfies the unconditional stability requirement over a range of 3–8 GHz. It means that the LNA will not oscillate with any combination of source and load impedances.

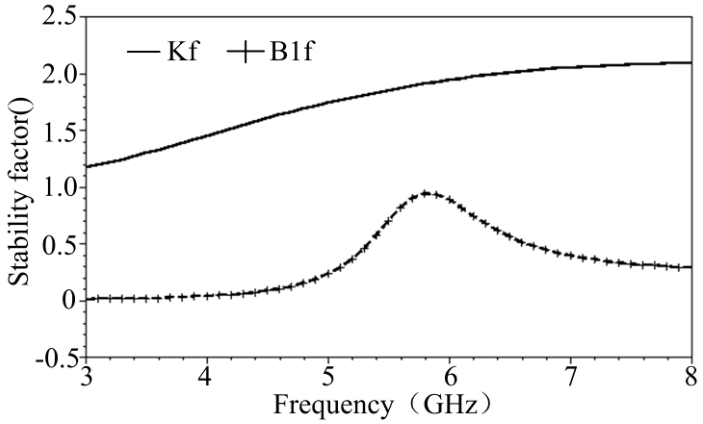


Figure 9. Simulation Result of the LNA Stability

Table 1 summarizes the performance of the proposed CMOS LNA compared to the recently reported literatures. As can be seen from table1, the proposed LNA achieves a lower noise figure, a higher voltage gain and a smaller power dissipation compared to prior techniques listed. These results demonstrate that the proposed LNA is suitable for IEEE 802.11a, 802.11n wireless applications [14-15].

Table 1. Comparison Between This Work and Other Reported Literatures.

Reference	Technology	Freq(GHz)	NF(dB)	Pdc(mW)	S21(dB)	S11(dB)	S22(dB)
[1]	0.35μm BiCMOS	5.8	3.0	3.8	12.1	−20.7	−9
[2]	0.18μm CMOS	5.5	3.12	3.0	20.63	−29.5	−25
[4]	0.18μm SOI	5.0	0.95	12.0	11.0	−33	−
[8]	0.25μm CMOS	5.745	5.48	6.12	24.6	−17.3	−5.3
[9]	0.18μm CMOS	5.8	2.0	16.0	14.1	<−10	−11
[10]	0.18μm BiCMOS	5.8	2.0	32.4	18.8	<−10	<−10
This work	0.18μm CMOS	5.8	0.97	6.4	17.04	−17.5	−22.4

4. Conclusion

In this work, we present a 5.8 GHz fully integrated LNA design and simulation using TSMC 0.18 μm RF process. The cascade topology was chosen for this design as it offers higher power gain, better reverse isolation and reduces miller effect. Simulation results have shown that the proposed LNA circuit consumes only 6.4 mW from a 1.8V supply voltage while achieving a power gain of 17.04 dB, a excellent noise figure 0.972 dB at the operating frequency 5.8 GHz. Considering the performance achieved, the proposed techniques demonstrate to be very suitable for the implementation of narrowband LNAs in wireless applications.

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